Electronics and Noise: MicroBooNE Experience and SBND/ProtoDUNE-SP Status

H. CHEN ON BEHALF OF THE COLD ELECTRONICS TEAM

BROOKHAVEN NATIONAL LABORATORY

MAY 15TH, 2017

70 YEARS OF DISCOVERY

A CENTURY OF SERVICE

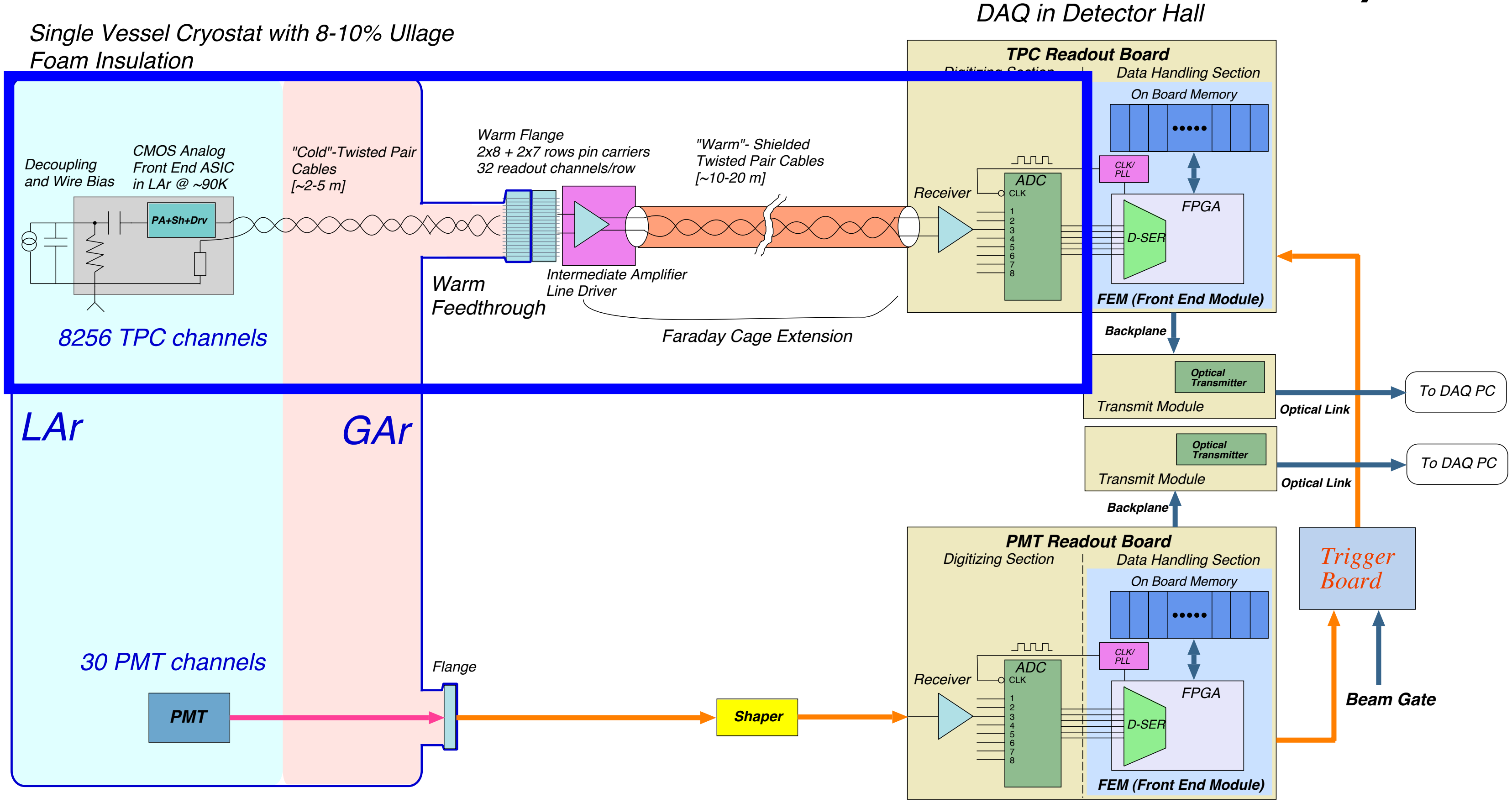
U.S. DEPARTMENT OF ENERGY

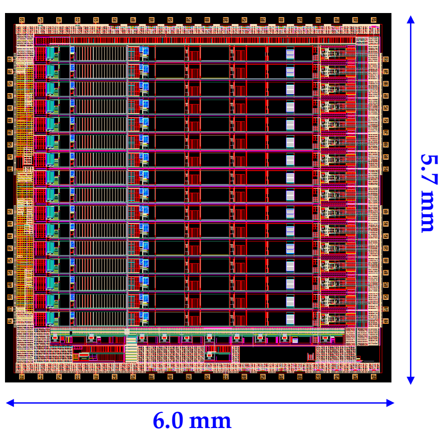
BROOKHAVEN NATIONAL LABORATORY

Outline

- MicroBooNE Experience
  - Readout Electronics System for MicroBooNE
  - MicroBooNE Noise Performance
- SBND/ProtoDUNE-SP Status
  - Readout Electronics System for SBND and ProtoDUNE-SP
  - Status of SBND/ProtoDUNE-SP Electronics Development
  - System Integration Test
- Summary

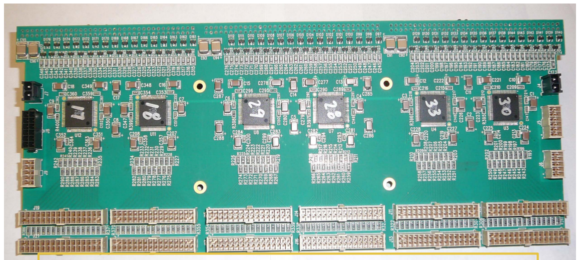
MicroBooNE Readout Electronics System



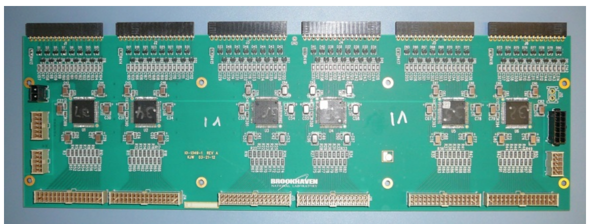


- MicroBooNE is the first experiment instrumented with cold CMOS ASICs
- Analog front end ASIC designed in 180 nm is running in LAr (~89 K) to achieve optimal signal to noise ratio
- The MicroBooNE front end readout electronics system was designed as an *integral system*, with TPC, signal feed-through and warm interface electronics

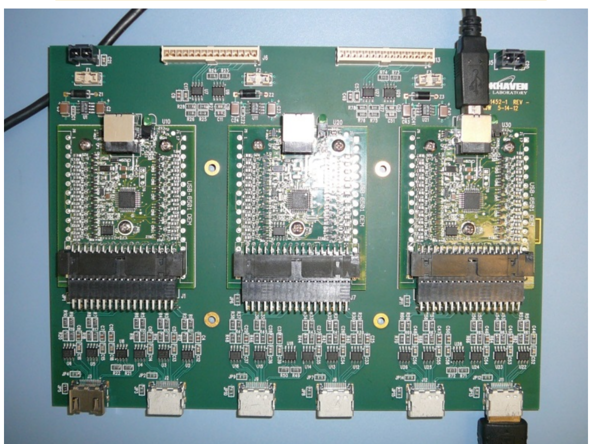
MicroBooNE Front End Electronics



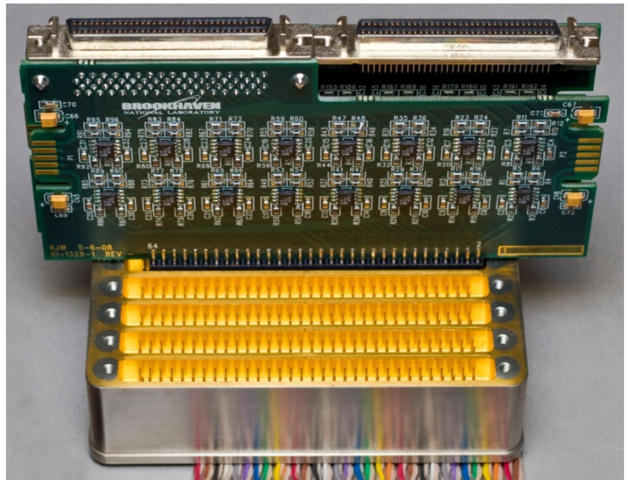
H. Cold Mother Board



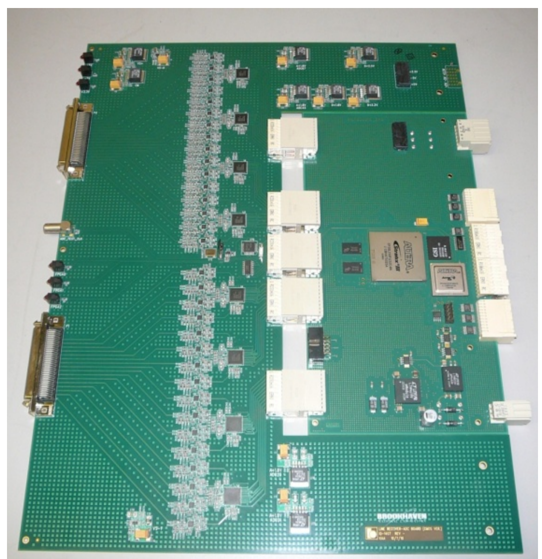
V. Cold Mother Board



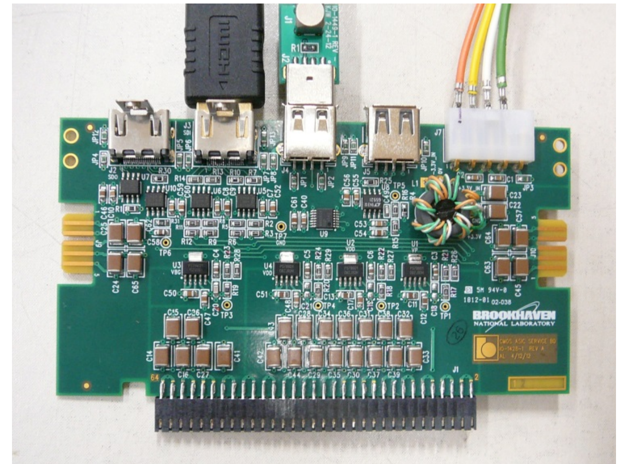
ASIC Configuration Board



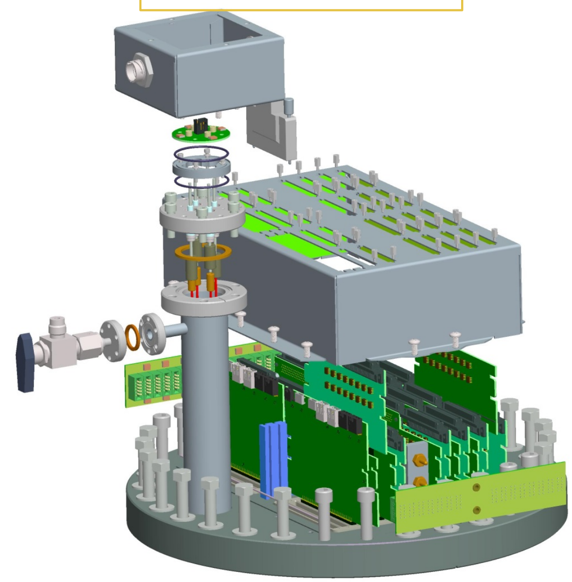
Intermediate Amplifier



Receiver ADC Board

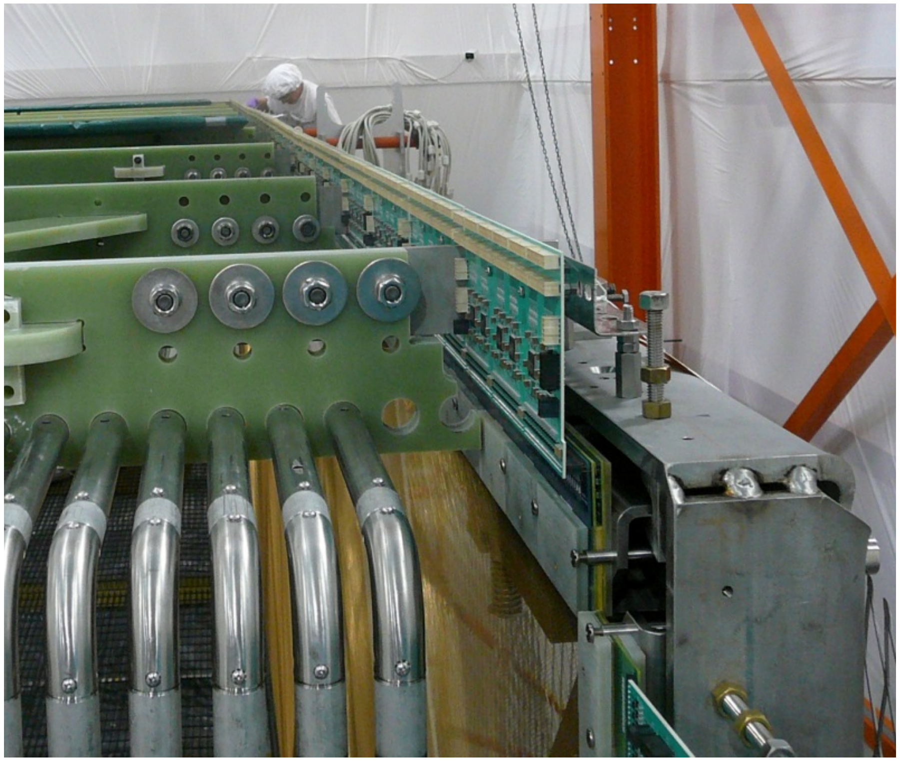


Service Board



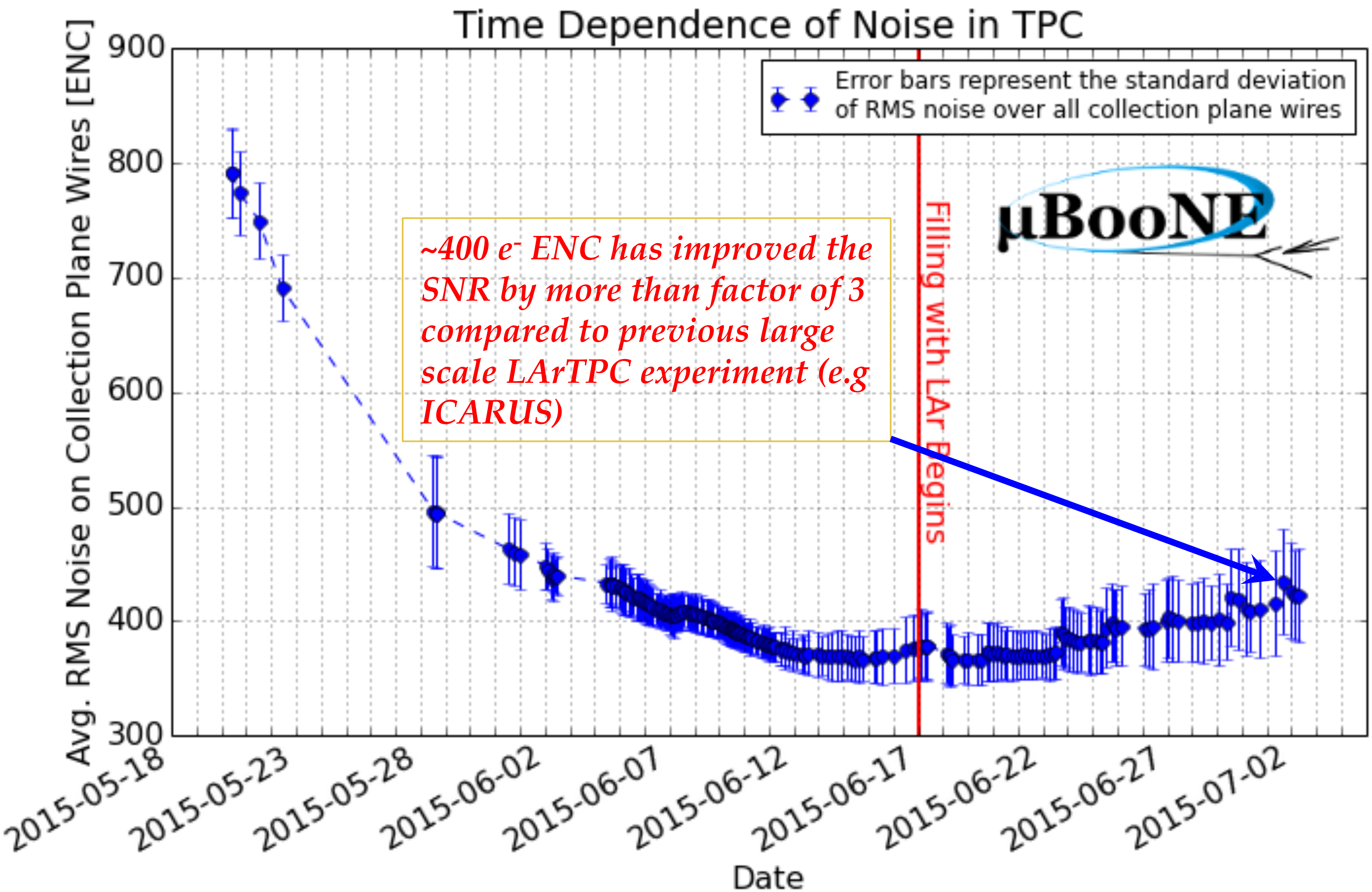
Signal Feed-through Assembly

MicroBooNE Front End Electronics



- **50 cold mother boards (8,256 channels)** were installed on MicroBooNE TPC in 2013, all channels tested successfully
- The full chain of front-end readout electronics was installed in cryostat and tested successfully in January 2014
- Detector was moved to experimental hall in June 2014

MicroBooNE Cold Electronics Temperature Dependence of Noise in TPC

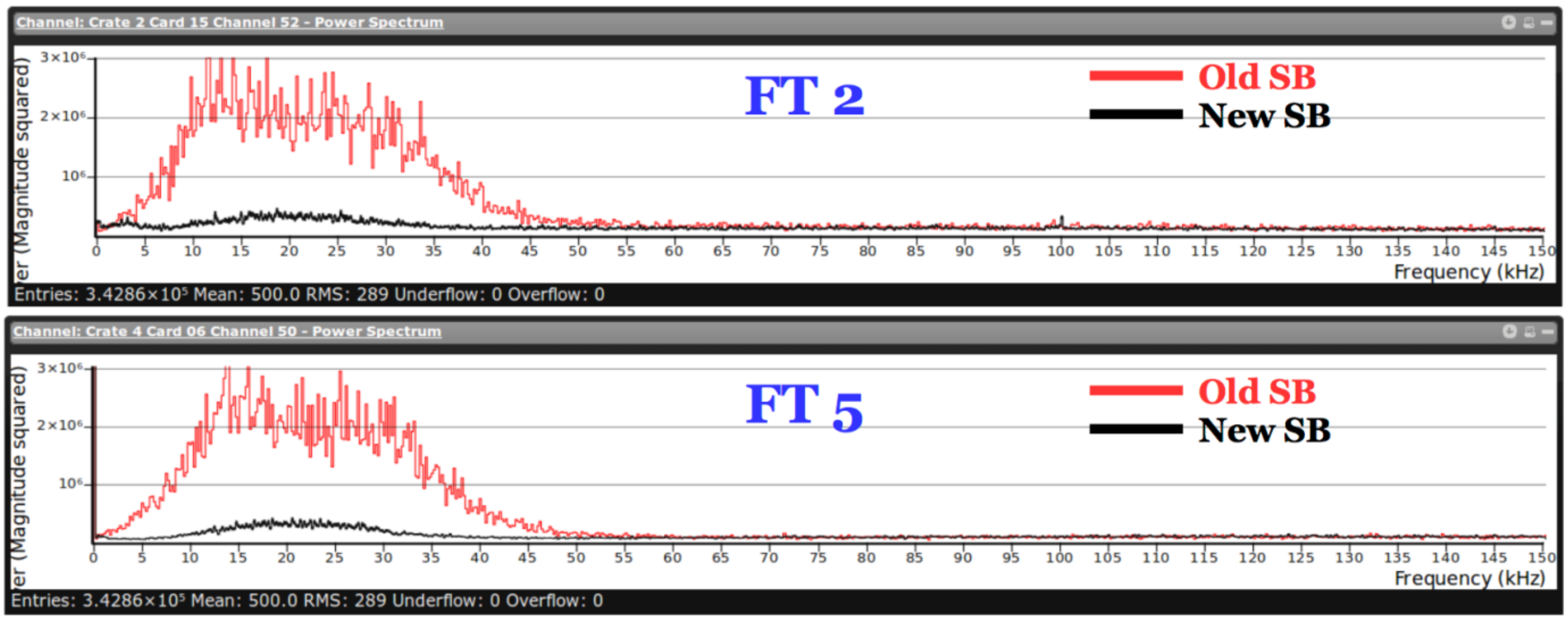


Inherent Input Transistor Noise and Excess Noise Sources

- **<u>Noise inherent to gain mechanism</u>** in the first transistor of FE ASIC
  - Expected ENC ~500 e^- at 1us t_p and 150pF C_d
- Latter stage noise (from intermediate amplifier and ADC) is negligible
- **<u>Excessive Noise Sources</u>**
  - Low frequency coherent noise from (warm) voltage regulator
  - Ripple from cathode HV power supply capacitively coupled from cathode to anode
  - Burst (aka "zig-zag") noise (slide 10)
- The first two excess sources exceeded the inherent noise
  - Initially they were removed by software filtering
  - Subsequently they were made very low-to-negligible by hardware filters
- For detailed discussion of MicroBooNE noise see publication, "Noise Characterization and Filtering in the MicroBooNE Liquid Argon TPC"
  - To be submitted to JINST soon

Low Frequency Noise from Voltage Regulator

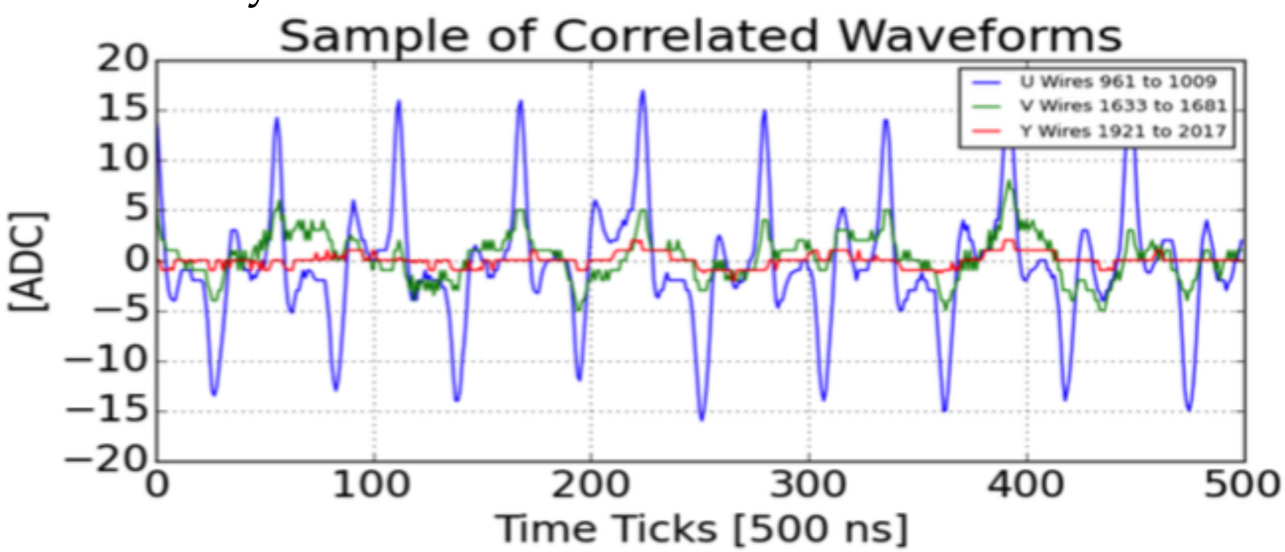
- Low frequency (10 - 30 kHz) coherent noise affecting groups of channels simultaneously
  - High correlation between channels on MB pairs (1 MB = 48U +48V + 96Y) on same service-board (SB) with low voltage regulator for ASICs
- New service boards with new voltage regulators to reduce this noise have been installed in summer 2016
- A correction waveform is constructed on a per sample basis and across sets of 48 contiguous channels to mitigate coherent noise



Frequency spectrum of new service board test on two signal feed-throughs

Cathode HV Power Supply Noise

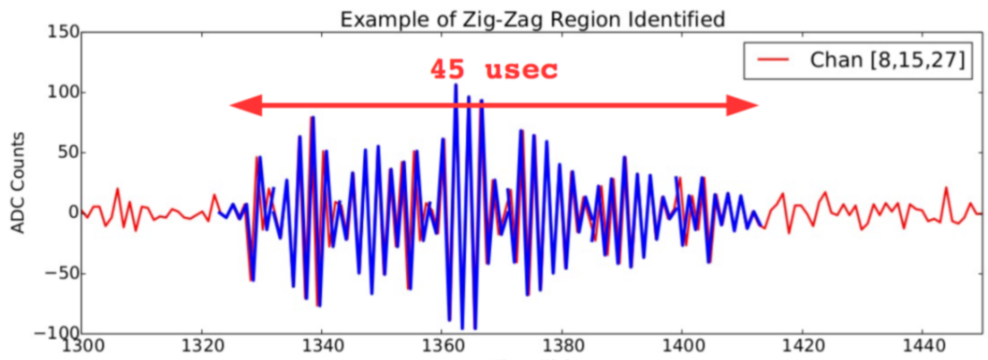
- Series of single frequencies (most prominent, 36kHz and 108kHz) were observed, odd harmonics of 36kHz, which is the fundamental freq. of HV power supply ripple
- Anode plane is sensitive to even small potential changes at cathode (which is 2.5m away). The induced current waveforms show decreasing amplitude in successive wire planes, as V-plane is shielded by U-wires & Y-plane is further shielded by V-wires:



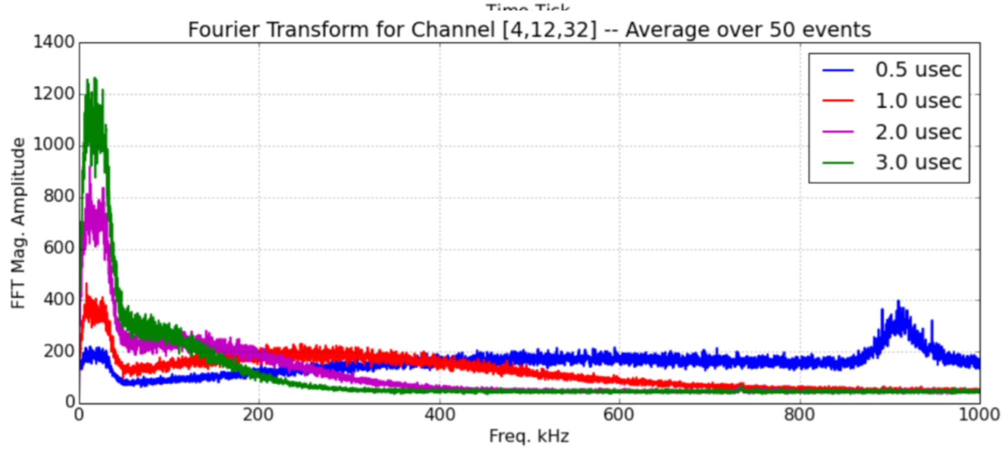
- This harmonic noise can be filtered out directly by masking discrete bins in the frequency domain. This became unnecessary after a second filter pot was installed in the HV system in 2016, which made this noise negligible.

900 kHz Burst Noise (aka Zig-Zag Noise)

- This high frequency noise is intermittent, and more prevalent on the downstream side of the TPC, where the services are located.
  - It can be clearly seen in the time domain, particularly with short peaking time
  - The source has not been conclusively identified
- No mitigation is necessary with nominal 2us peaking time
  - This noise can be easily filtered with low-pass offline filter for channels running at 1us peaking time



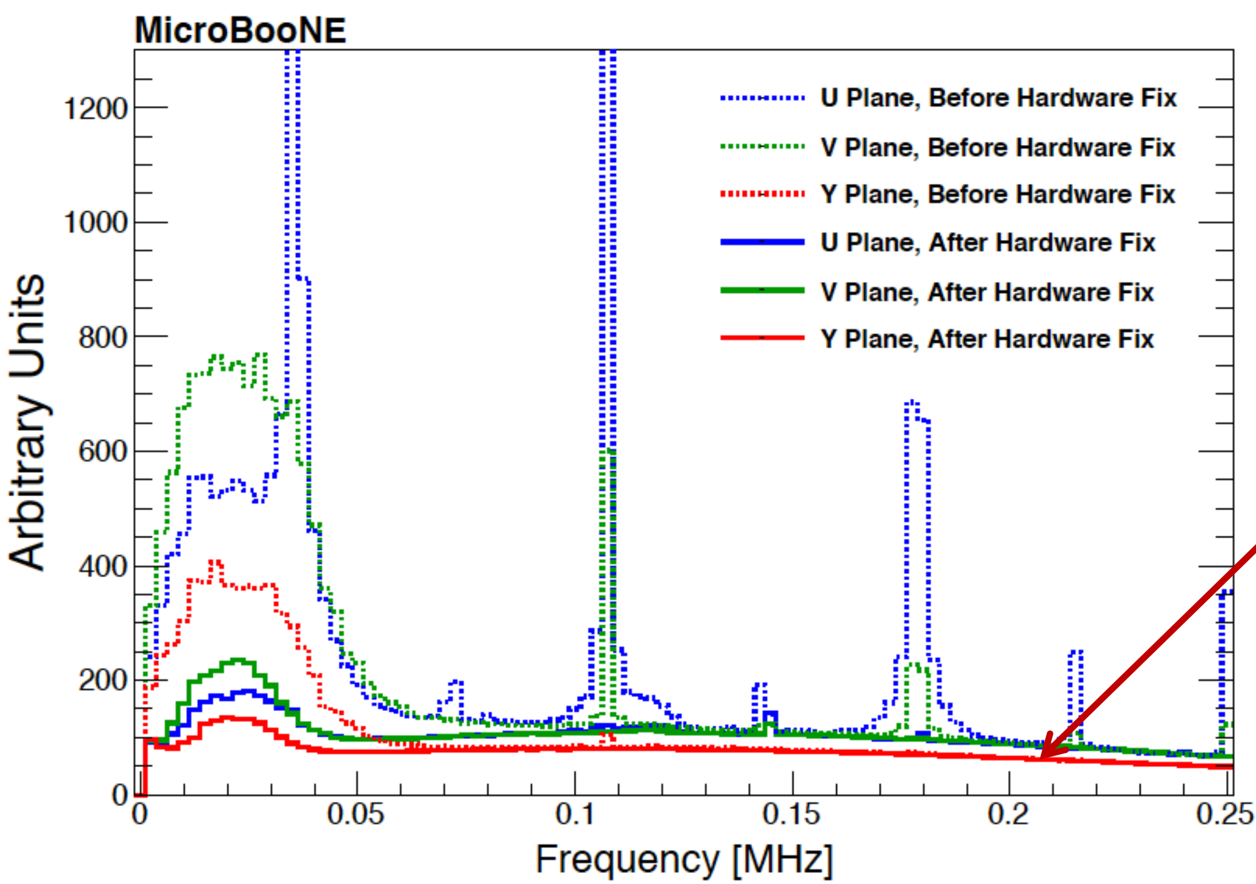
Time domain



Frequency domain

Performance after Hardware Upgrades

- Hardware upgrade has been implemented to mitigate noise from HV power supply and low voltage regulator in 2016
  - A second filter pot was installed in the drift HV system
  - New service boards with new voltage regulator were installed



Y-plane after hardware upgrade

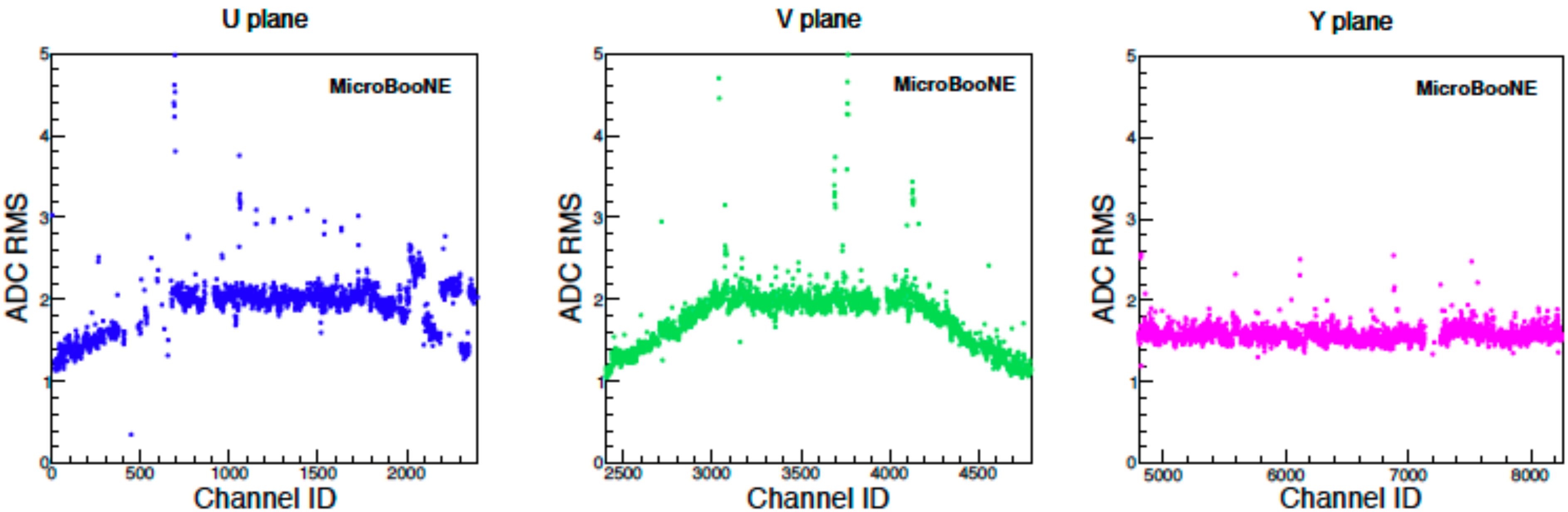
Non-functioning Channels

- There are some channels from FT's 7-9 with uniformly higher noise (x20), confirmed to be coming from touching wires (V touching U & Y → FE ASIC inputs in contact with each other)
  - These channels can't be used and can be identified using high RMS cut to filter out from the data analysis
- There are ~4% non-functioning channels due to FE ASIC start-up issue
  - These non-functioning channels can be filtered out using very low RMS cut and can be clearly identified using pulser data
- A small number of channels (~20) shows saturation of the FE ASIC due to wire motion with proper bias setting of 500pA. This number is much larger if the bias current is very low (100pA)

Table 1. Summary of the non-functioning channels for Run 3455 Event 6. A total of ~862 channels are considered non-functioning. MB stands for front-end motherboard.

# non-functioning channels	Reason
~20	ASIC saturation
96	6 ASICS on one MB not connected to wires
304	19 ASICs due to start-up problem
126	channels sorrounding U-Y shorted wires with 10 noisy channels
287	channels sorrounding U-V shorted wires with 28 noisy channels
36	noisy channels not located near the shorted wires

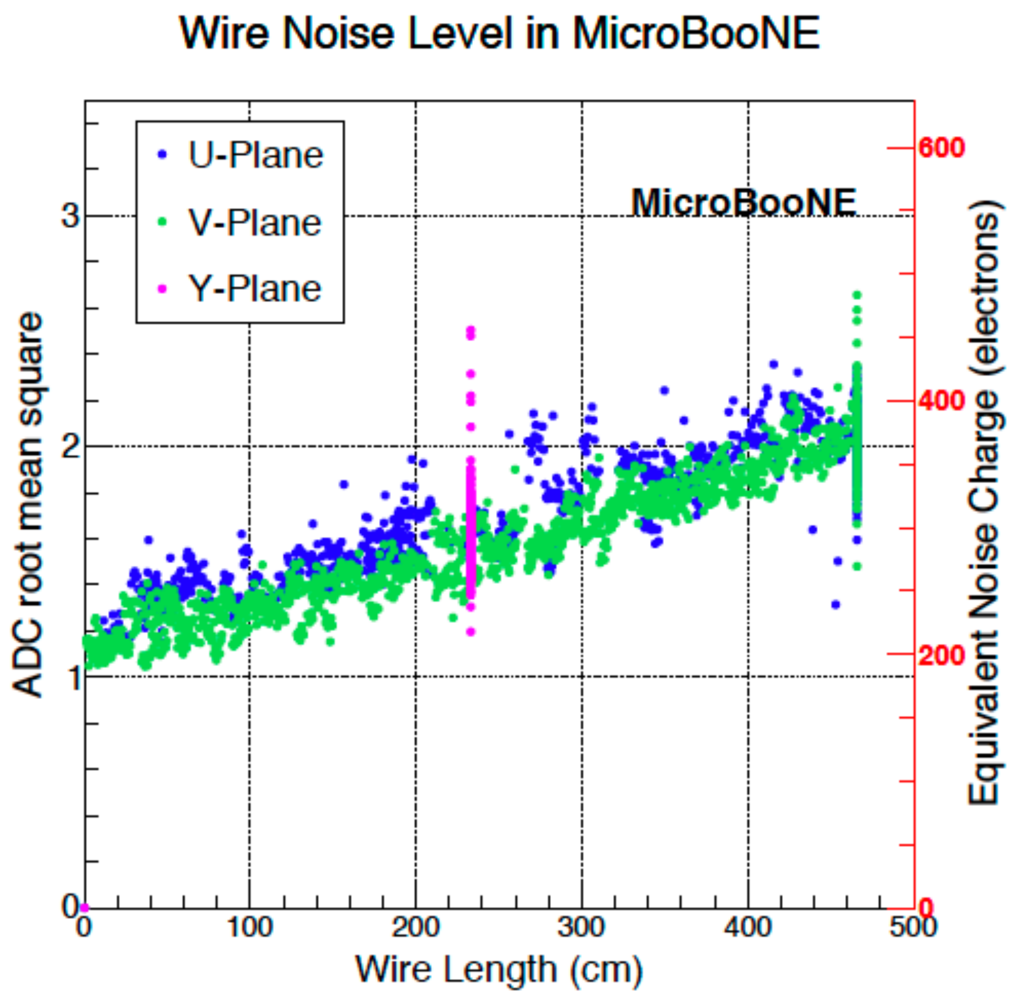
Residual Noise Level



The noise level in terms of ADC is converted to the equivalent noise charge (ENC) as follows:

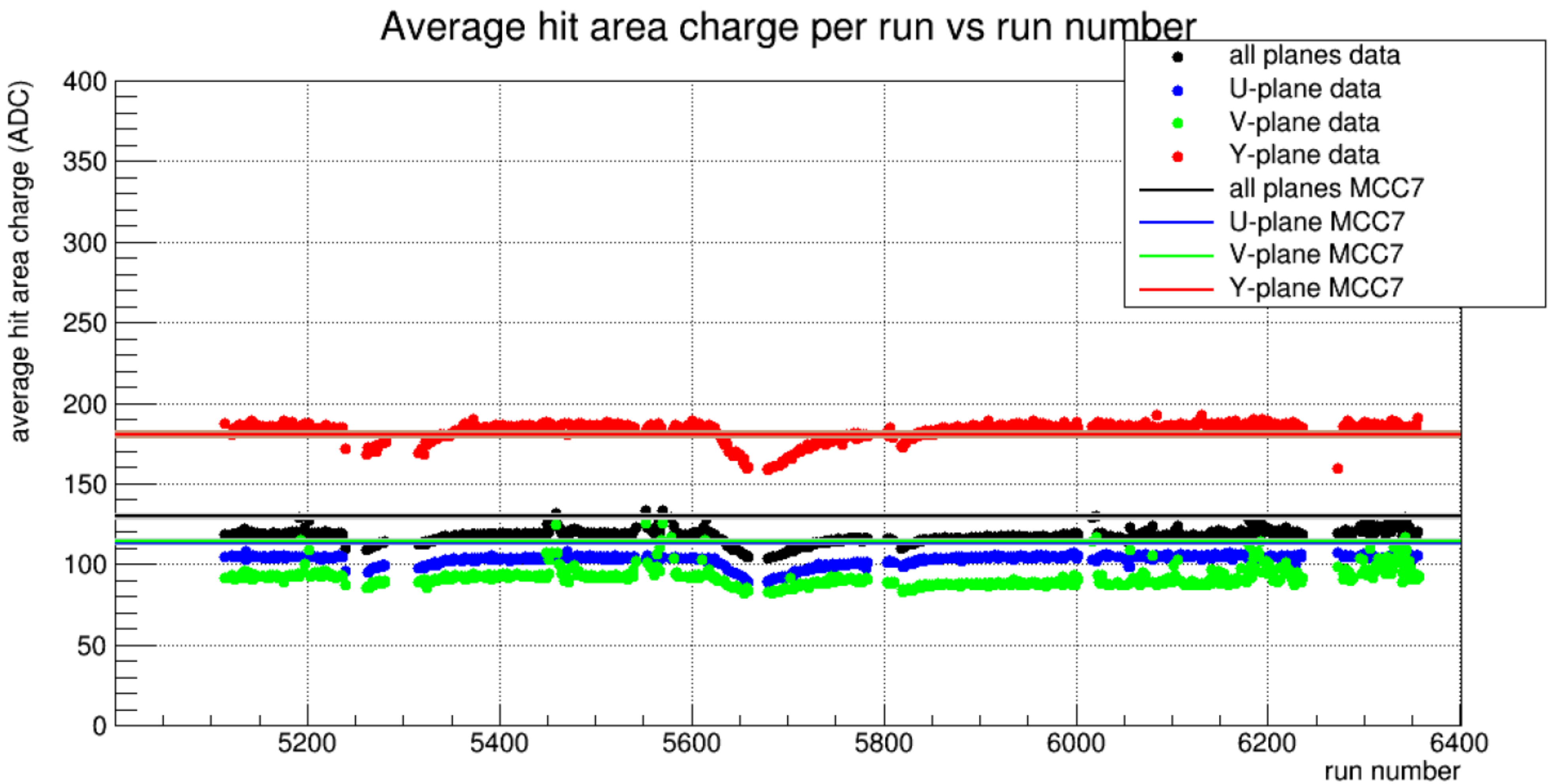
$$\frac{ENC}{ADC} = \frac{2000\ \mathrm{mV}}{4096\ \mathrm{ADC}} \times \frac{1\ \mathrm{fC}}{14\ \mathrm{mV}} \times \frac{1}{1.2} \times \frac{6241\ e^-}{\mathrm{fC}} = 182\ \frac{e^-}{ADC}. \tag{6.1}$$

TPC Noise vs. Wire Length



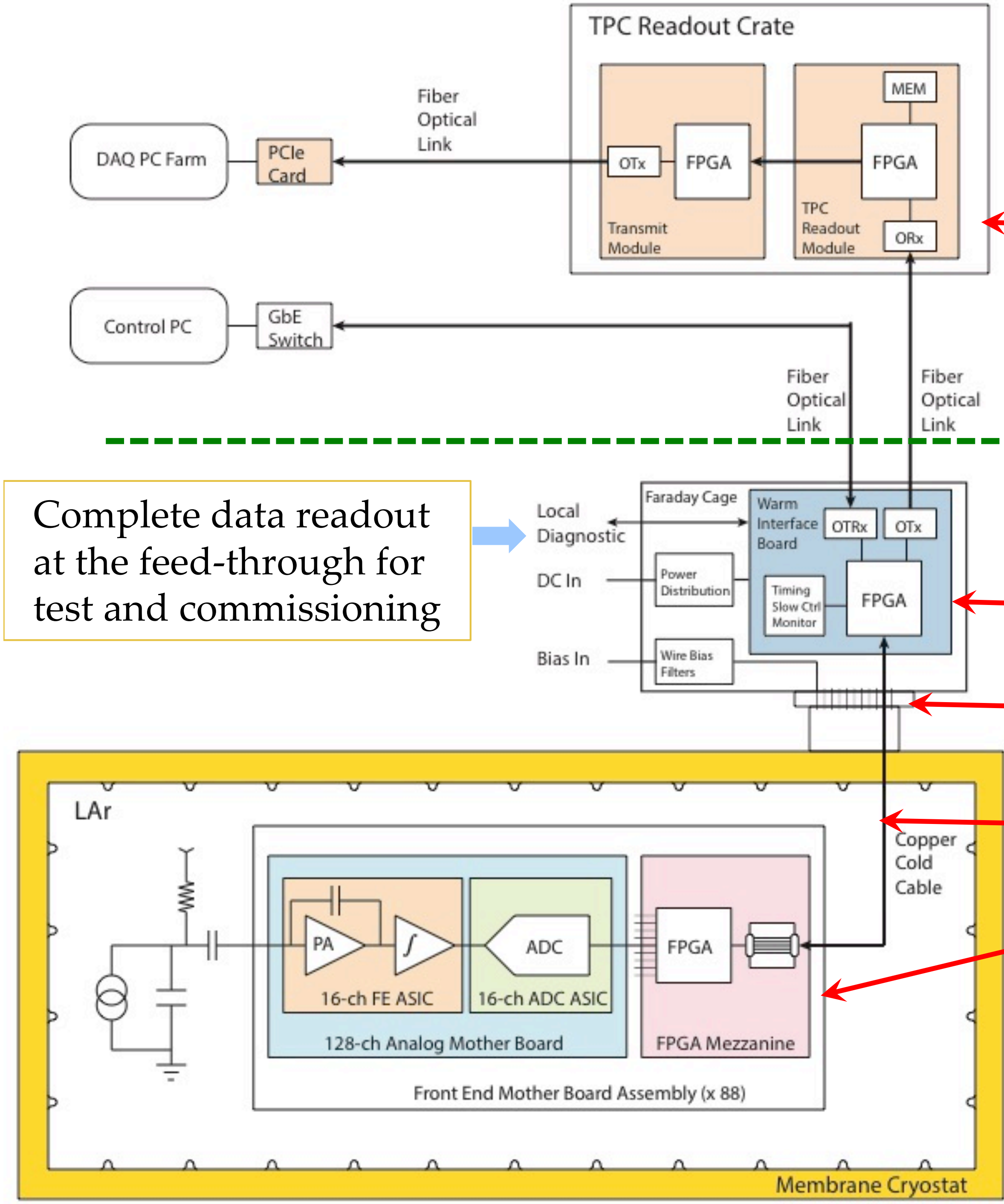
- ENC after noise filtering is < 400 electrons for 85% of channels, in agreement with the bench tests of FE ASIC
- Measured efficiency requiring two wire planes with real location of dead channels is about 97%

MB Long Term Stability: Average Hit Area Charge, incl. Argon Purity Variations



- MICROBOONE-NOTE-1013-INT

SBND TPC Electronics



Complete data readout at the feed-through for test and commissioning

TPC Readout Electronics

Back End Electronics

Front End Electronics

Warm Interface Electronics: crate with 28 boards

Signal Feed-through (4 sets)

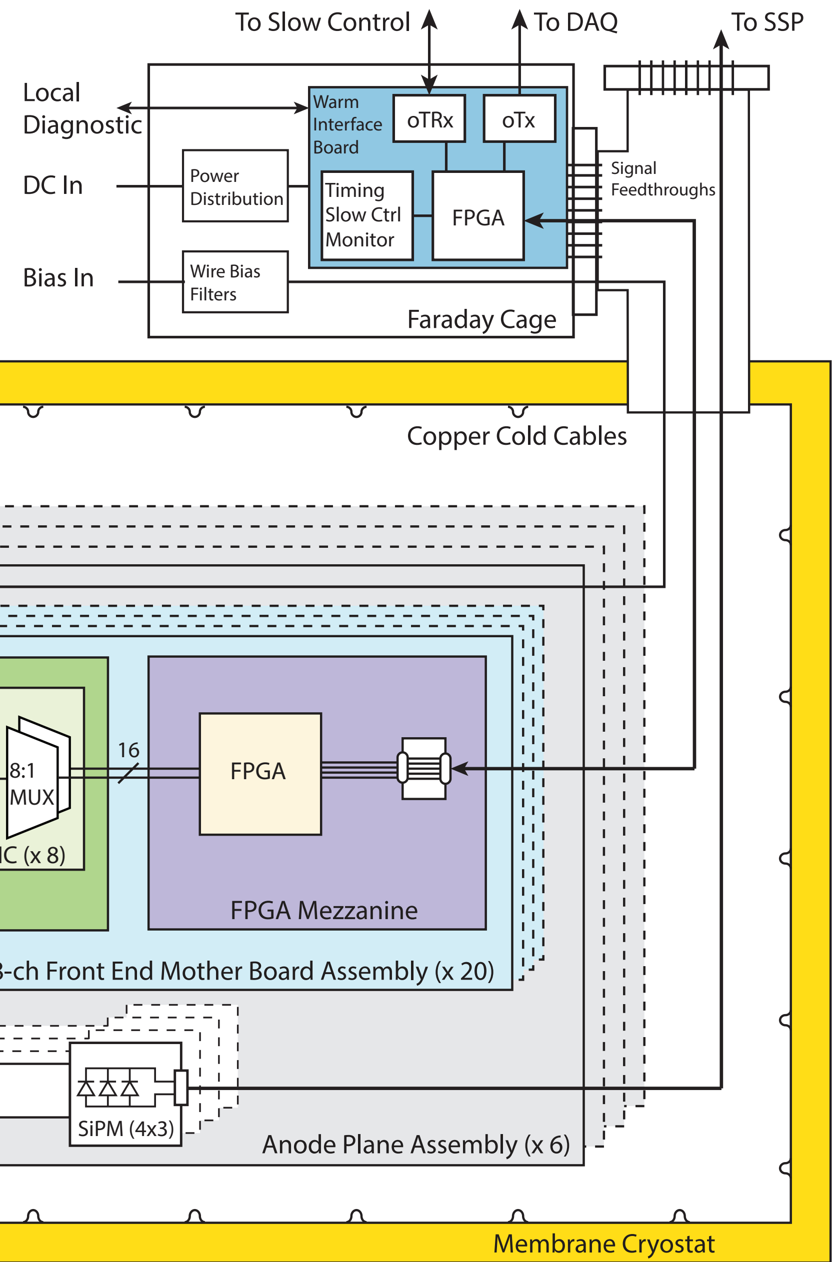
Cold Cable (4 bundles)

Cold Electronics:

- ***704 FE ASICs/704 ADC ASICs/88 Cold FPGAs***
- ***88 Front End Mother Board assemblies***

ProtoDUNE-SP TPC Readout Electronics

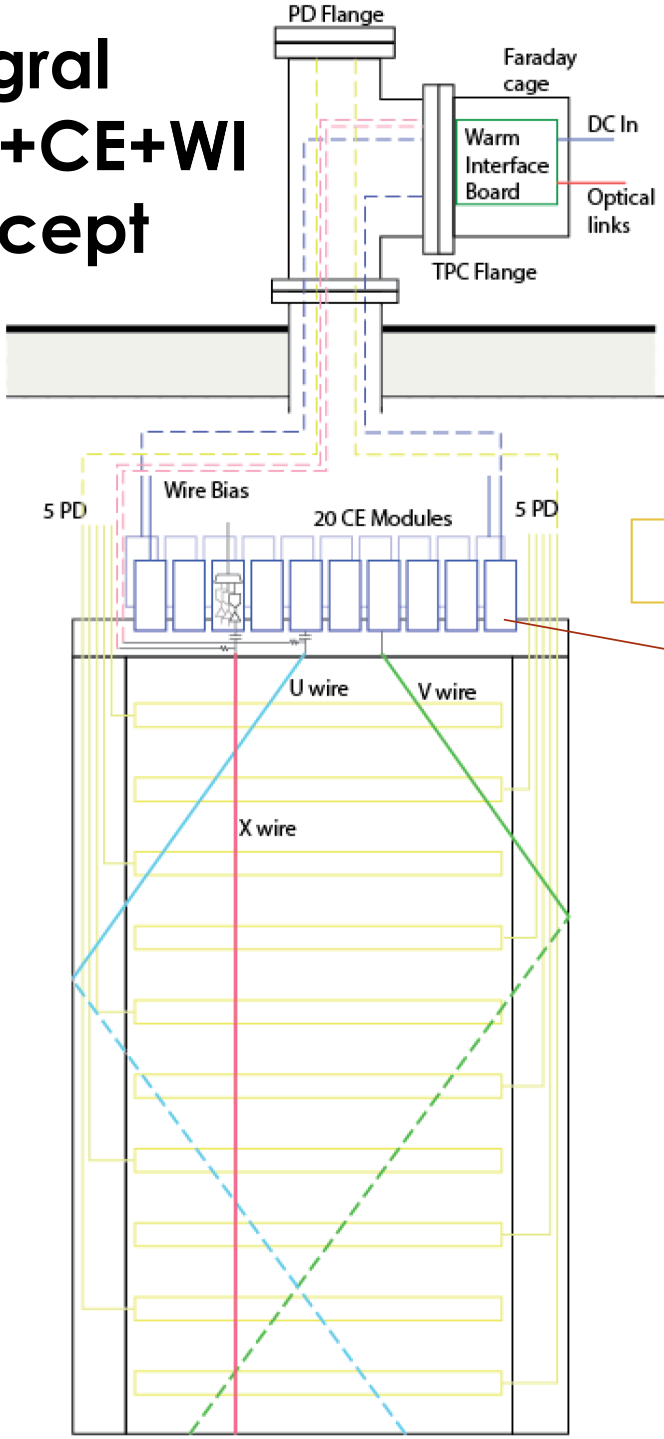
- ***Front End Electronics System***
  - ***960 FE ASICs/960 ADC ASICs/120 Cold FPGAs***
  - ***120 Front End Mother Board assemblies***
  - ***6 sets of cold cable bundles, 6 sets of signal feed-throughs***
  - ***~36 boards in warm interface electronics crate***

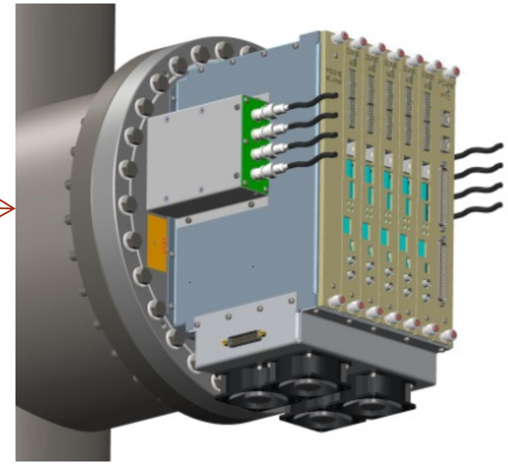


SBND and ProtoDUNE-SP Electronics System

- SBND and ProtoDUNE-SP share many common development of front end readout electronics
  - SBND: 11,264 channels vs. ProtoDUNE-SP: 15,360 channels
  - Shared development of Cold FE ASIC and ADC ASIC
  - The functionality of the FEMB (Front End Mother Board) will be the same
    - Small differences in layout are required due to the wire spacing differences and readouts in the two detectors
    - FPGA mezzanine has minor difference on connectors due to the choice of cold cable
  - The feed-throughs are similar from an electrical connection point of view, but different in cold cable interface
  - The Warm Interface Electronics is similar with small differences in the way the timing protocols are handled.
- Both systems have been following the ***integral design*** concept, APA + cold electronics + warm interface

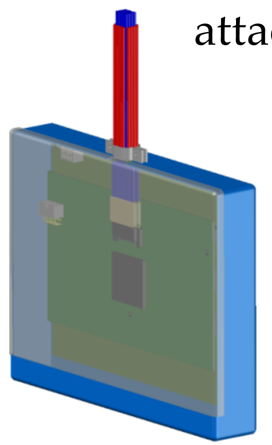
Integral APA+CE+WI Concept

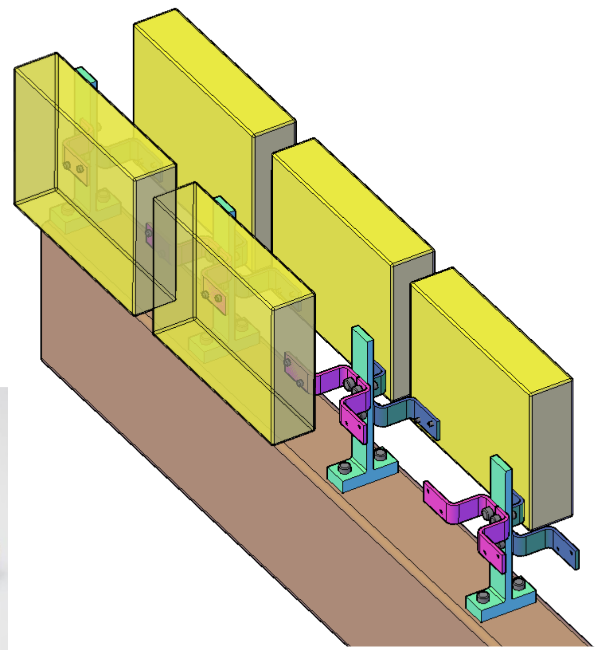




ProtoDUNE-SP

Cold electronics module and its attachment to the APA frame

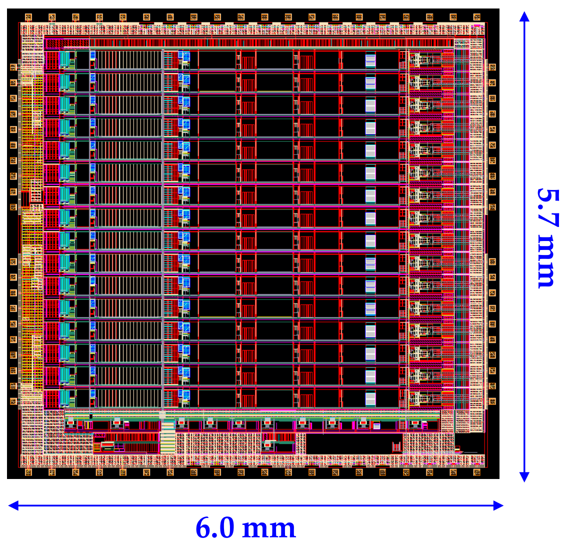




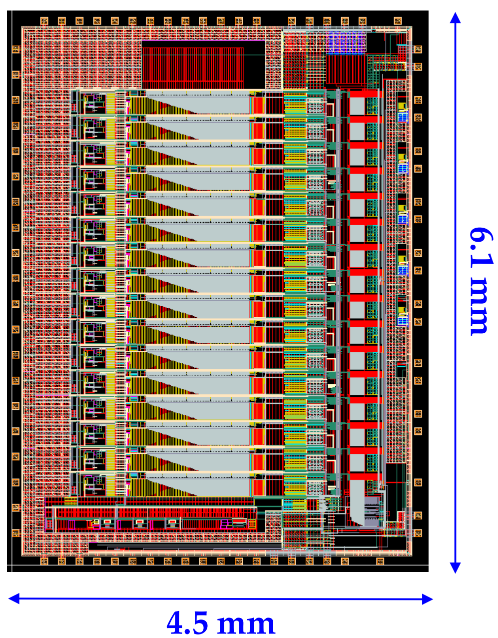
SBND/ProtoDUNE-SP Electronics Status

- SBND is working on the preliminary design of front-end electronics system
  - Prototype electronics boards are available for lab test and integration test
  - A cold ADC committee chaired by Mike Shaevitz is to advise the development of cold readout electronics
    - Explore different options, including commercial ADC in cold, dual gain configuration with ASIC ADC etc.
    - Conclusion is expected in summer 2017
- ProtoDUNE-SP is working on the production of front-end electronics system
  - PRR in April 3rd for mechanical parts and May 3rd for electrical parts of cold electronics system
  - DUNE has a cold electronics task force chaired by Dave Christian to advise the development of cold readout electronics
    - Explore different options of cold ASIC development for DUNE far detector
    - An interim report will be presented tomorrow in DUNE collaboration meeting

CMOS Cold ASICs Upgrades Implemented

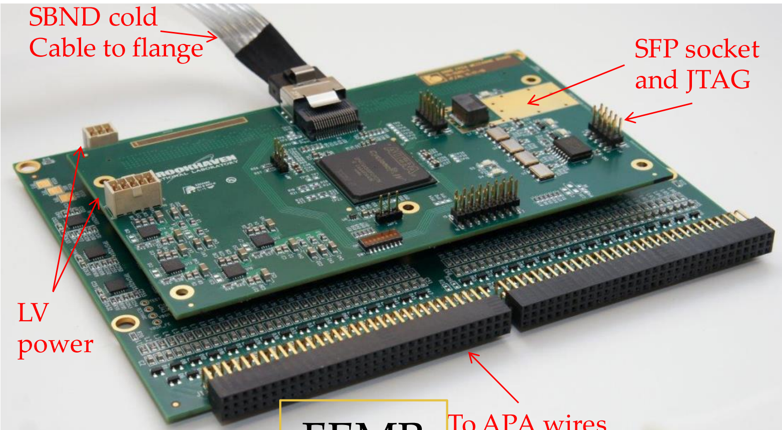


- FE ASIC
  - Built-in 6-bit DAC for calibration pulse generation
  - Built-in analog monitoring output for debug
  - Address pole-zero cancellation and drive capability in buffer-off mode
  - Add higher bias current (1nA and 5nA) options and smart reset
  - Revise BGR start-up circuit and increase ESD protection on I/O

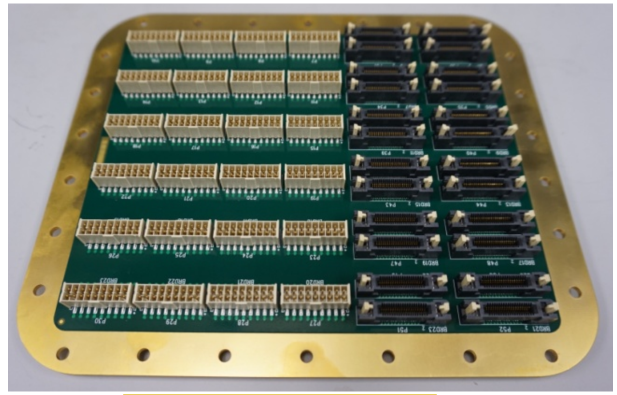


- ADC ASIC
  - Implement COLDATA compatible interface and FE ASIC compatible configuration
  - Address the early saturation and roll-back
  - Implement power-on default configuration and extend soft-control functions
  - Revise BGR start-up circuit and increase ESD protection on I/O
  - Improve ADC INL/DNL → <u>not completely resolved</u>

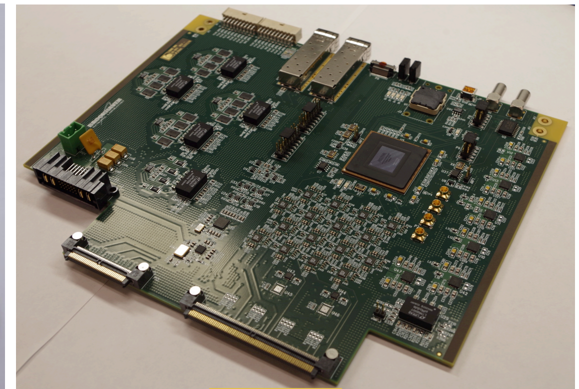
SBND/ProtoDUNE-SP Front End Electronics



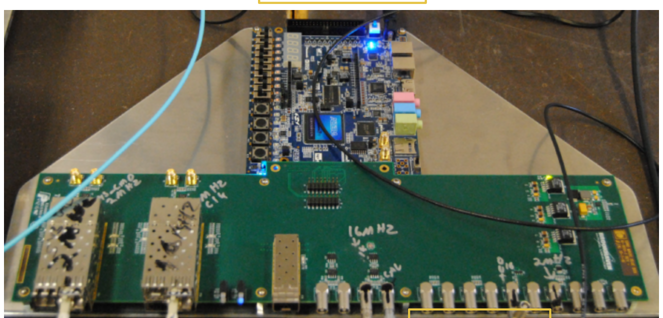
FEMB



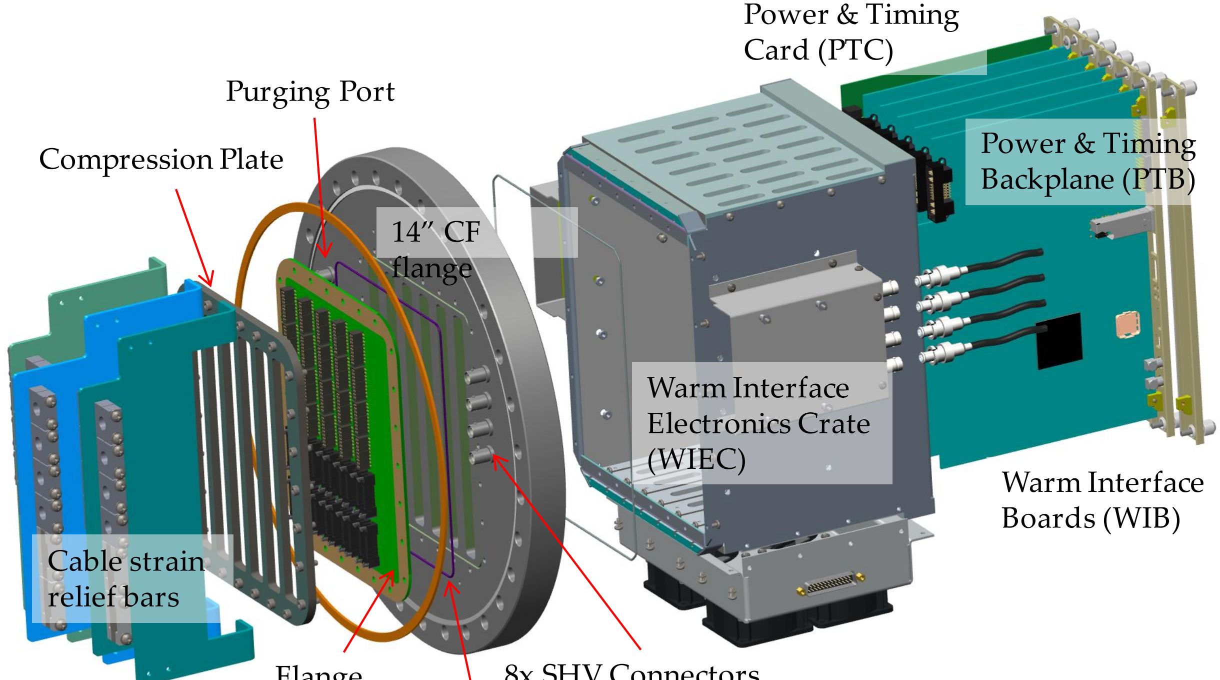
Flange Board

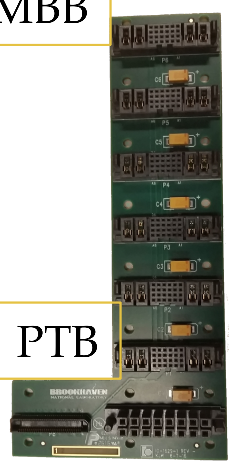


WIB



MBB



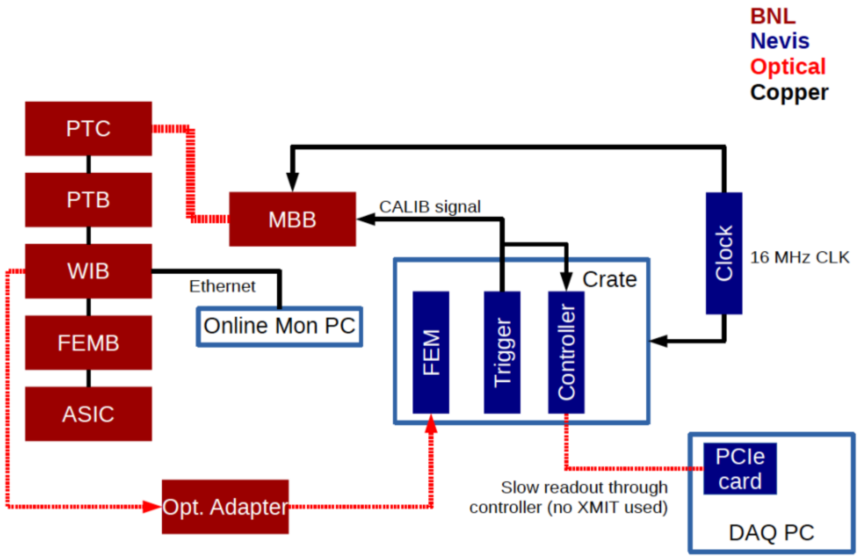


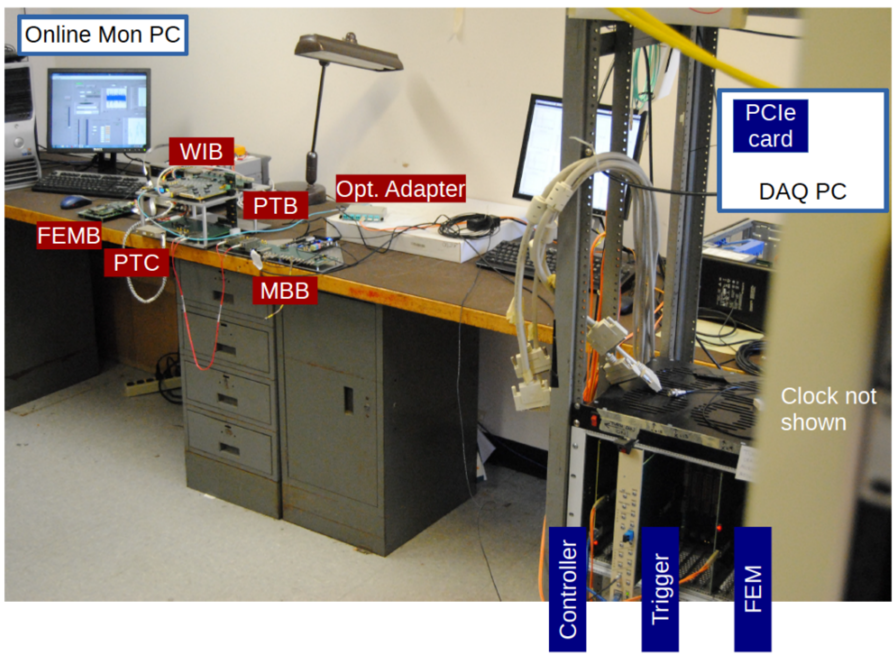
PTB

Signal Feedthrough+WI Assembly

Cold Cable

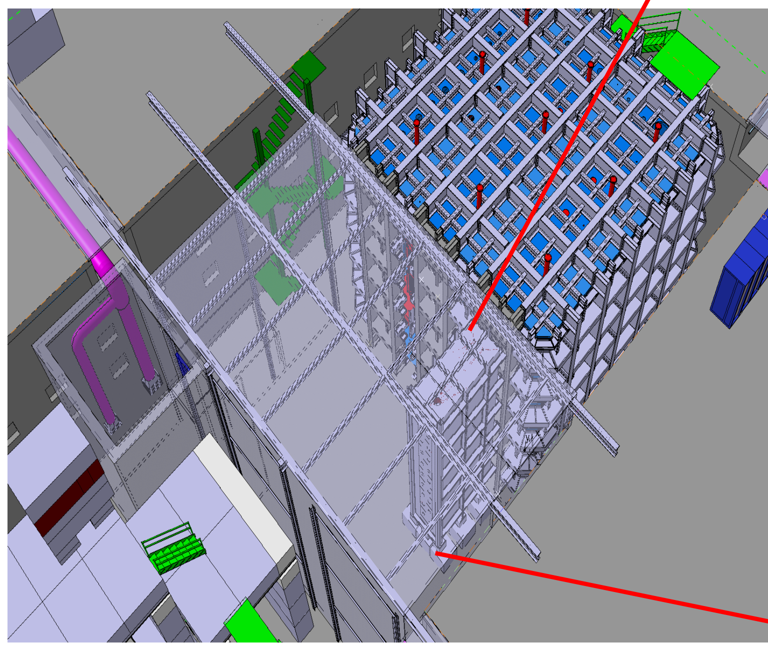
SBND Integration Test

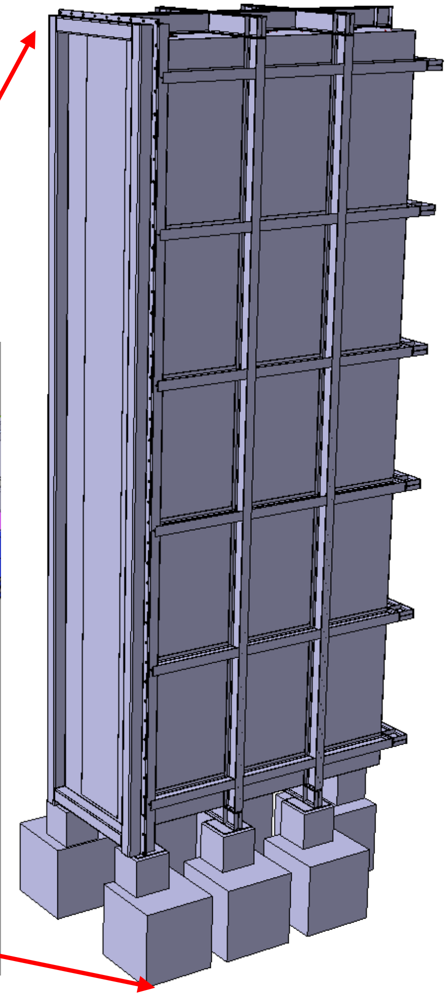




- Two successful integration tests have been carried out
- First integration test of SBND full readout chain took place at Nevis labs on Sept 22nd
  - Successful data flow from FEMB → WIB → FEM → Ctrl → DAQ PC
  - Stable optical link was established between WIB and FEM
  - Calibration data was acquired and displayed on DAQ PC successfully
- Second integration test of SBND full readout chain took place at Nevis labs on Nov 18th
  - Synchronous readout from FEMB → WIB → FEM → Ctrl → DAQ PC has been established
  - Timing distribution Clock/Calib → MBB → PTC → PTB → WIB → FEMB has been exercised successfully

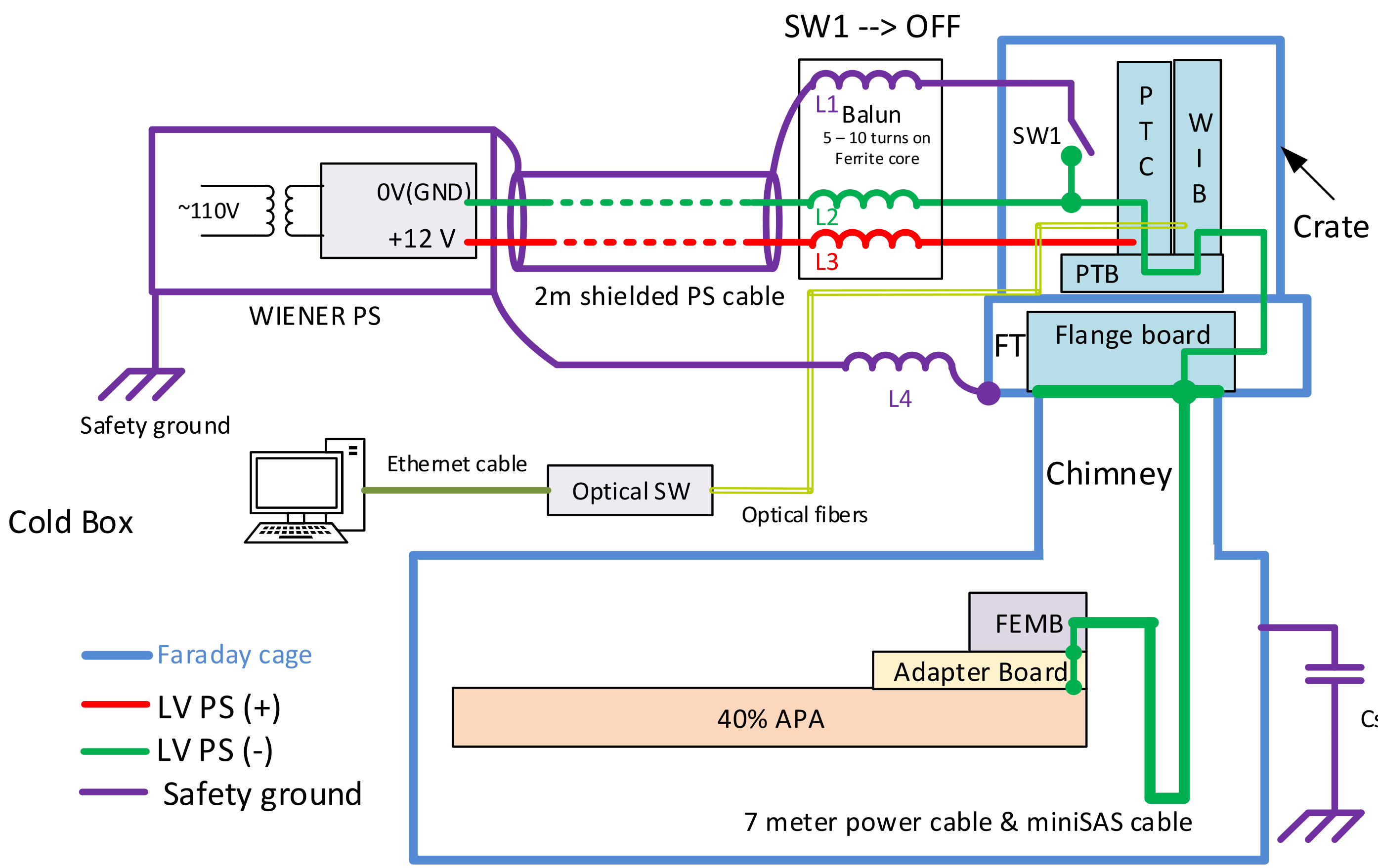
Integration Test Stand





- Fermilab
  - RF shielded room with isolation transformer
- CERN
  - Cold box to house ProtoDUNE-SP APA and readout electronics
  - Full electronics chain test at LN2 temperature

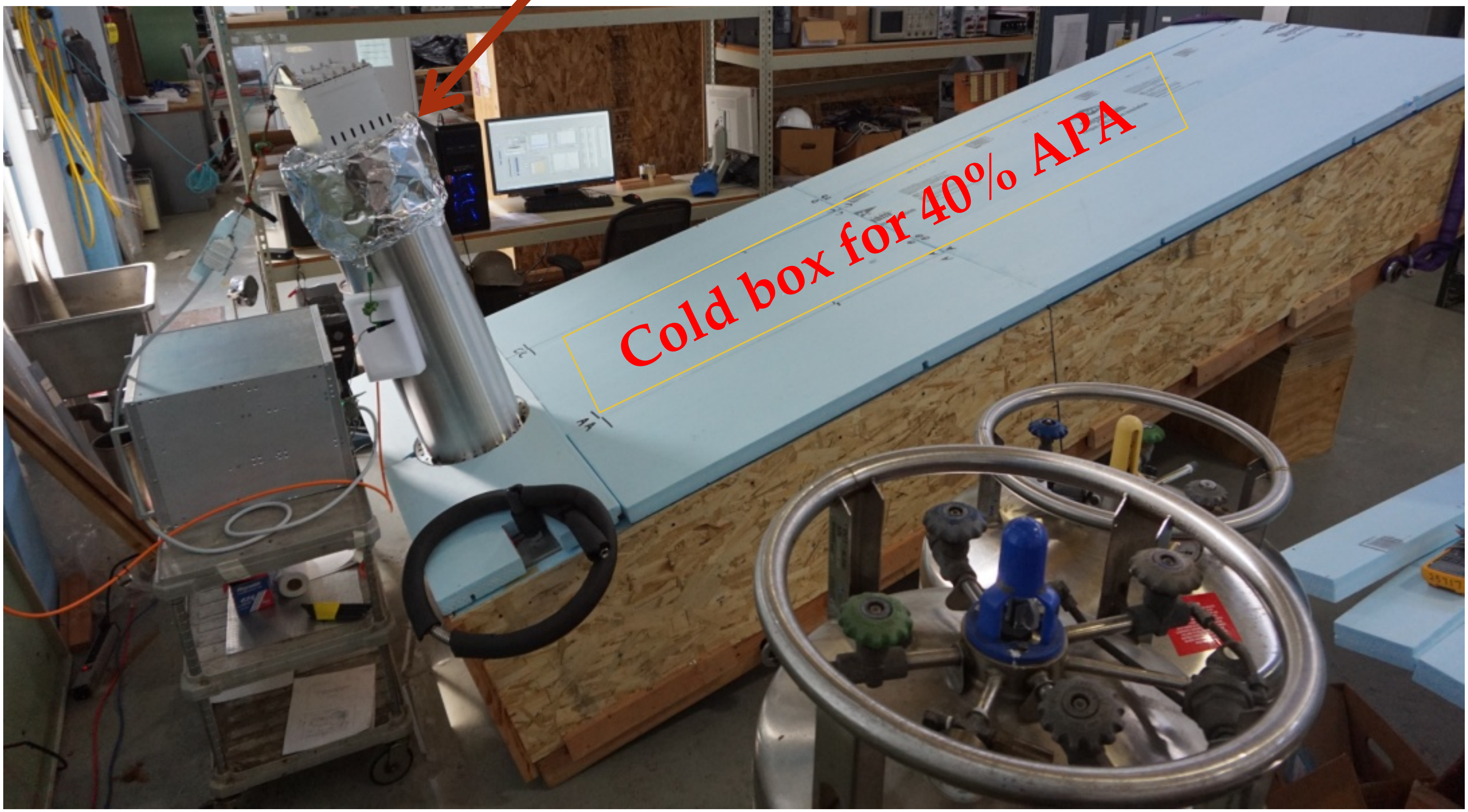
BNL Cold Integration Test Stand



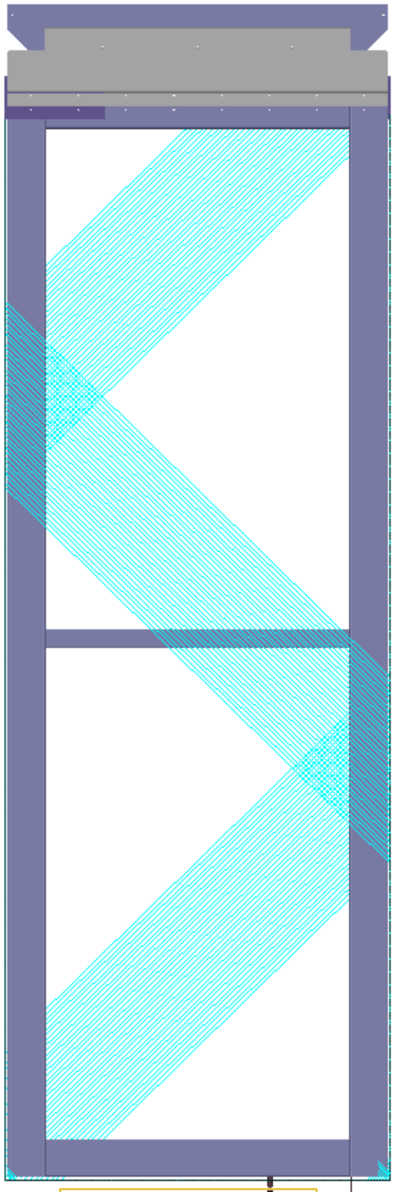
- Full electronics chain test at LN2 temperature
- Following grounding and isolation rules for ProtoDUNE-SP

BNL Cold Integration Test Stand

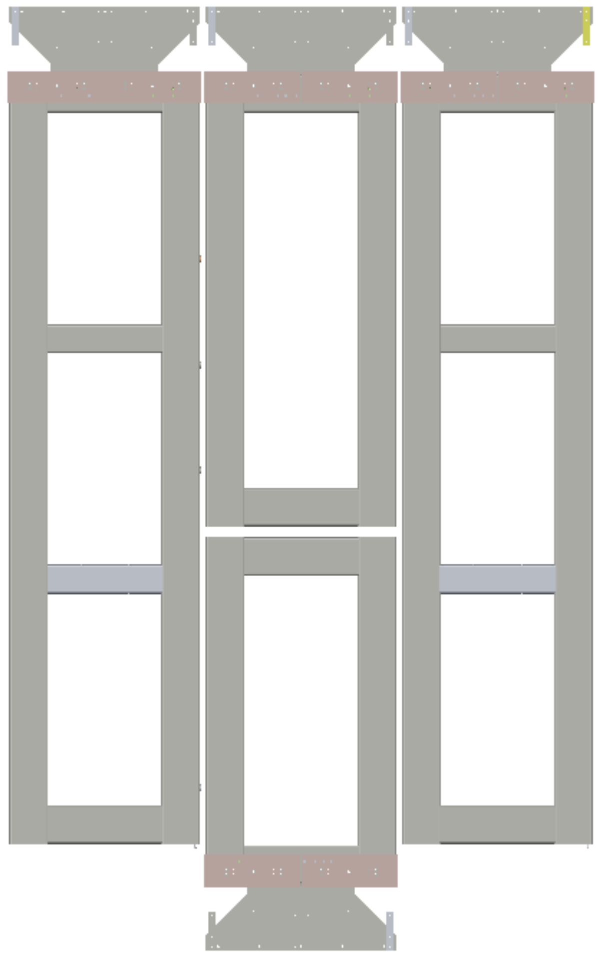
Feed-through+WIB



APA Size Comparison



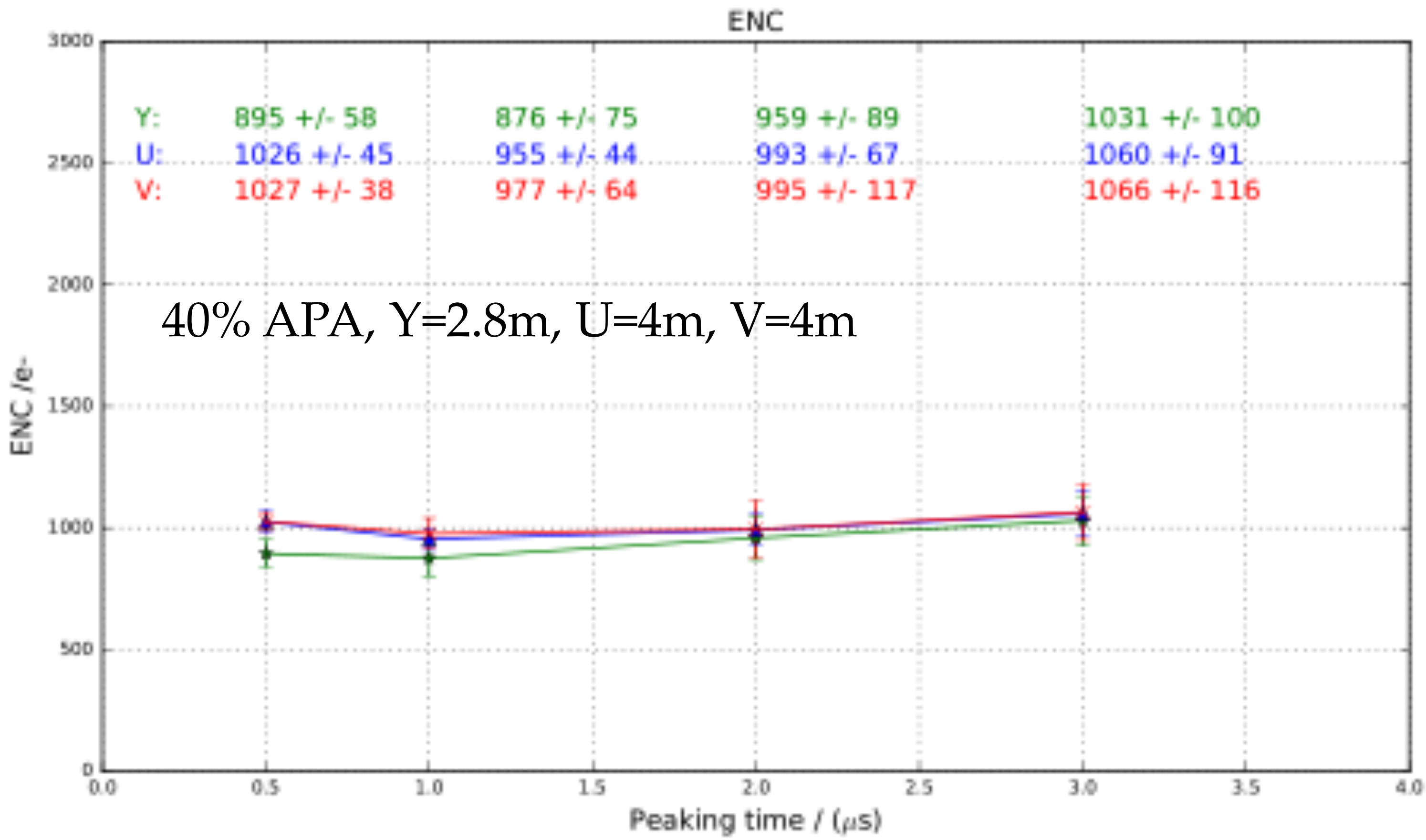
40% APA



35ton APA

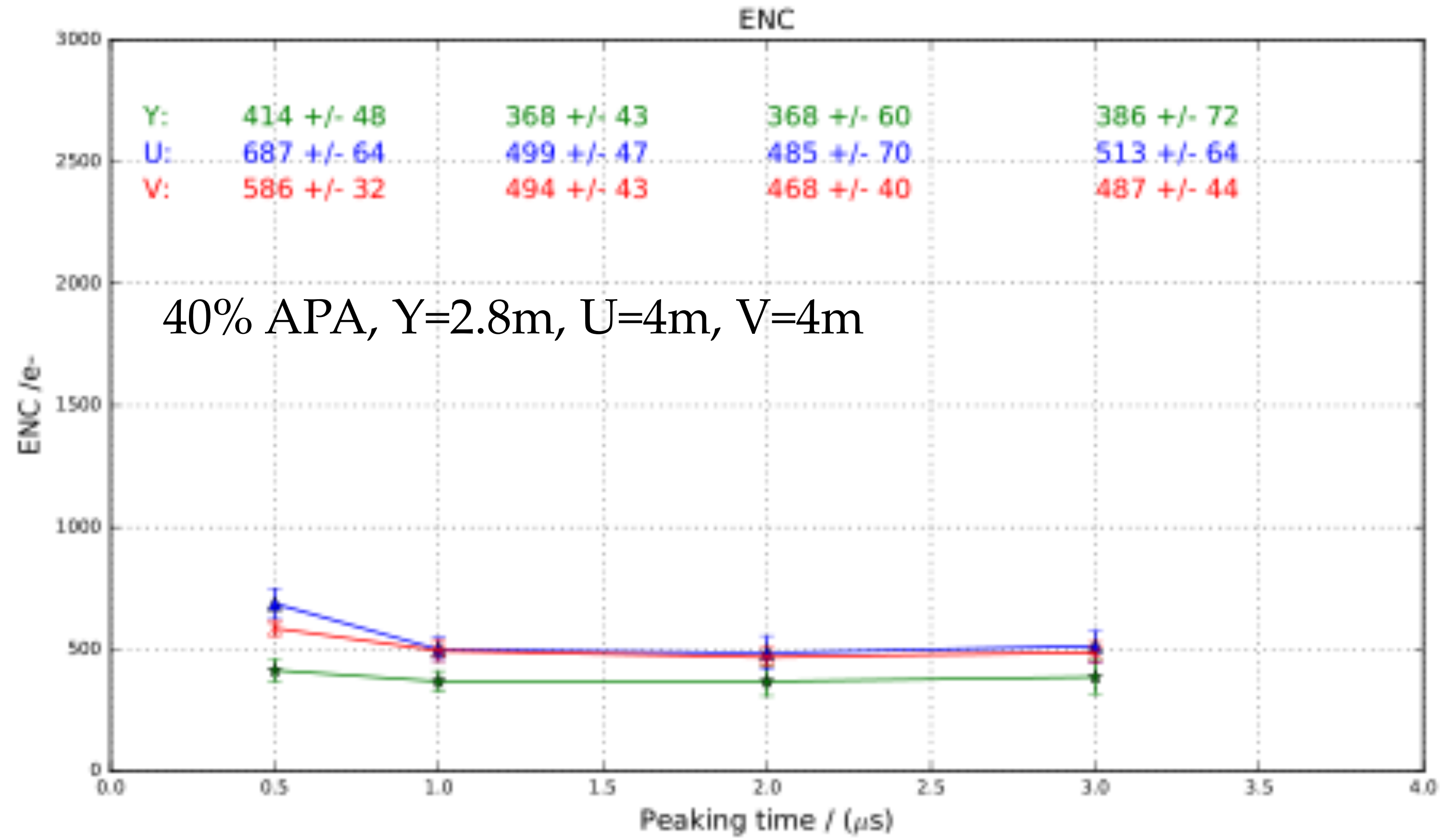
- DUNE APA
  - 6m x 2.3m
- **40% APA~**
  - 2.8m x 1.0m ~ $\mathbf{2.8m^2}$
  - 40% of original LBNE APA of 7m x 2.5m
  - ~45% of DUNE APA
- **35ton** has 3 sizes of APA
  - 2m x 0.5m
  - 1.2m x 0.5m ~ $\mathbf{3m^2}$
  - 0.8m x 0.5m
- SBND APA
  - 4m x 2.5m

40% APA at RT: Preliminary Test Results



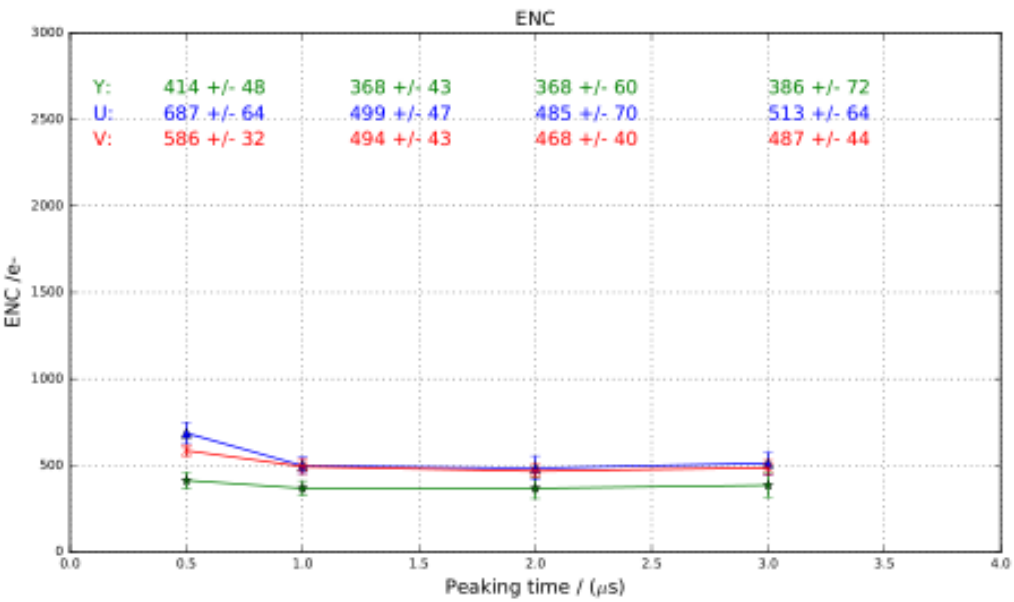
- Integration test at BNL is ongoing, more tests will be carried out in coming weeks
  - Preliminary test results are promising
- ENC at Room Temperature
  - Collection plane is ~880 e^- and induction plane ~980 e^- at 1us peaking time

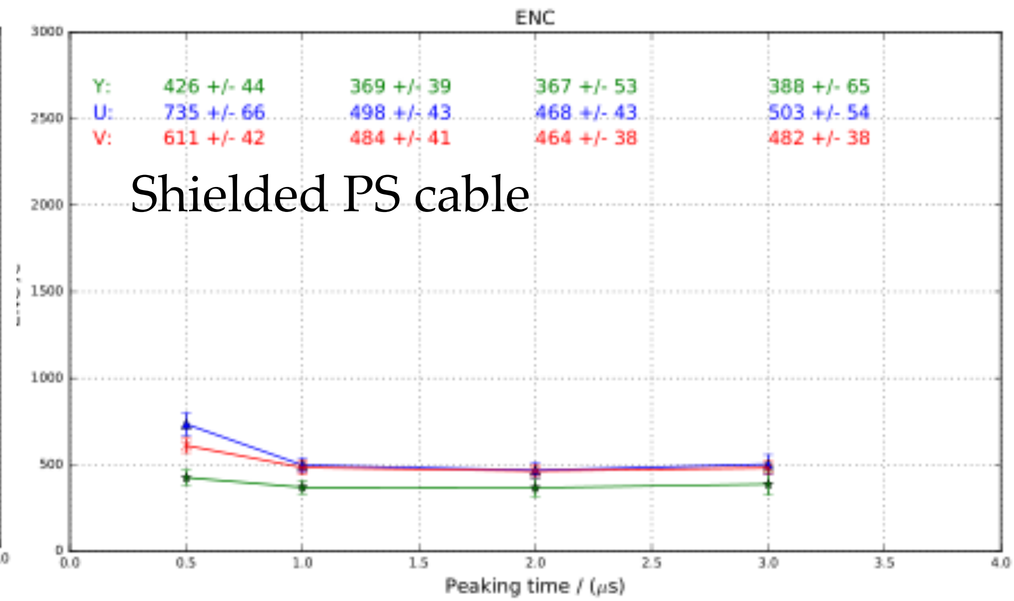
40% APA in LN2: Preliminary Test Results



- Integration test at BNL is ongoing, more tests will be carried out in coming weeks
  - Preliminary test results are promising
- ENC at LN2 Temperature
  - Collection plane is ~370 e^- and induction plane ~500 e^- at 1us peaking time

40% APA in LN2: Preliminary Test Results
Power Cable Shielding Test





- Test different power cable configurations, shielded and unshielded
  - No obvious difference is identified
- This is consistent with what is described in the literature
  - S. Shenfeld, “Magnetic Fields of Twisted-Wire Pairs”, IEEE Transactions on EMC, Vol. EMC-11, No. 4, Nov 1969
  - Magnetic field will be attenuated by ~100dB with distance of 10cm from the twisted-wire pair
- Plan to proceed with unshielded power cable for ProtoDUNE-SP

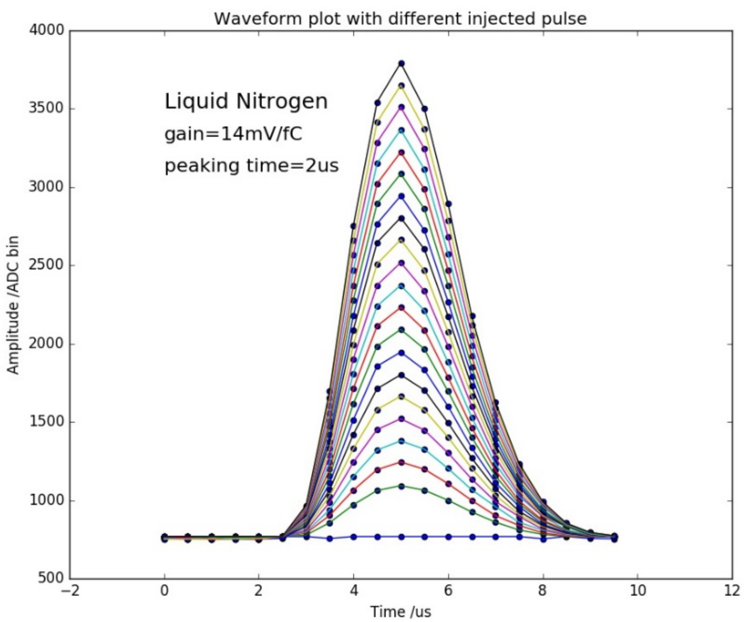
Summary

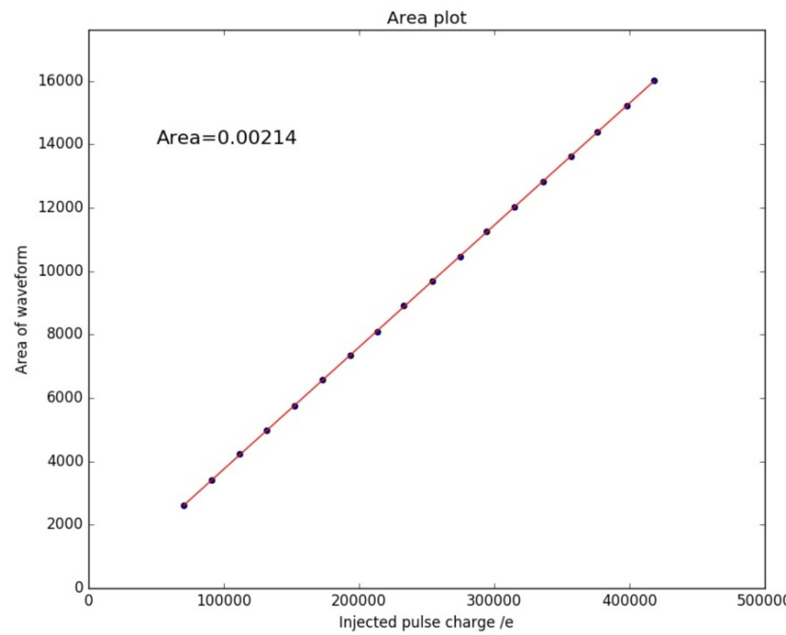
- MicroBooNE is the first running experiment instrumented with CMOS cold electronics
  - The readout electronics is designed as an **integral system**, with TPC, signal feed-through and warm interface electronics
  - Excellent noise performance (~400e$^-$), as for the FE ASIC on the bench, has been achieved after understanding and addressing several excess noise sources
- Full cold readout chain with CMOS ASICs and FPGA will be used to instrument the SBND and ProtoDUNE-SP LAr TPCs
  - A necessary (but not sufficient!) condition to achieve a good performance: **An integral design concept** of **APA+CE+Feed-through**, and **Warm Interface Electronics** with **local diagnostics** and strict isolation and **grounding rules** will have to be followed. The design of the feed-through with WIB in a Faraday Cage is essential.
  - Different integration tests at BNL, Fermilab and CERN are being used to characterize the system performance with APA.

Backup Slides

FE + ADC ASIC Evaluation for ProtoDUNE-SP

- P2 FE + P1 ADC Test
  - **<u>Peak and area(charge)</u>** linearity test of P2 FE and P1 ADC in LN2
  - Same FE channel is used to test 16 ADC channels
  - Both peak and area measurements show reasonable non-linearity (< 0.5%)
  - FE 14mV/fC, 2us t_p + ADC 2Msps
    - Peak INL: 0.274+/- 0.050%
    - Area INL: 0.254 +/- 0.070%



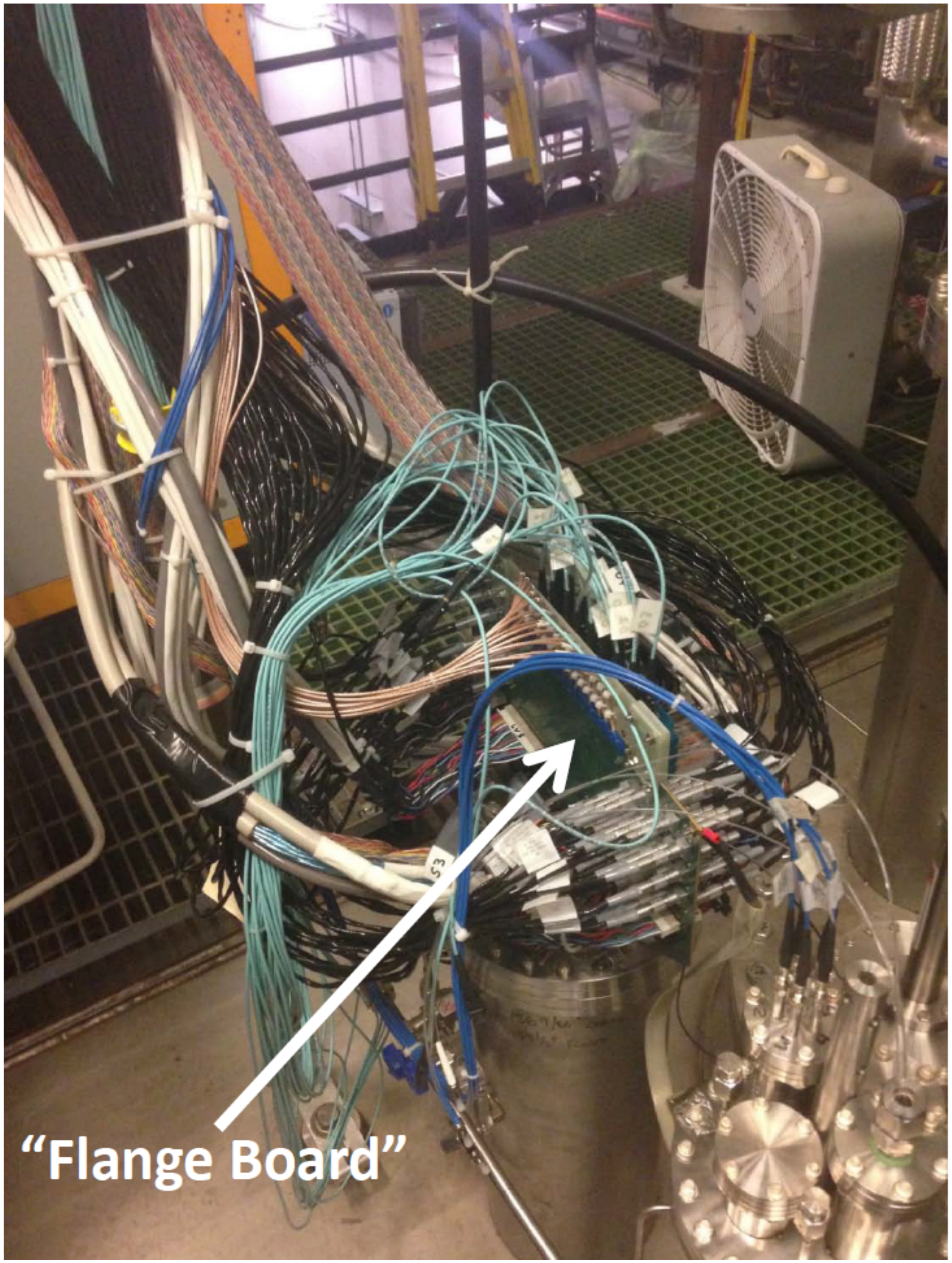


Summary comments on HNS in 35 ton

- The HNS, while high (~4fC), is still in the linear region and in the lower part of the dynamic range of the TPC readout (~100fC).
- The linearity of the readout response was confirmed by checking that the injected (calibration) pulser signal response was the same during the HNS as in normal operation. **This rules out an oscillation in the readout chain.**
- The **coupling** (magnetic or electrostatic) between the wire planes of different APAs, or from FEBs to the wire planes, **is too weak to sustain an oscillation** involving several APAs or any "collective oscillation" (verified by calculations).
- APA1 with ~400+ working channels shows ENC as low as ~700 e, **which could not be the case if an oscillation were present.**
- To be complete, some components of CE showed performance deficiencies (e.g., voltage regulator noise, ADC differential nonlinearity). None of those contributed to HNS, nor prevented readout functioning, some of which was for the first time (digital readout via FPGAs, which functioned through all the tests).

All observations point to marginal conditions of HNS, where the overall system instability involved the power supply and cabling system. The grounding guidelines (such as in MicroBooNE) were not followed, and the feedthrough was assembled without Faraday cage, making *a posteriori* diagnostics very difficult.

35ton (open) feedthrough



MB feedthrough