ProtoDUNE-SP CE Electricals

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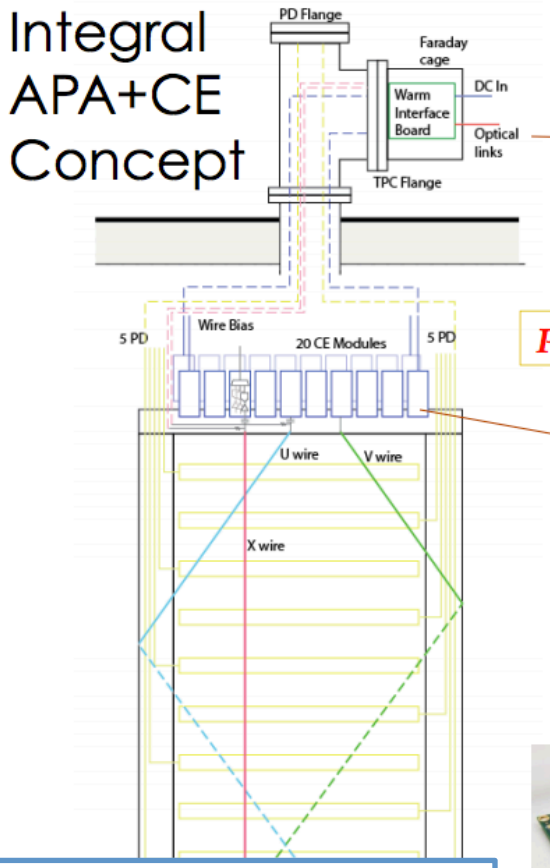
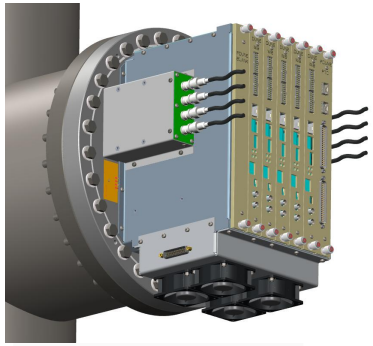
ProtoDUNE-SP Cold Electronics Production Readiness Review
May 3, 2017

Outline

- Cold Electronics introduction
- Electrical components
  - FE and ADC ASICs
  - Front End Motherboard (FEMB)
  - Warm Interface Board (WIB)
  - Power and Timing Card (PTC)
  - Power and Timing Backplane (PTB)
- Schedule and shipping
- Summary

LArTPC Cold Electronics

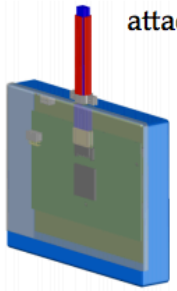


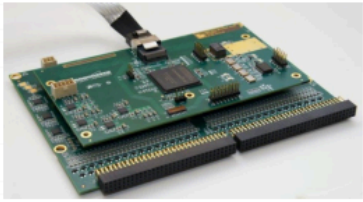


Warm Interface Electronics Crate: interface between CE and DAQ with local real-time diagnostics.

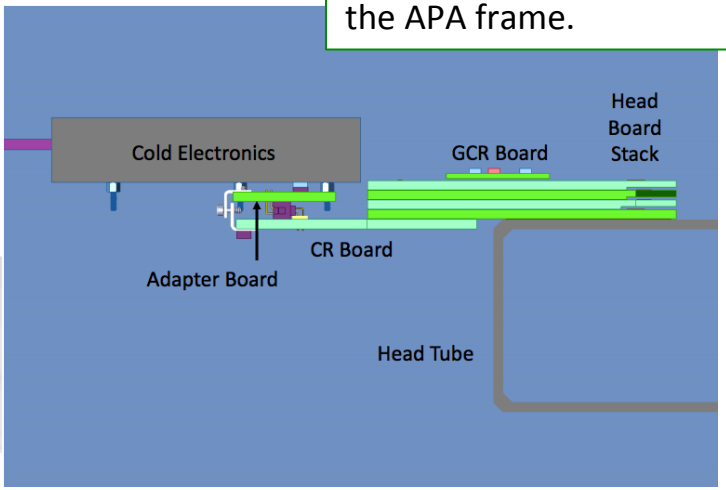
ProtoDUNE-SP

Cold electronics module and its attachment to the APA frame





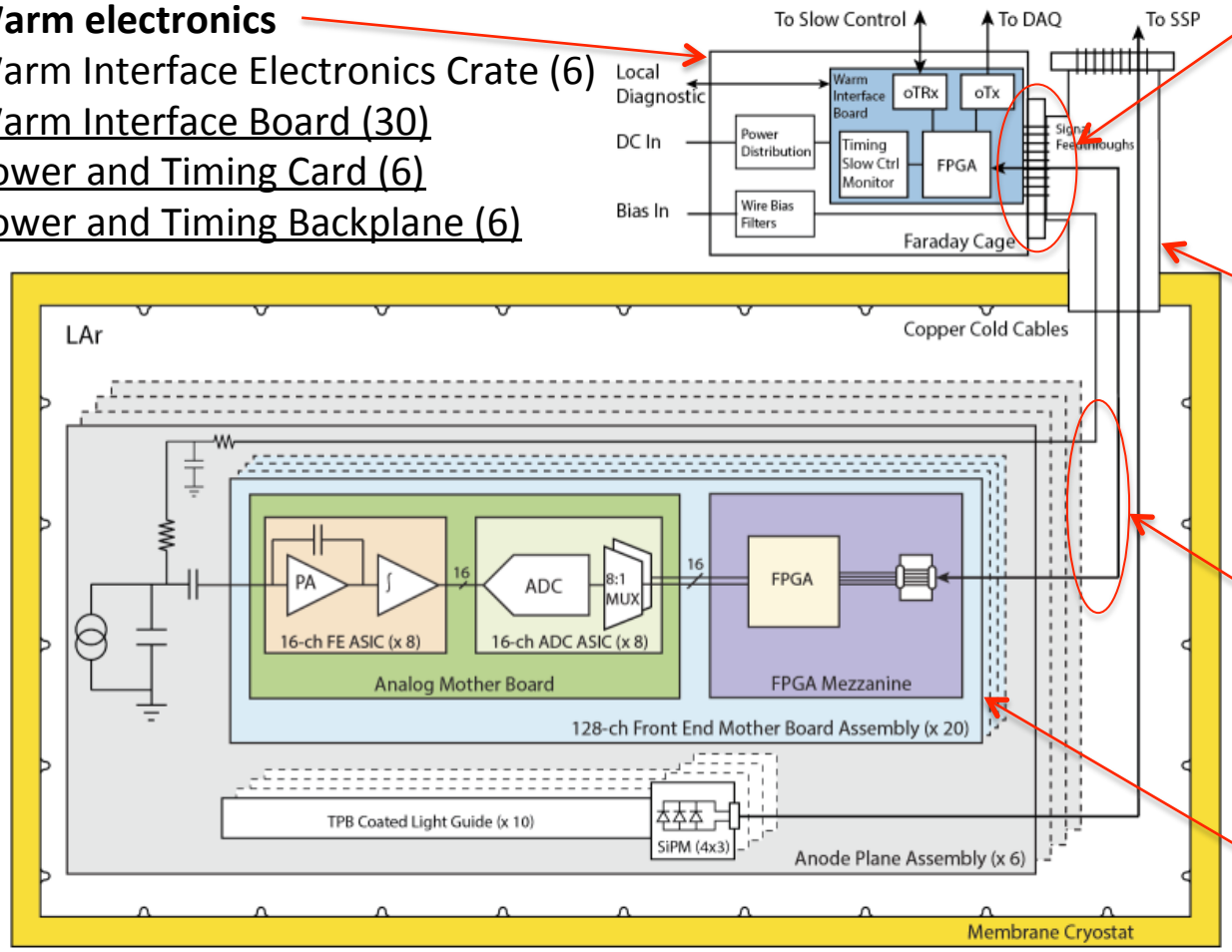
Common plane of all cold electronics must make low impedance connection to the APA frame.



Each APA must be isolated inside the cryostat and only connected to the cryostat at the flange.

ProtoDUNE-SP Cold Electronics

Warm electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable to FEMB
LV and data cable (120+120) and APA wire-bias SHV cable (48)

Front End Motherboard (FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

Front End ASIC

- ~5mW/channel for long lifetime
- 16 independently programmable channels
  - 4 gains: 4.7, 7.8, 14, 25 mV/fC
  - 4 shaping times: 0.5, 1, 2, 3 µs
  - 2 baselines: 200 mV/900 mV
  - Analog test output
- 2012 design of front end (FE) ASIC deployed in multiple LAr TPCs:
  - MicroBooNE (**ENC ~400e-**), CAPTAIN, LArIAT, 35-ton, ARGONCUBE@Bern, ICARUS 50l TPC@CERN
- 2 subsequent revisions:
  - P1 version tested at MSU/BNL since July 2016
  - Current version (P2) has been at BNL since November 2016

Bandgap Reference

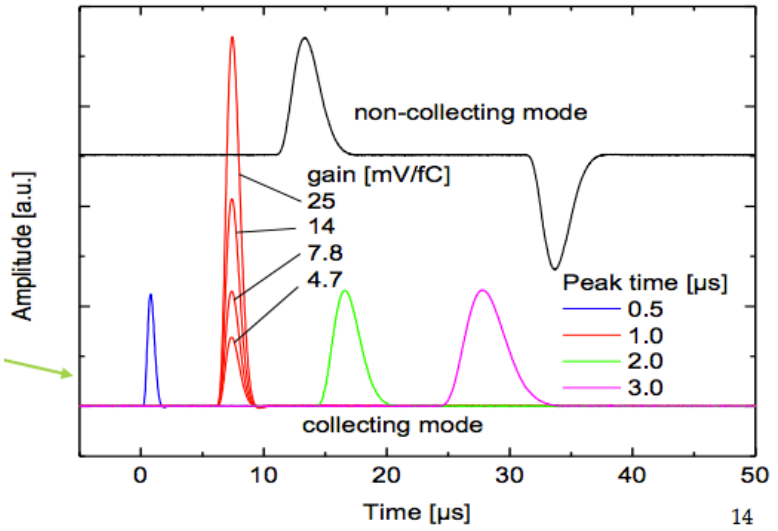
$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{at}\ 300\ ^\circ K \\ 1.164\ V \ \text{at}\ 77\ ^\circ K \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{at}\ 300\ ^\circ K \\ 259.3\ mV \ \text{at}\ 77\ ^\circ K \end{cases}$$

~ 2.86 mV / °K

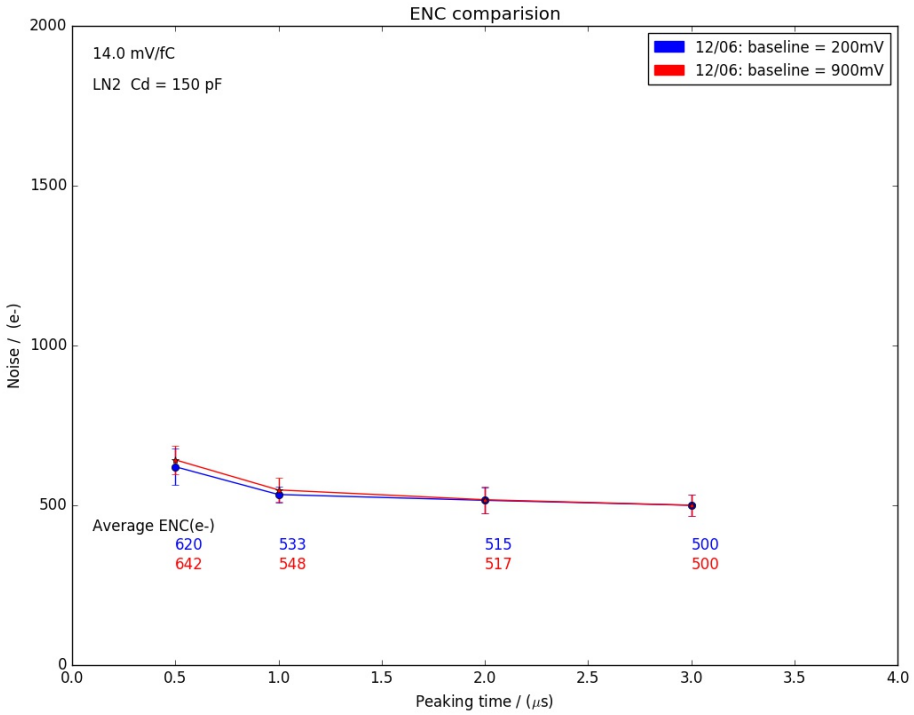


Datasheet: DUNE Doc 1484

FE ASIC Development

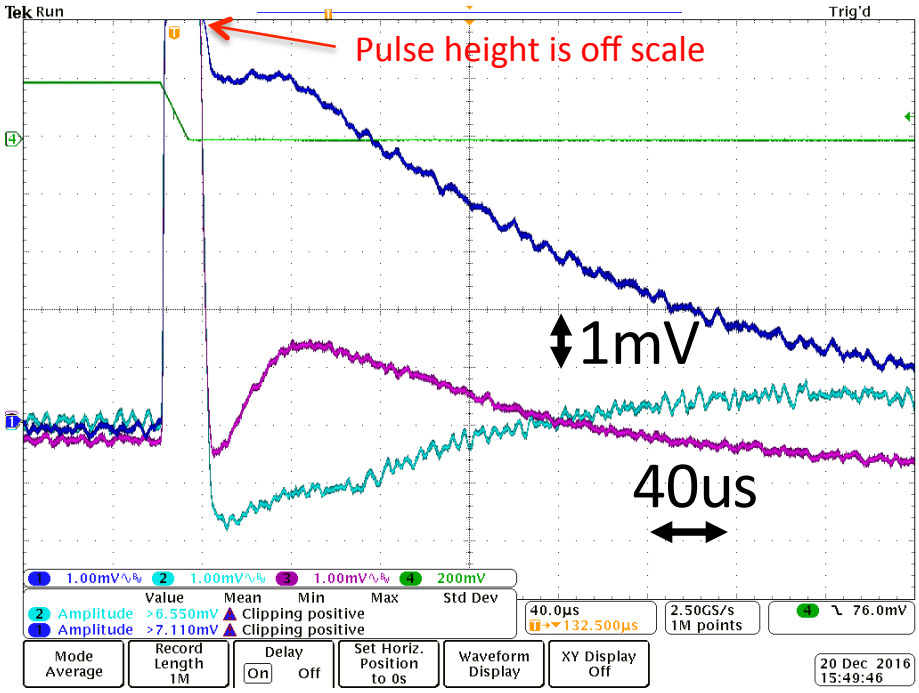
Version	Feature	Tested
P1	6-bit internal DAC	DNL < 0.2 LSB; INL < 0.5 LSB
P1	Buffer-off mode (ADCs onboard FEMB)	OK
P1	Add 1nA and 5nA leakage current capability	OK
P1	Add “smart” reset (2 pins instead of 1)	OK
P1	Revise BGR start-up circuit (~5% ASICs fail to power on in cryo)	No failures seen under 2000 thermal cycles
P1	Increase ESD protection on IO	OK
P2	Revise bias current design (removes need for external resistors to bring up every channel)	OK
P2	Address pole-zero cancellation	< 1.5% dispersion
P2	Add analog output	OK

P2 FE ASIC Evaluation



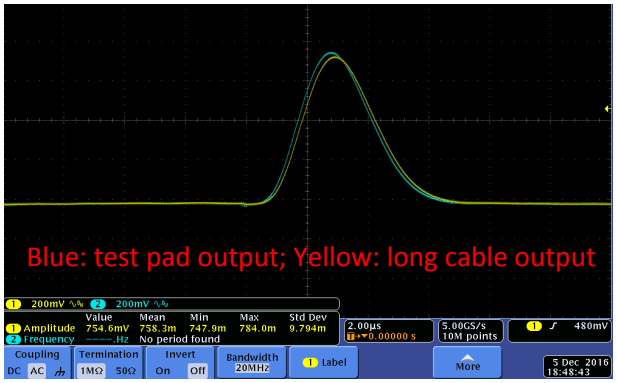
Noise < 550 ENC at shaping times > 1 μs
Measured on FEMB with V* ADCs
(stuck codes removed)
No 1 GOhm external resistors needed

Pole-zero cancellation
P1 FE baseline recovery dispersed by ~5% of peak height ⟶ P2 FE ~1.5% PH



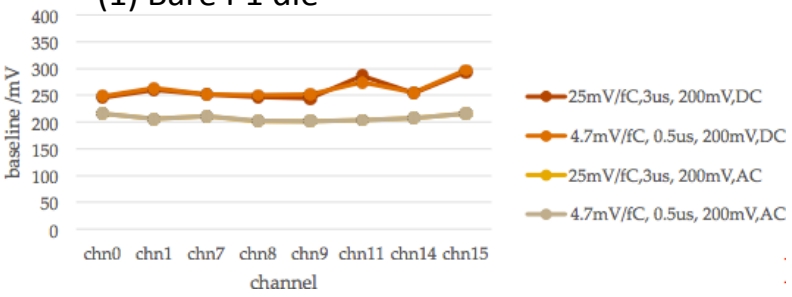
(Green: Calib Pulse); (Dark Blue: P1 chn14); (Light Blue: P2 chn2), (Pink: P2 chn14)

P2 FE ASIC Evaluation

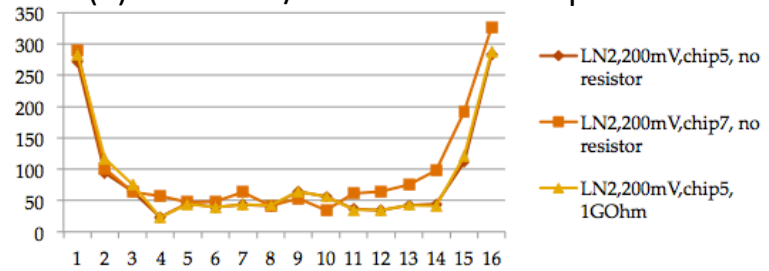


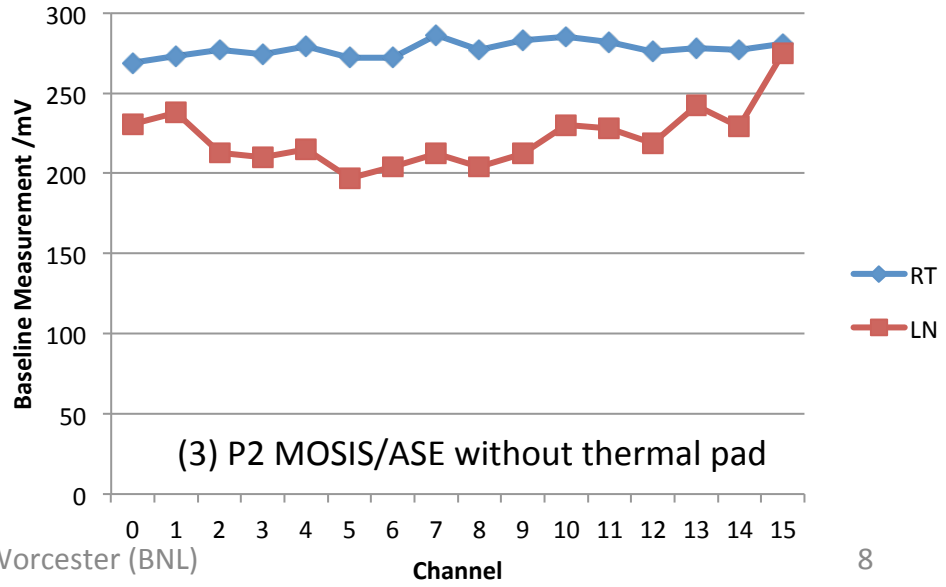
- FE analog output
  - Shares the same pin with the calib test pulse input/DAC output
  - The configuration register will control one of 16 channels to be routed to the monitoring output
  - FEMB design has signal routed to the WIB via the cold cable
- Baseline non-uniformity in LN2
  - Observed in P1/P2 ASICs (200 mV only)
  - Thought to be caused by combination of thermal pad and packaging stress
  - Tested three vendors: Quik-pak, Novapack, and MOSIS/ASE
  - MOSIS/ASE provides the best packaging solution at the moment: low stress compound w/o thermal pad

(1) Bare P1 die

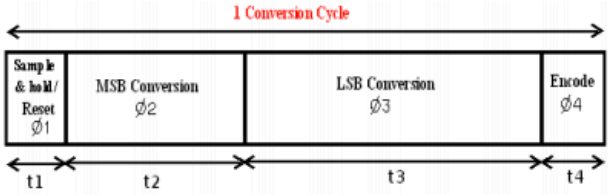


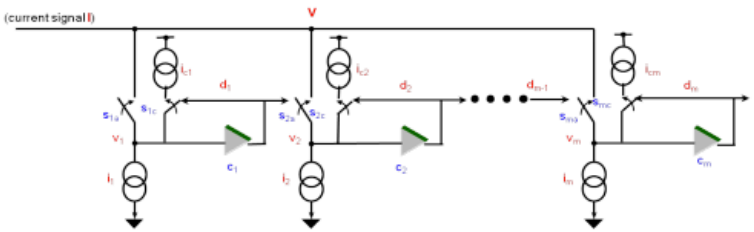
(2) P1 MOSIS/ASE with thermal pad

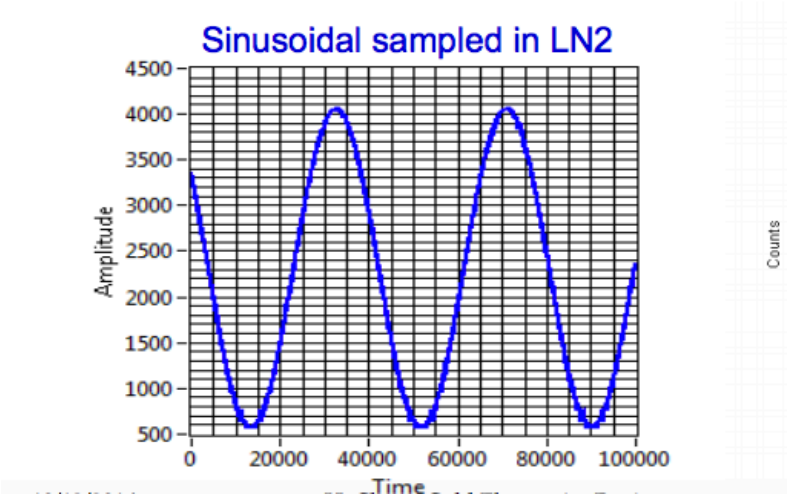




ADC ASIC







Datasheet: DUNE Doc 1485

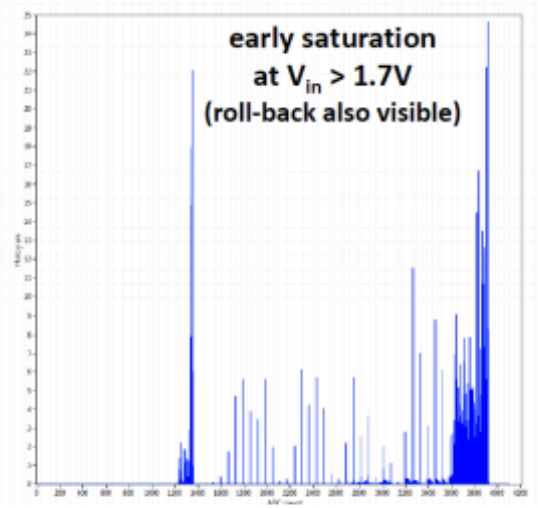
- ~5mW/channel for long lifetime
- Current-mode domino architecture with 4 phase operation
  - Sample/hold
  - 6 MSB conversion
  - 6 LSB conversion
  - encoding
- 16 programmable channels
- 12 bit ADC up to 2 MHz internal or externally-applied sampling clock
- 2014 version of ADC ASIC deployed in 35-ton prototype
  - Stuck codes observed
  - All high-speed digitized data links (2048 channels) functioned in LAr
- V* ADC tested at BNL since Jan 2016
  - Used to qualify FEMB prototypes up through P2 FEMB
- Current version (P1) ADC has been at BNL since October 2016

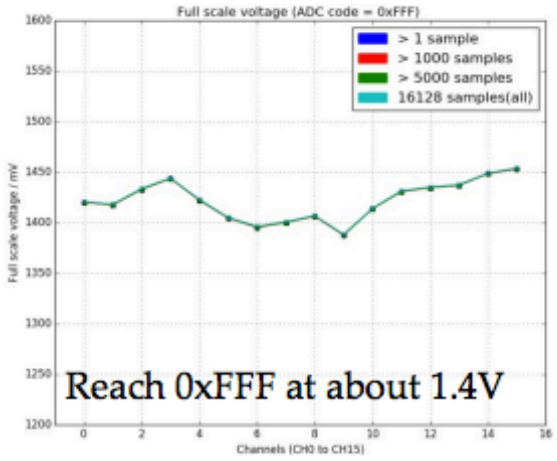
ADC ASIC Development

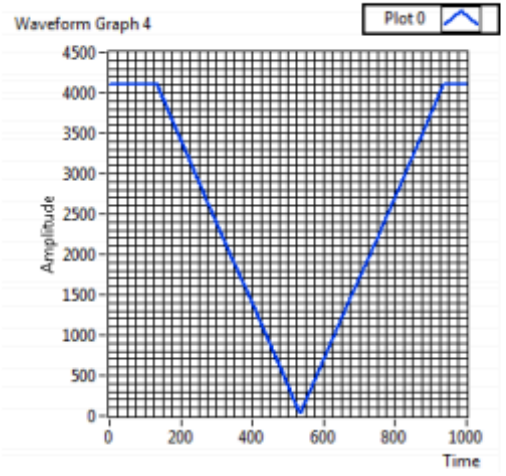
Version	Feature	Tested
V*	Partial fix to INL/DNL (stuck codes)	OK
V*	COLDATA compatible (external sampling clock and ADC-busy signal)	OK
P1	Add test-pattern and FIFO soft reset	OK
P1	Fix INL/DNL (stuck codes)	NO
P1	Fix early saturation and roll-back issues	OK
P1	Revise BGR start-up circuit	No failures seen in 2000 thermal cycles
P1	Increase ESD protection on IO	OK
P1	Modify configuration interface (from LVDS to single-ended for FE ASIC compatibility)	OK
P1	Default power ON in data collection mode	OK

P1 ADC ASIC Evaluation

- Early saturation (ADC not reaching 0xFFF) no longer present
- Roll-back (as input voltage increased above saturation, codes decrease) fixed
- DNL "stuck codes" are still observed
  - Approximately 5% in P1 (all channels) in LN2 averaged over entire dynamic range
  - Can be further mitigated by careful selection of operating mode
- Other design features verified







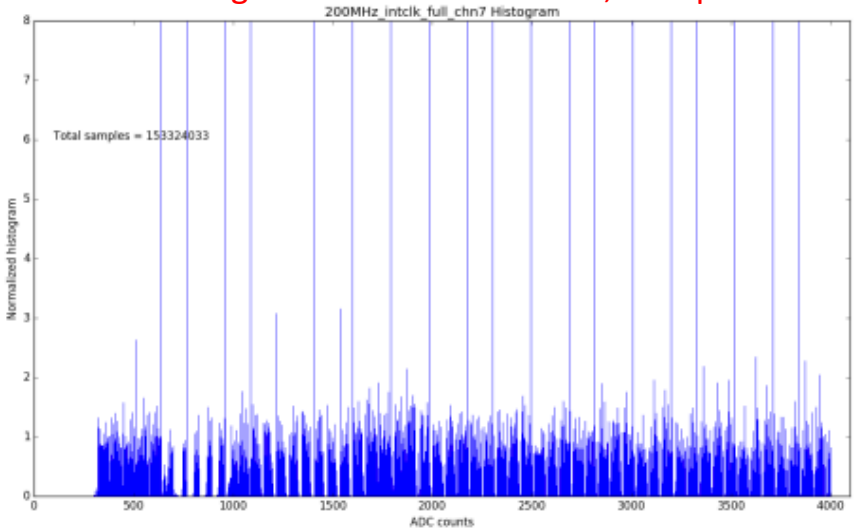
V* ADC with early saturation

Early-saturation & roll-back is fixed on P1 ADC

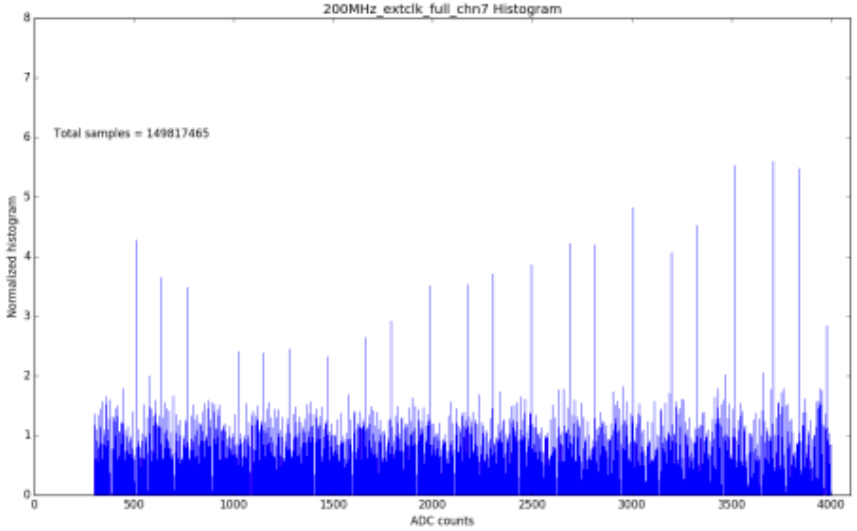
P1 ADC DNL “stuck codes”

- Test ADC with a high-precision ramp voltage in LN2:

Using 200 MHz internal clock, 2 Msps

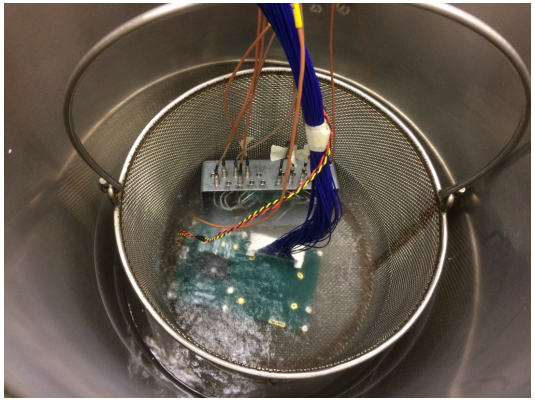


Externally generated 200 MHz clock, 2 Msps

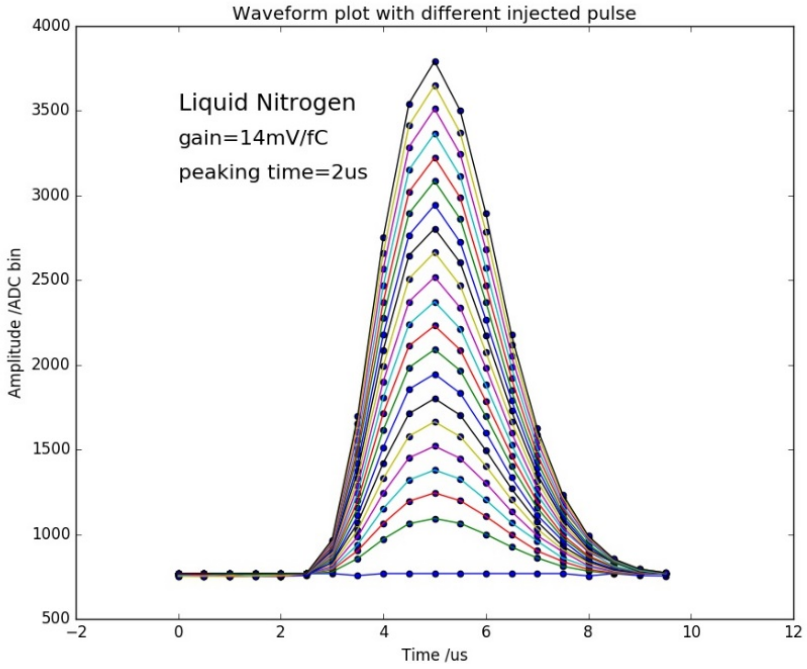


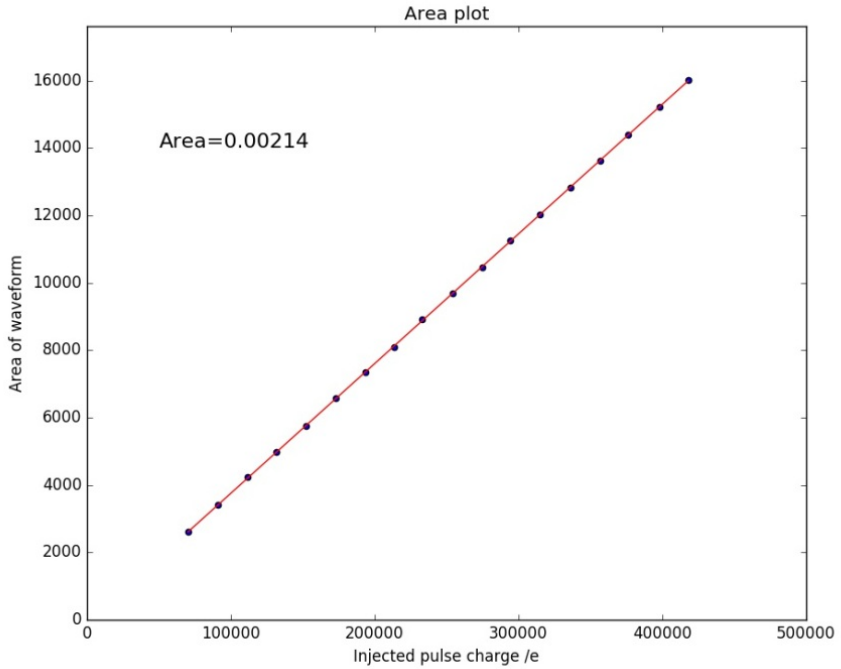
- Preferred operation mode of P1 ADC has been established
  - Full steering current
  - External control clocks
  - AC coupling with bias to eliminate low ADC range

P1 ADC ASIC Evaluation



- P2 FE + P1 ADC Test
  - Peak and area linearity test of P2 FE and P1 ADC in LN2
  - Same FE channel is used to test 16 ADC channels
  - Both peak and area measurements show reasonable non-linearity (< 0.5%)
  - FE 14mV/fC, 2us t_p + ADC 2Msps
    - Peak INL: 0.274+/- 0.050%
    - Area INL: 0.254 +/- 0.070%





ASIC Production

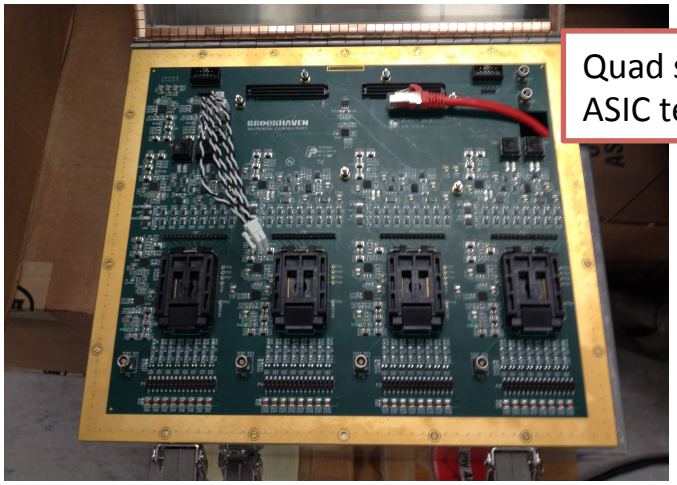
- 280 P2 FE and 400 P1 ADC ASICs ordered in January to prepare APA1 electronics
  - Expect packaged ASICs at BNL for QC testing in late May
- Final production: at least 3000 each of the P2 FE and P1 ADC submitted to MOSIS
  - Following Tech Board approval on Jan 25th
    - Early approval needed because of long lead time
  - Expect packaged ASICs at BNL for QC testing in late June
- Use custom ASIC testboards and Cryogenic Test System (CTS) for all QC testing

FE ASIC QC Plan

- Every FE ASIC will be tested at RT and a cryo yield will be measured with ~10% of the ASICs prior to FEMB assembly
  - All FE ASICs will be tested in LN2 under multiple thermal cycles on assembled FEMB

  CE QA/QC Electricals Plan Dune DocDB 1809
- Criteria for passing:
  - All 16 channels functional at every setting in Table 2
  - Channel cross-talk measured
  - Built in FE DAC pulser functional at all 64 amplitudes, all channels
- Quad socket FE ASIC testboard schematics

  Dune DocDB 3345
- All test results will be stored in CE QC database
- ASICs which pass will be assembled onto FEMB



Quad socket FE ASIC testboard

Parameter	Values	# of test cycles	Channel/ Global
Gain	4.7, 7.8, 14 and 25 mV/fC	4	CH
Filter peaking time	0.5, 1, 2, and 3 μs	4	CH
Baseline	200/900 mV	2	CH
Test capacitor	enable/disable	2	CH
Coupling	AC/DC	2	CH
Buffer	enable/disable	2	CH
Channel 1 setting	signal/monitor monitor = temperature or bandgap	3	GL
Leakage current	0.1, 0.5, 1.0, 5.0 nAmp	4	GL
Analog out	enable/disable	16	CH

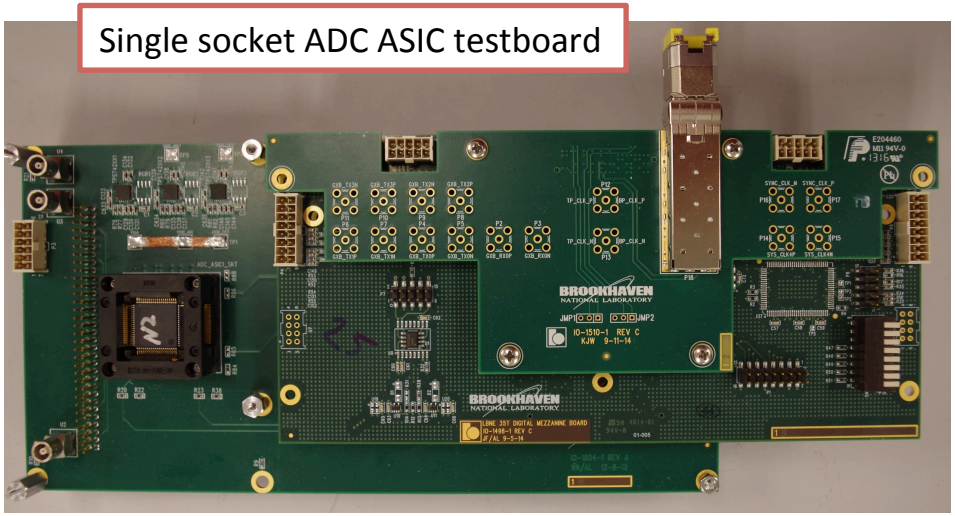
Table 2: Summary of P2 FE ASIC parameter test cycles.

ADC ASIC QC Plan

- Every ADC ASIC will be tested at RT and in LN2 prior to FEMB assembly

  CE Electricals QA/QC Plan Dune DocDB 1809
- Criteria for passing (Table 3):
  - ADC functional with internal/external clock sources for all channels
  - Preferred operation mode with FE ASIC input functionality OK
  - External ramp test (next slide)
- Single socket ADC ASIC testboard schematics

  Dune DocDB 3345
  - Quad socket ADC ASIC layout done
- All test results will be stored in CE QC database
- ASICs which pass will be assembled onto FEMB
  - FE & ADC ASICs for APA1 selected by mid June
  - FE & ADC ASICs for APA2-3 selected by late July

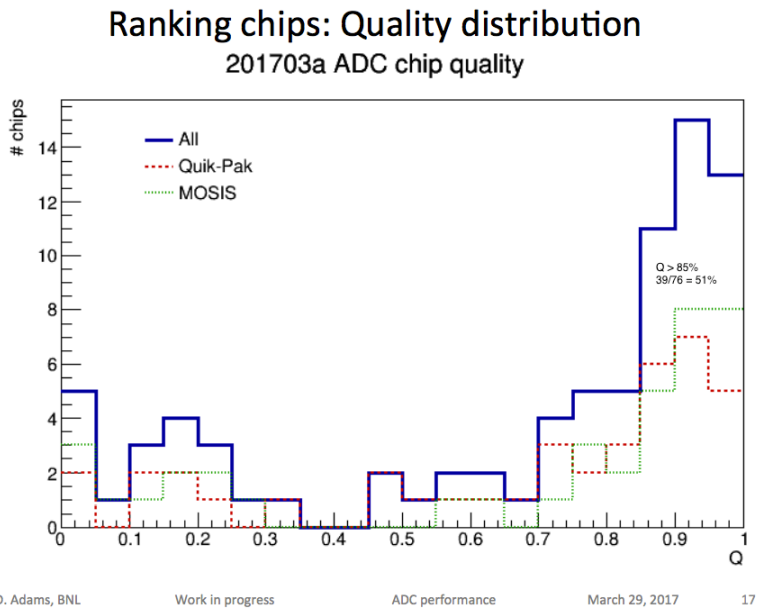


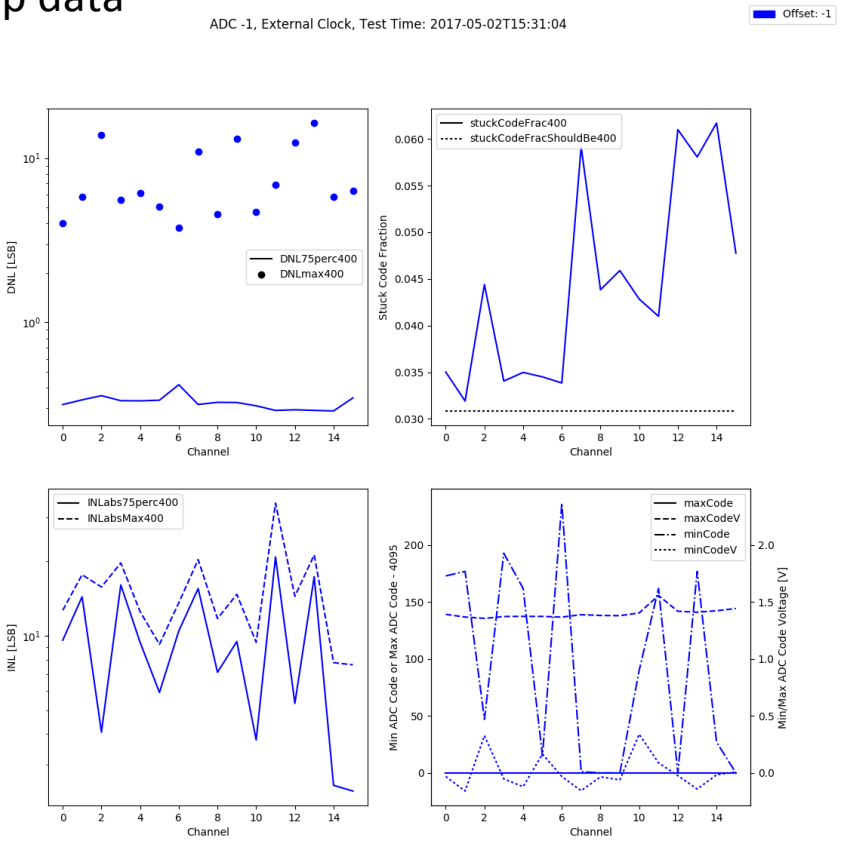
Source	Values/Test	# of test cycles
Digitize clock	external 1.0 and 2.0 MHz internal	4
FE ASIC	multiple FE ASIC settings normal operation of ADC	32
External ramp	Stuck code, saturation, roll-back, & linearity	1

Table 3: Summary of ADC ASIC parameter test cycles.

ADC ASIC QC Ramp Criteria

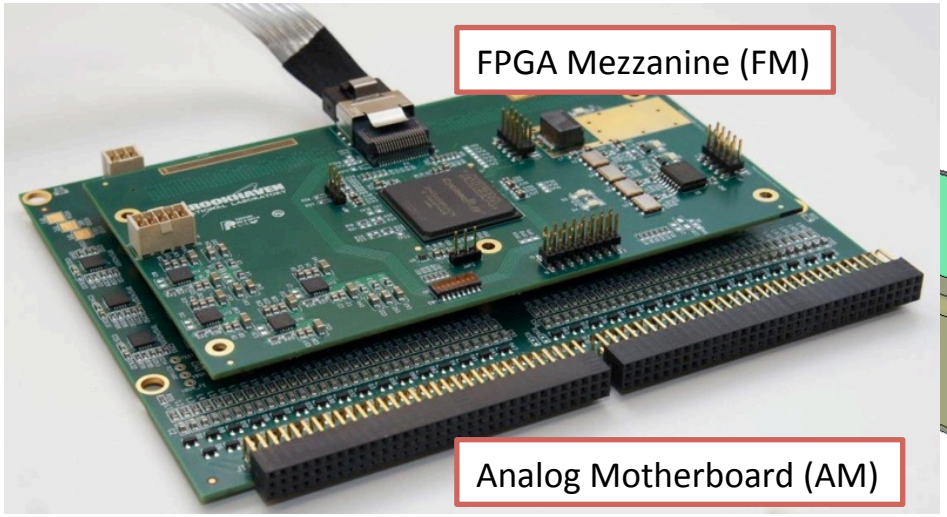
- External ADC ramp input measures linearity, stuck code fraction, and effective ADC range (saturation and roll back)
- ADCs will be passed by quality criteria on ramp data
  - Overall linearity (fit values and chi2)
  - Residual bin resolution
  - Differential non-linearity and stuck code fraction
  - Effective range

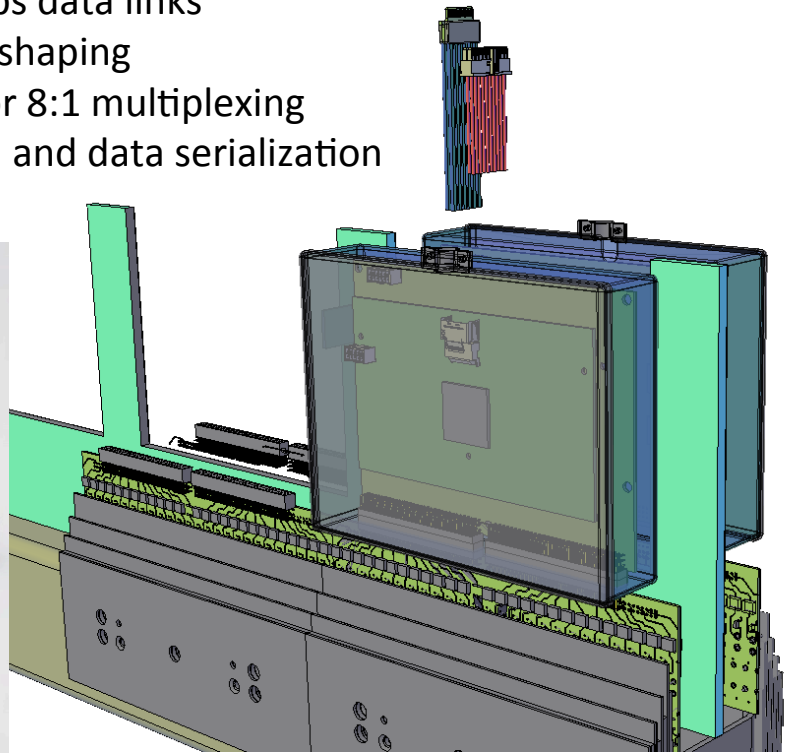




FEMB

- 128 channels of digitized wire readout, 4x1 Gbps data links
- 8 16-channel FE ASICs: pulse amplification and shaping
- 8 16-channel ADC ASICs: digitization and 16:1 or 8:1 multiplexing
- FPGA mezzanine for ASIC control/configuration and data serialization





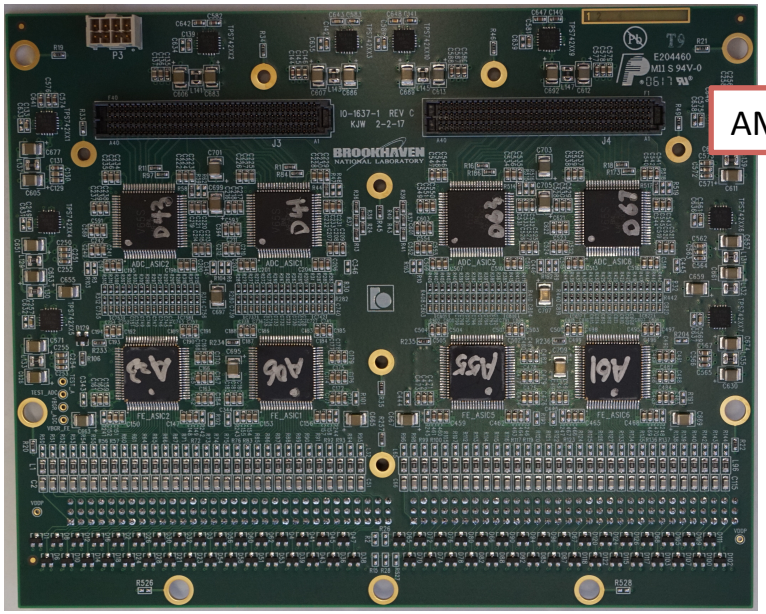
FEMB individually enclosed in CE Box: 20 FEMB/APA

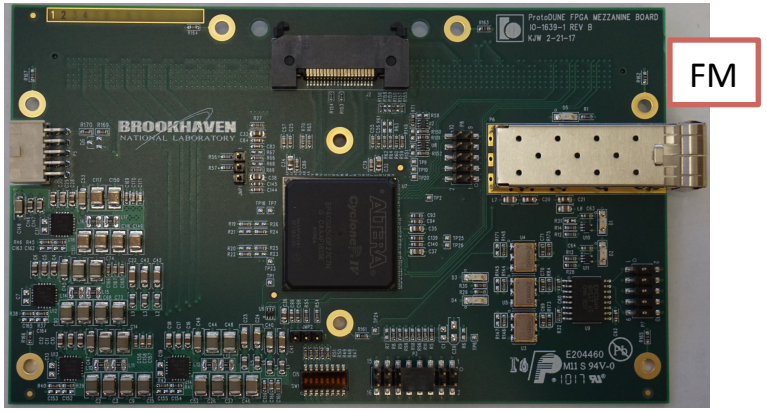
- Attaches to PSL APA adapter and incorporates built-in cable strain-relief
- Low impedance connection from FEMB ground to APA frame
  - Reinforced by copper braid from CE Box to APA mounting brackets

P2 FEMB contain P2 FE and P1 ADC

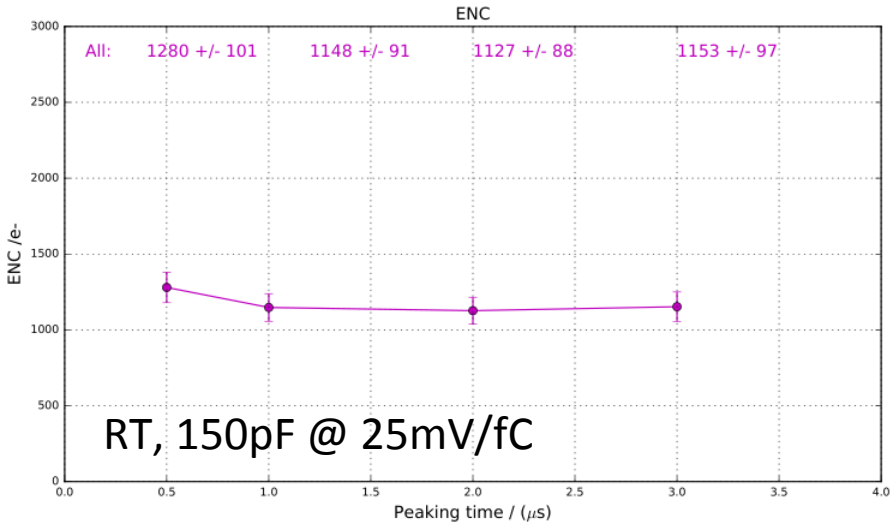
FEMB

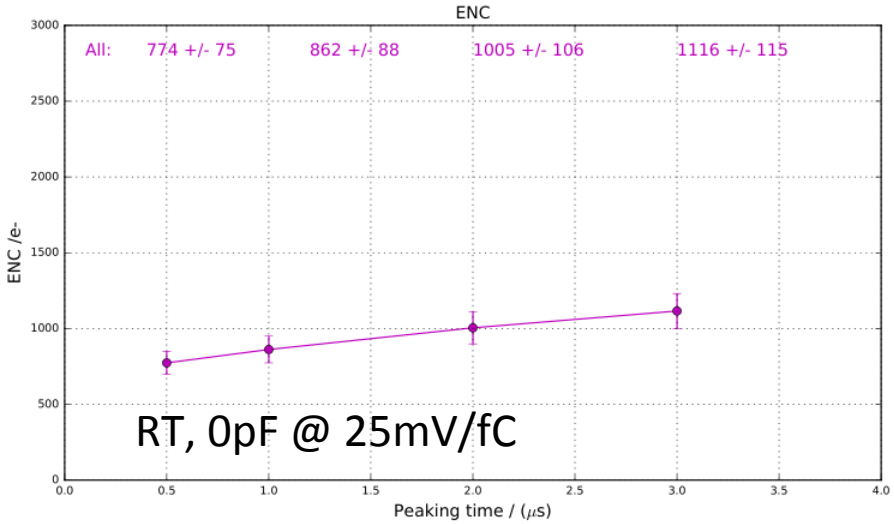
- FEMB schematics, layout, and BOM in [DUNE DocDB 1419]
  - Includes toy TPC which enables 150 pF load (~7m wire equivalent) on all 128 FE channels
- Current status
  - Extensive testing with P1 FEMB (P1 FE/V* ADC) aka “SBND prototype”
  - 3 P2 FEMB at BNL
    - Functionality OK; good ENC performance in reception testing (next slide)
- Production plan
  - Sufficient PCB at BNL to assemble 25 FEMB with January ASIC order for APA1
    - Submit APA1 FEMB assembly when ASIC QC complete in early June
    - 2 weeks for assembly
  - Submit final order of PCB fabrication for 160 AM and FM on 5/24
    - 2 weeks lead time
- Ready for final FEMB assembly with production ASICs in late July

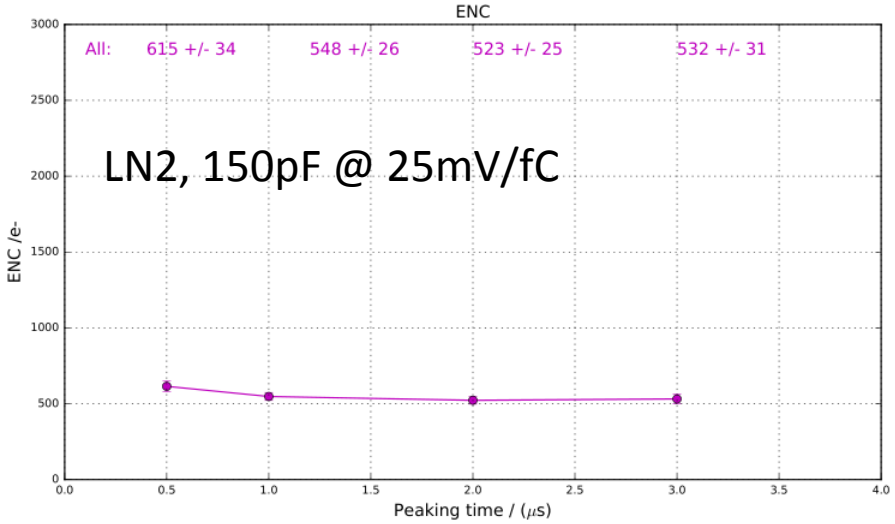


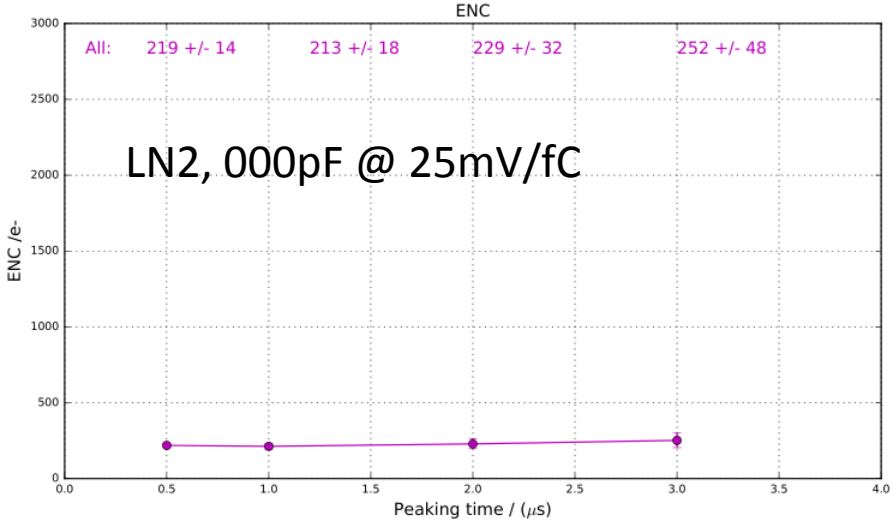


ProtoDUNE FEMB ENC Performance









FEMB QC Plan

4.1 Functionality

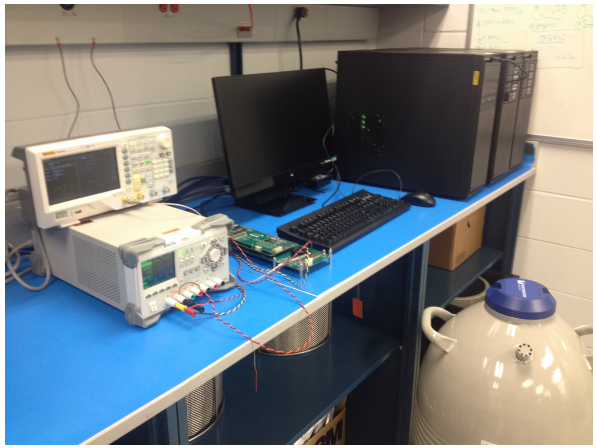
To validate the functionality requires testing the following features of the FEMB both at room temperature and under multiple thermal cycles in LN2:

- successful loading of the FPGA programming from the onboard EEPROM;
- ability to program the FPGA and EEPROM over the backup JTAG links in the cold data cable bundle;
- ability to set the control registers on the FPGA via the I^2C control IO links;
- confirmation that the backup onboard oscillators can generate the clock for the FPGA state machine in case the clock from the system is lost;
- confirmation that the FPGA can configure all 16 ASICs on the analog motherboard via SPI interface and synchronize the data from all serial links from the ADCs (either 16:1 or 8:1 multiplexing on each ADC ASIC);
- verify that in the state with all ASICs configured, the current drawn by the CLR for all LV power inputs are nominal, indicating the FPGA is programmed and ASICs operational;
- confirmation that all channels observe both the FPGA internal pulser and an external pulser with the FE test capacitor enabled;
- confirmation that all channels observe the FE ASCI internal pulser;
- successful transmission of all digitized waveform data over all 4 ~1.2 Gbps links at sufficiently low Bit Error Rate (BER).

- FEMB will be delivered to BNL from vendor
  - Visually inspected and cleaned upon reception
- All FEMB will be pre-tested in LN2 to reject/replace bad components
  - Functionality tests + repeat ASIC QC testing
- Selected FEMB will be “dressed”
  - Installed in CE Box with mounting hardware
  - Cold cables clamped and cover closed
  - PSL adapter board attached
- FEMB + cable + adapter are final unit and each one will be individually retested in LN2
  - Connection from adapter socket to FEMB input checked with toy TPC (redesign for adapter is done)
  - Criteria to pass QC:
    - Full suite of FEMB QC passed: functionality, noise characterization, ADC response (DUNE DocDB 1809)
    - No visible stress damage or loose hardware after return to room temperature
  - Results stored in QC database for comparison at CERN
- Final units shipped from BNL to CERN
  - Custom shipping crates to be designed and built at BNL
  - Electronics can be stored in shipping boxes until installation

QC Teststands and Shift Plan

- PCs, power supplies, and equipment for QC teststands installed at BNL

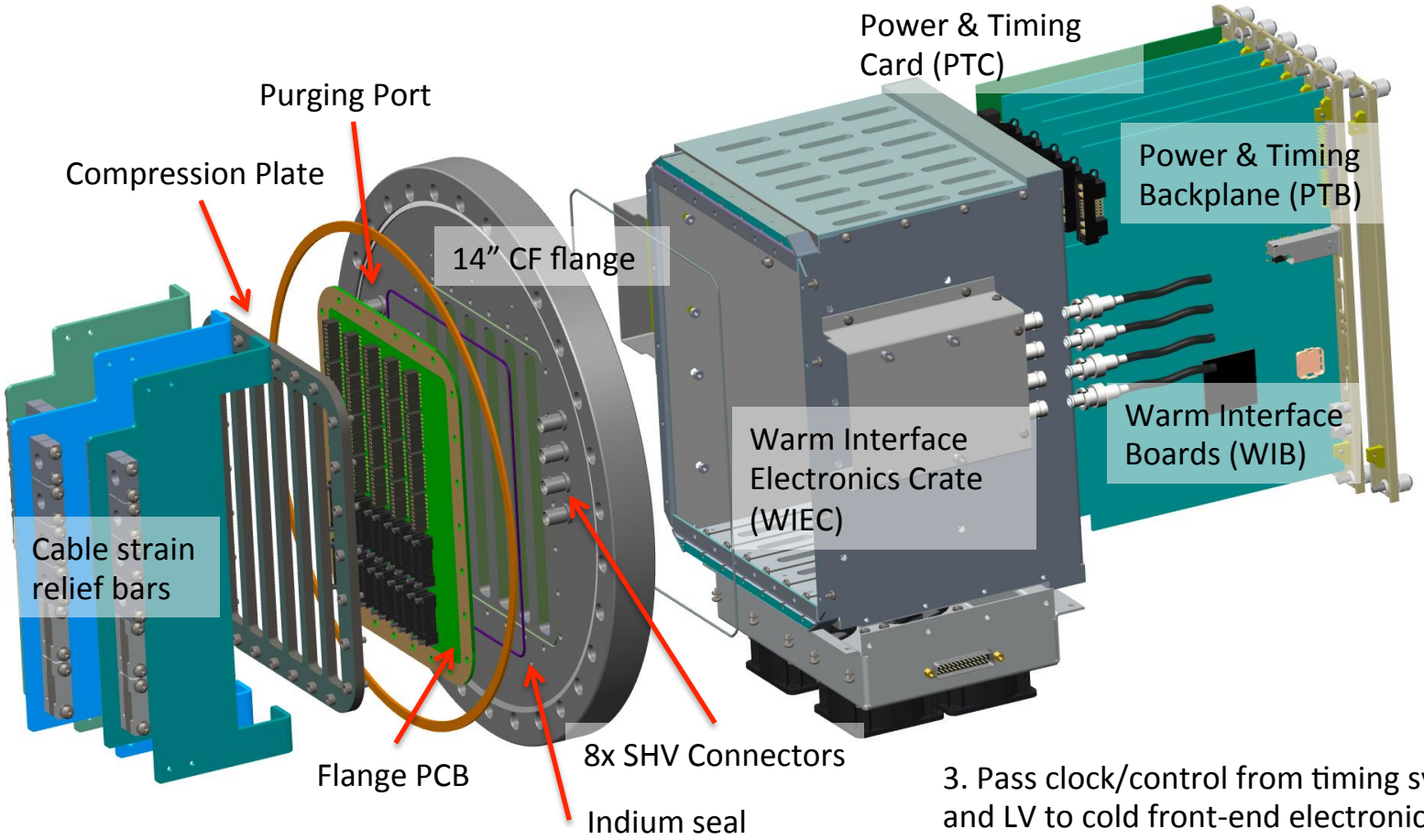


- E. Worcester and M. Bishai shift coordinators
  - Guang Yang (SBU) and Jyoti Joshi (BNL) shift leaders
  - B. Kirby (software), B. Viren (computing), S. Gao (ASICs), J. Fried (FEMB) on call expertise
- Shift calendar to sign up available:

https://docs.google.com/spreadsheets/d/15a-QsJhyJppWninh5XQquv_DmerxDRAn_NDW2tmgj4c/edit#gid=494612915

  - Shifters will be trained at BNL
  - CE expertise not required to shift
- Tagged QC software releases available: https://github.com/DUNE/femb_python
- Shifts expected to run from June-September 2017

CE Warm Components



1. Connection to detector ground at CE flange
2. Pass wire-bias and FC HV to cryostat

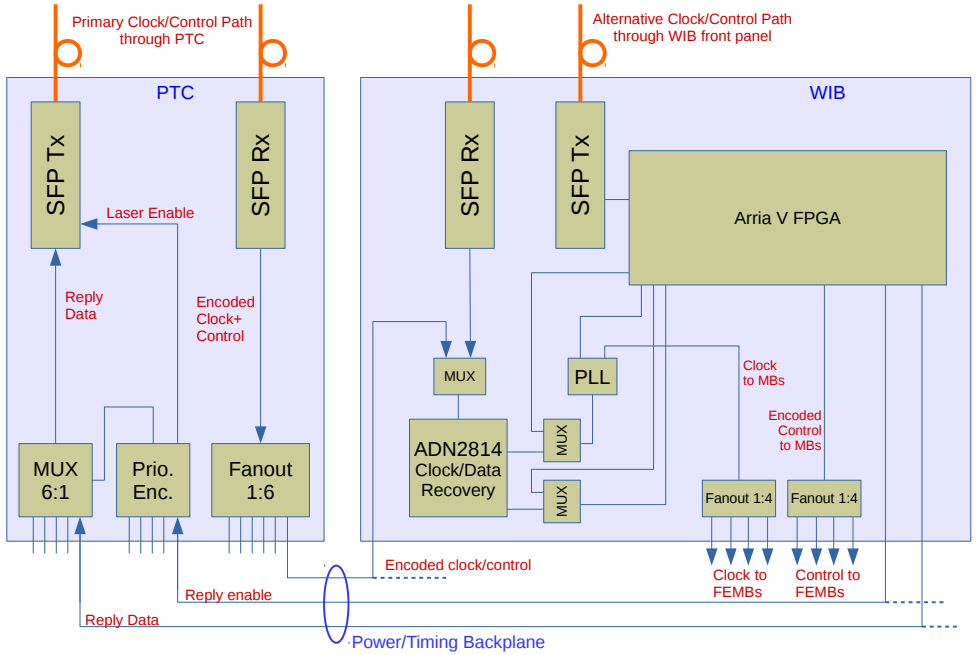
3. Pass clock/control from timing system and LV to cold front-end electronics
4. Deliver high-speed TPC wire data from cryostat to DAQ

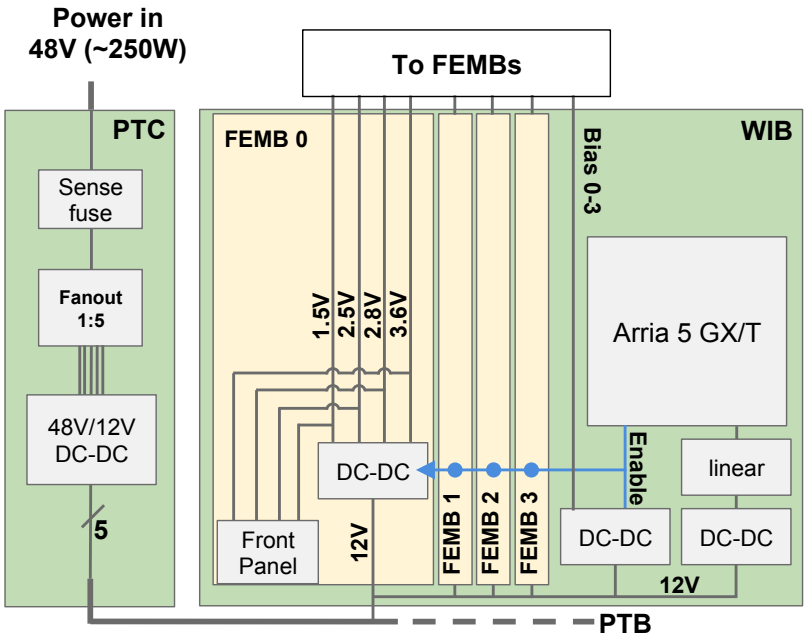
Warm Electronics

PTC receives the timing and control from the 50 MHz encoded system clock and fans it out to all WIB in WIEC over the PTB

WIB sends timing and control to 4 FEMBs and receives high-speed TPC data over cold data cable and transmits it to the DAQ systems over optical fiber

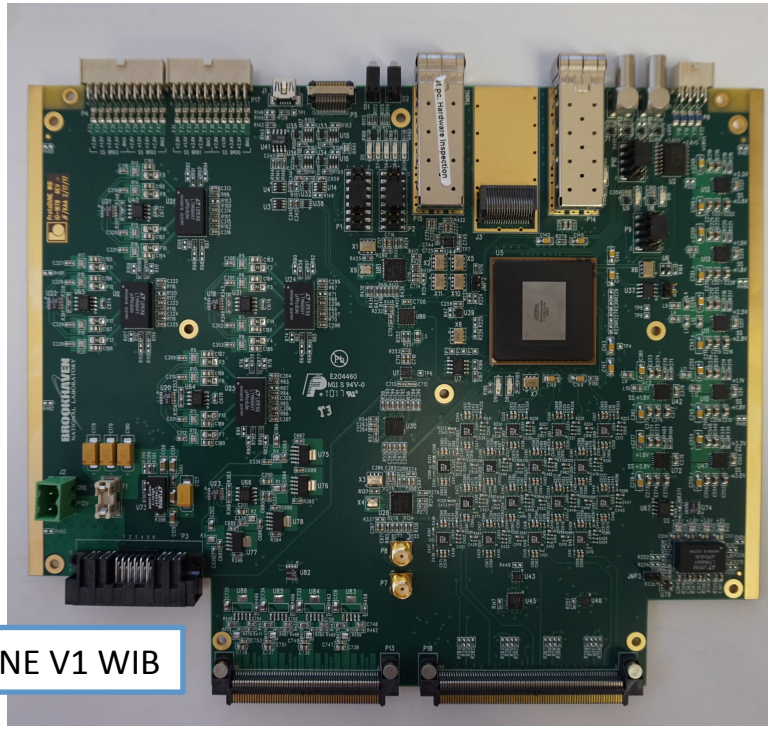
PTC receives 48VDC from LV power units, steps it down to 12VDC and fans it out to WIB over the PTB, WIB steps 12VDC down to VDC required for FEMB and provides LV power over cold LV cable





WIB

- Collaboration between BNL (hardware) and Boston University (firmware)
- V1 WIB schematics, layout, and BOM in DUNE DocDB 3327
- Current status
  - Integration/noise measurements ongoing with SBND WIB at Fermilab and BNL
  - ProtoDUNE V1 WIB received and tested at BNL (next slide)
    - Arria V GT variant FPGA (10 Gbps links)
    - ProtoDUNE clock/data separator
  - 1 WIB will be delivered to BU
    - Development of firmware for FEMB-WIB and WIB-RCE communication ongoing with SBND prototype
    - Develop firmware with timing endpoint from Bristol group (Xilinx to Altera port)
- WIB firmware repository:
  Boston DUNE WIB

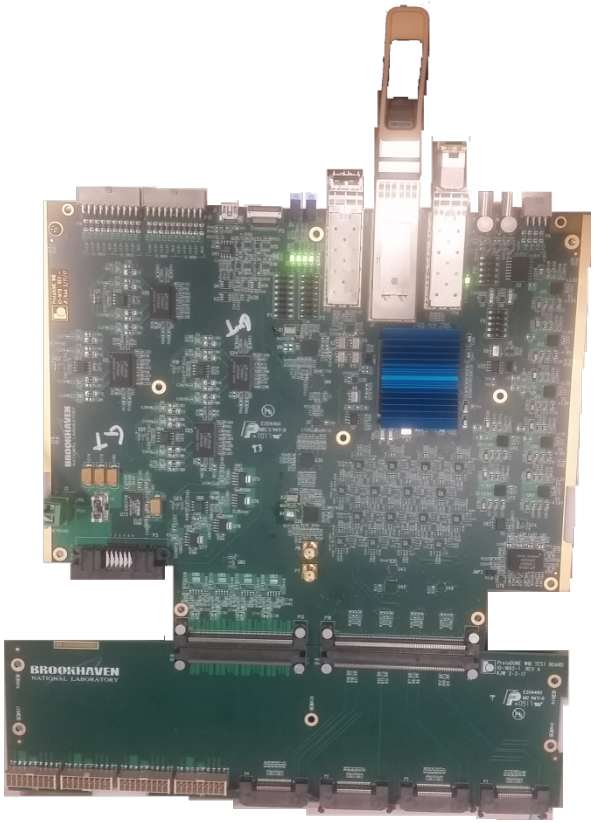


ProtoDUNE V1 WIB

- Production plan
  - Assemble 4-5 more V1 WIBs by end of May
    - Test and deliver to collaborators: FNAL, CERN
  - Minor modifications will be made for V2 WIB
    - Submit order for V2 fabrication on 5/12
    - V2 assembly of ~10 WIB done by late June
    - 5 V2 WIBs available for full crate test at BNL in July
  - Assemble full production WIBs early August
    - 2 weeks lead time
  - 3 weeks for QC in integration test stand

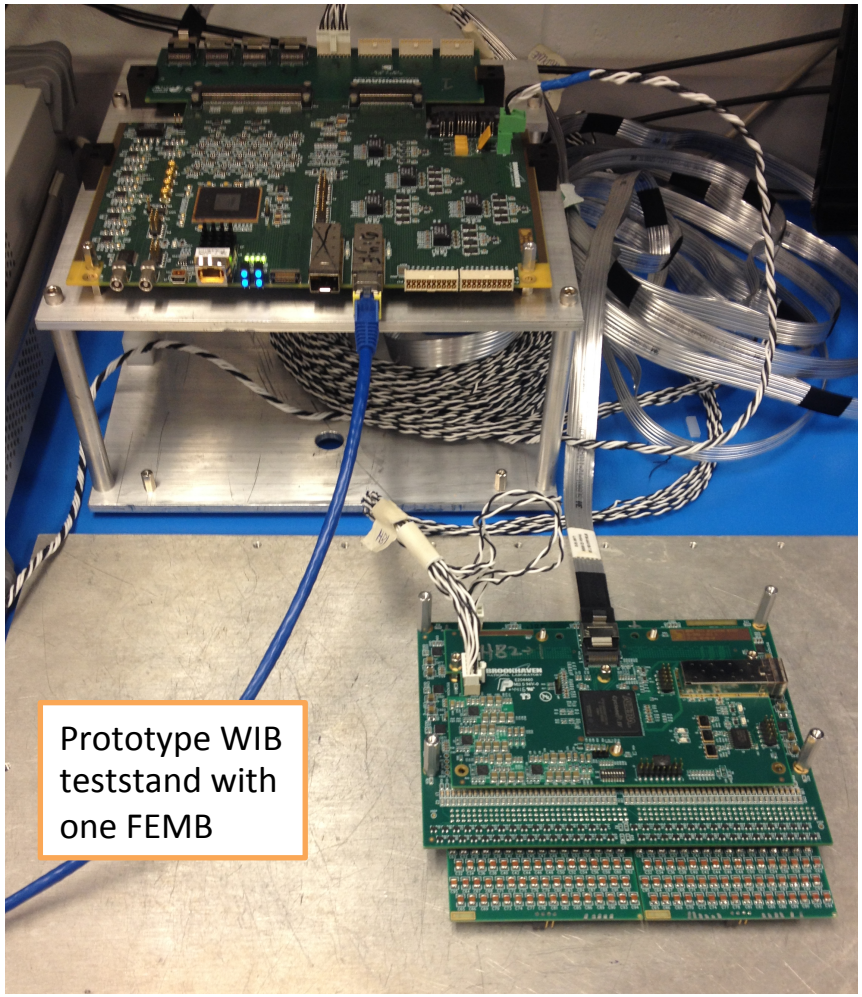
ProtoDUNE WIB Test Results

- Arria V GT transceivers with new FPGA layout
  - Gigabit Ethernet link
  - All 16 FEMB links operational
  - Each QSFP link tested at 6.25 Gbps for ~2×10^{13} bits
  - Verified 10 Gbps links
  - New Silabs PLL used for transceiver recovered clock verified
- New timing control paths tested
  - ADN2814 (clock/data recovery)
    - Verified signals form front panel SFP & PTB arrive to ADN2814
  - Silabs SI5344 PLL clock distribution operational
- WIB power monitor
  - Verified new power monitors for WIB FPGA regulators
- WIB Prototype issues corrected and verified
  - DC-DC converters are disabled at power up with no FPGA code
  - I^2C level translators added to power monitoring chips
  - FPGA DC-DC converter power up issues resolved when using force Conduction Mode (allows for lower output ripple)
  - Replaced high current DC-DC converters used for FEMB regulator bias with low current DC-DC converter reducing power by 420mW per FEMB



WIB QC Plan

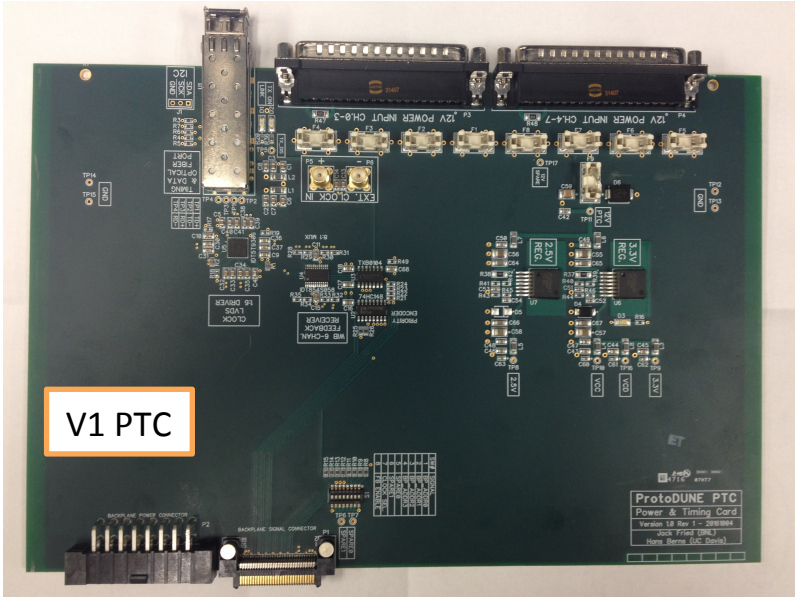
- V2 WIB will ship to BNL from vendor
- 3 weeks for QC
  - Every WIB will be tested in the integration teststand
  - Criteria for acceptance
    - WIB receives clock from timing system and transmits return synchronization clock
    - All four FEMB receive timing and clock from WIB and pass all functionality tests
    - All high-speed data transmitted without significant BER ($<10^{-13}$)
  - All WIB tested at BNL with BU firmware
- Production WIB ship to CERN in mid September
  - WIB packaged individually in anti-static bags

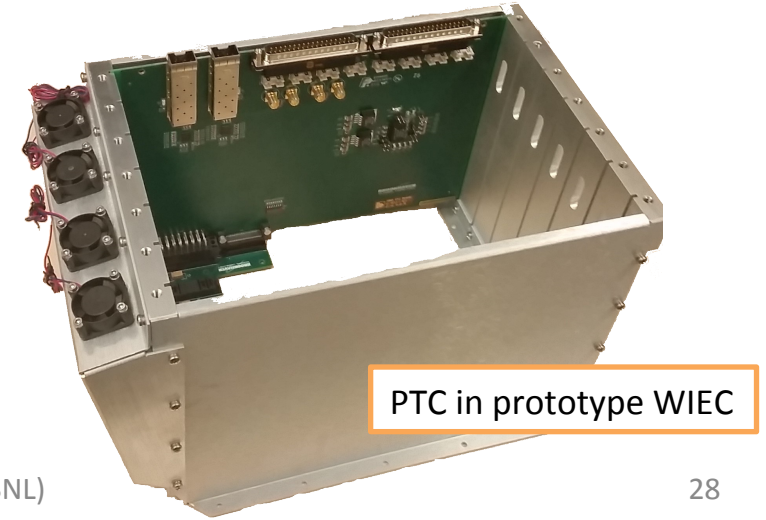


Prototype WIB teststand with one FEMB

PTC

- V2 PTC schematics, layout, and BOM in DUNE DocDB 2988 (UC Davis)
  - 2 variants for 2 options for 48/12V DC converters
    - V2-A: with Vicor "Cool Power" Pi3546
    - V2-B: with Linear Tech. LTM8064
- Current status
  - Integration/noise measurements ongoing with SBND WIB and V1 PTC at BNL
  - ProtoDUNE V1 PTC received and tested at BNL
  - V2 prototype order has been placed
- Production plan
  - Receive V2 PTC in 1 month
  - Test and select DC converter option
  - Place production order in mid June
    - 1 month lead time (fab and assembly)
  - Receive final PTC in mid July
  - 1 week for QC in integration test stand

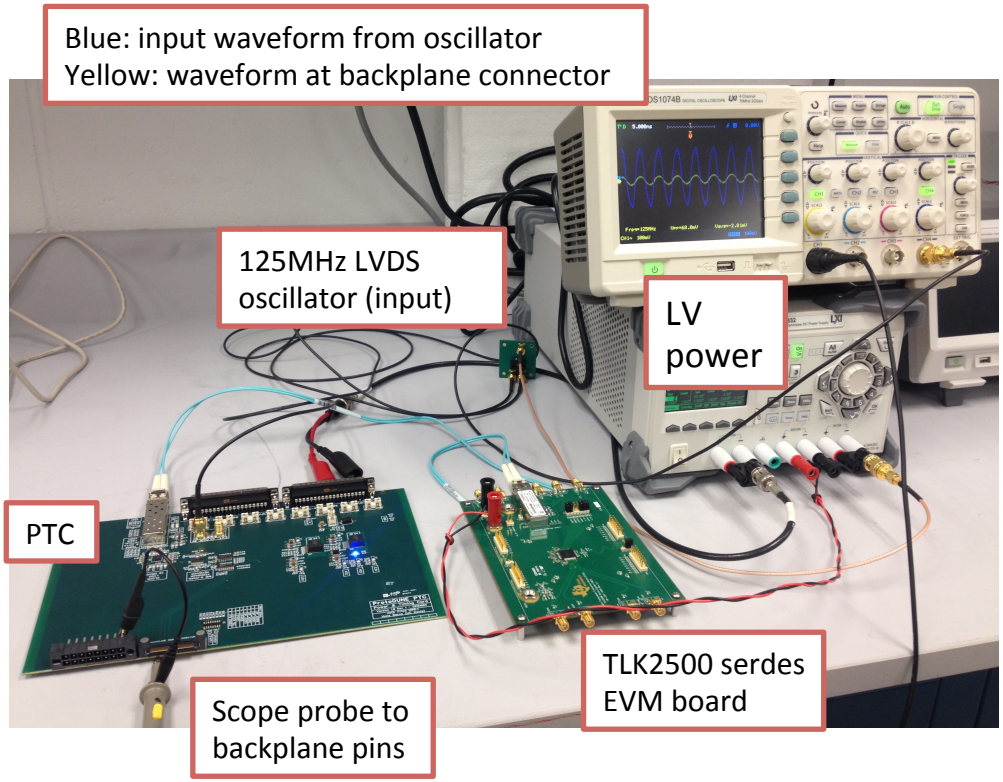




PTC QC Plan

- V2 PTC will ship to BNL from vendor
- 1 week for QC
  - Every PTC will be tested in the integration teststand
  - Criteria for acceptance
    - WIB receives clock from timing system and transmits return synchronization clock
    - 48V power is stepped down and delivered to WIB in crate with acceptable noise and crate temp remaining within manufacturer thresholds for components
- Production PTC ship to CERN in mid September
  - PTC packaged individually in anti-static bags

V1 PTC bench top evaluation

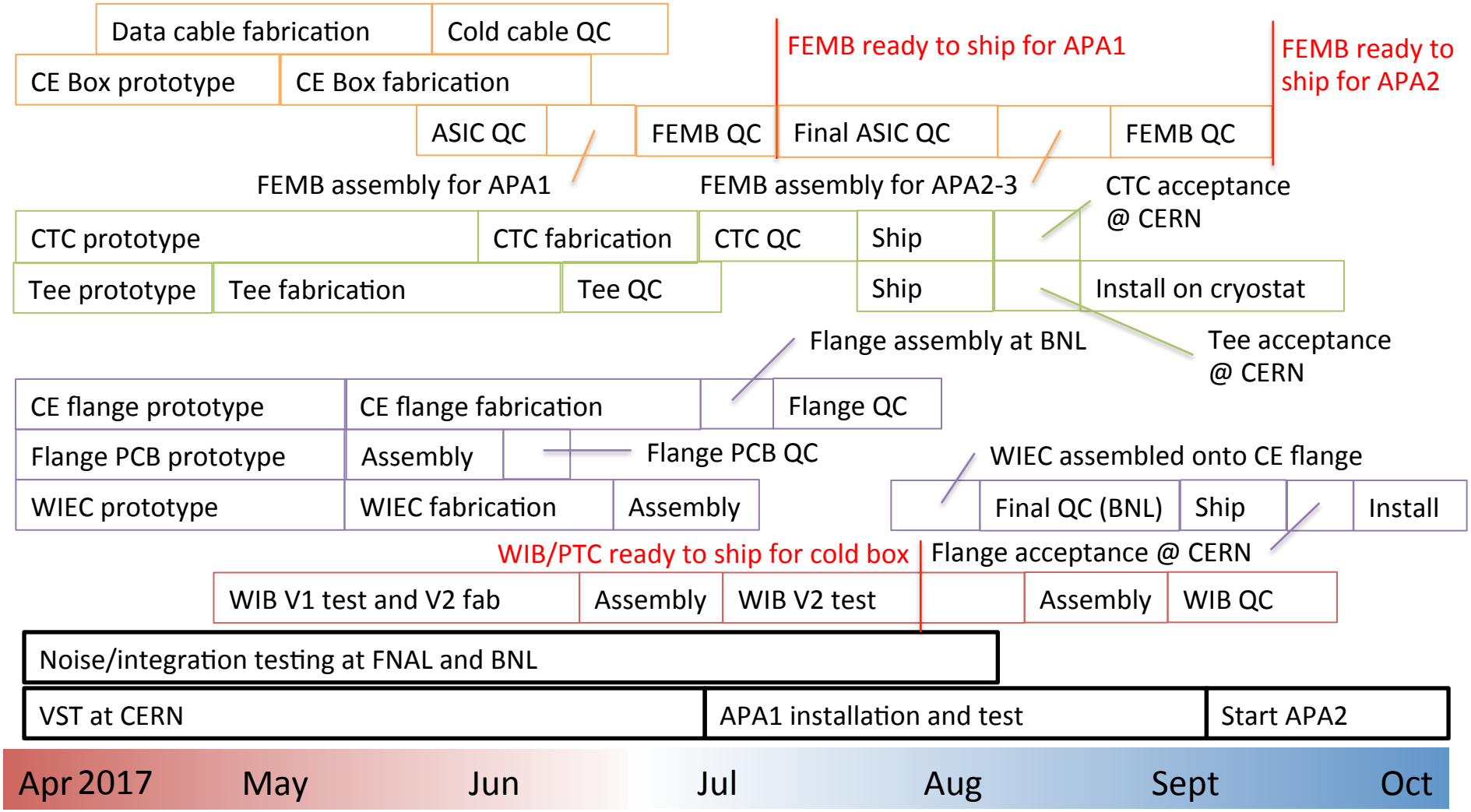


PTB

- PTB schematics, layout, and BOM in DUNE DocDB 3327
- Current status
  - Integration/noise measurements ongoing with SBND WIB and V1 PTC at BNL
- Production plan
  - Place production order in early June
    - 1 month lead time (fab and assembly)
  - Receive final PTB in early July
  - 1 week for QC to check backplane pins and connections
    - Visual inspection and electrical connectivity tested
- PTB will be assembled into CE flange/WIEC units in late July
  - Tested in the CE flange QC procedure
    - CE Mechanicals QC Plan DUNE DocDB 1809
  - CE flange units will remain assembled to ship to CERN in custom crates designed and built at BNL

CE installation (as of March 2017)
- APA1: 6/28
- APA2: 9/8
- APA3: 10/26

QC Schedule



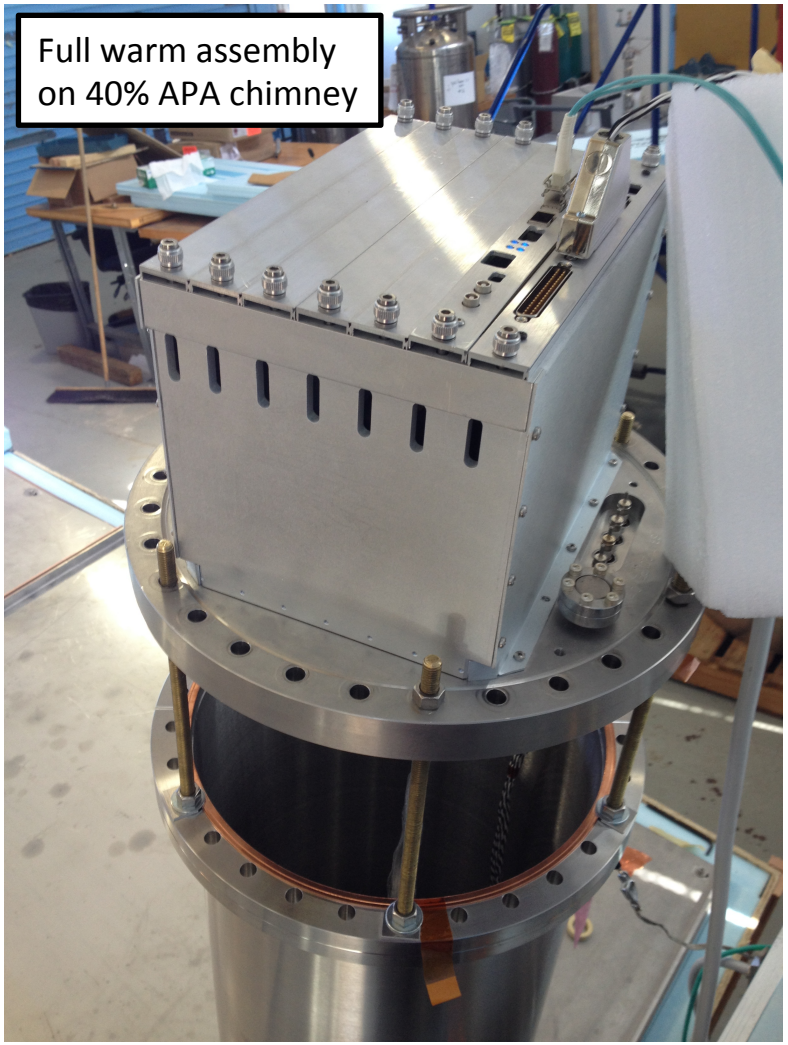
Labeling

- Each electronics unit will have a primary label for identification at CERN
  - FEMB: vendor will etch ID onto CE Box
    - ASICs and FEMB will have individual IDs for QC testing at BNL
    - Once installed in CE Box, box ID becomes the final label for QC tests and tracking
    - QC database will allow for reporting test results from box ID back to each individual ASIC
  - WIB: barcode attached to board, ID on front-panel
  - PTC: barcode attached to board, ID on front-panel
  - PTB: vendor will etch ID onto stainless steel flange
    - Flange PCB/WIEC/PTB will be QC tested on flange and follow flange ID
- All electronics will all be tracked by a hardcopy traveller
  - Receiving and assembly history
  - Sign off on QC results
- Cables will be labeled at each end after FEMB pass final QC tests
  - Once FEMB are installed on APA and cable routed, label at box end will be removed

Shipping to CERN

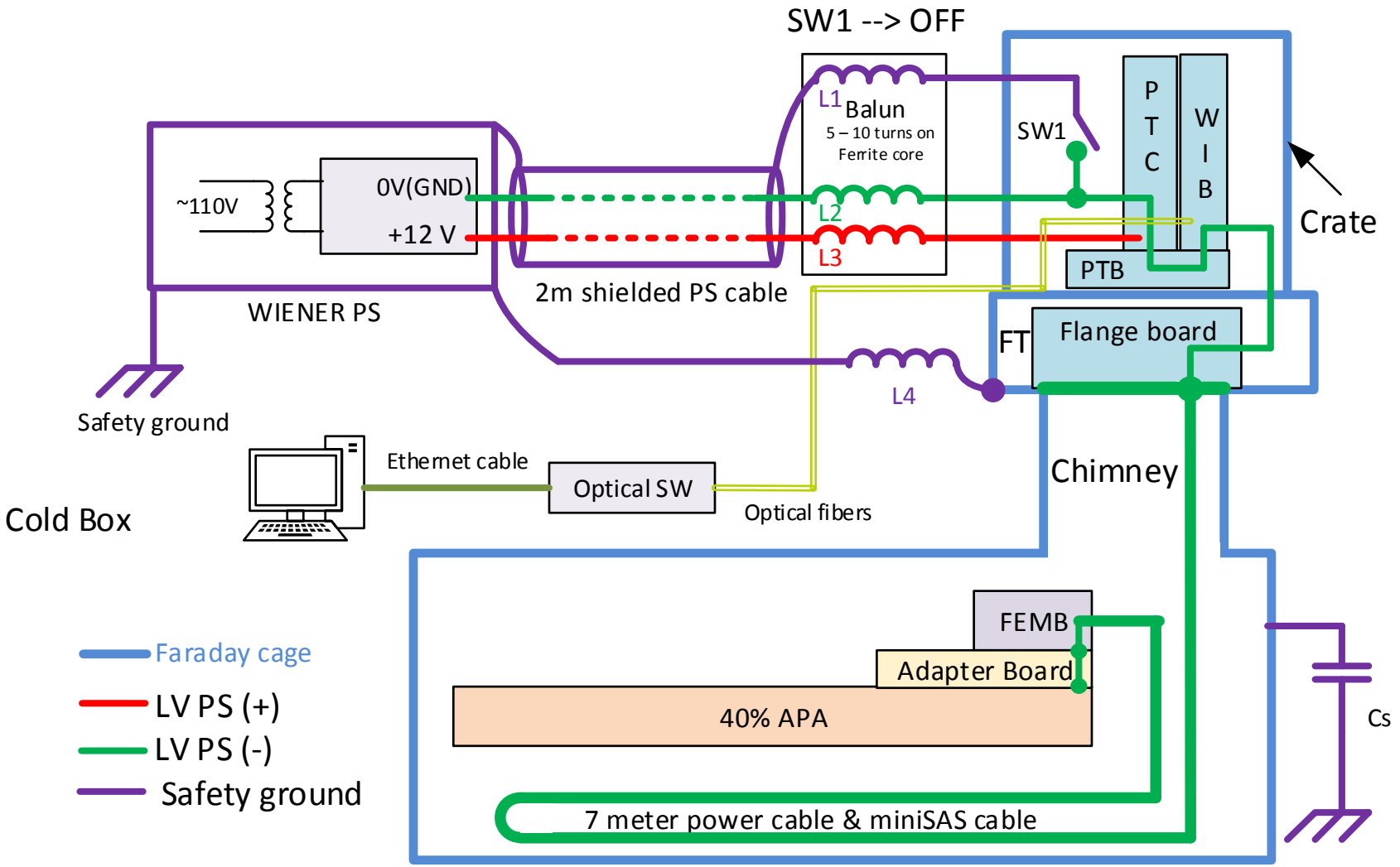
- Handled by Interfreight, an experienced broker, to CERN directly
  - Done for ATLAS LAr Calorimeter electronics for 10+ years
  - BNL rep will interact directly with Interfreight
- Custom packaging for all items will be designed and built by BNL team that installed MicroBooNE
  - FEMB/CE Box/PSL adapter will ship as unit
  - WIB and PTC will ship in individual boxes already available at BNL
  - CE flange/WIEC/PTB unit will ship as unit
- Electronics protection
  - Cables will be detached from FEMB prior to shipping
  - Shorting cards will be designed to protect electronics from ESD
    - Attached to the ends of the 7m cables during shipping and installation
  - All electronics shipped in anti-static bags
  - All electronics packed/unpacked using ESD straps

40% APA Integration Teststand



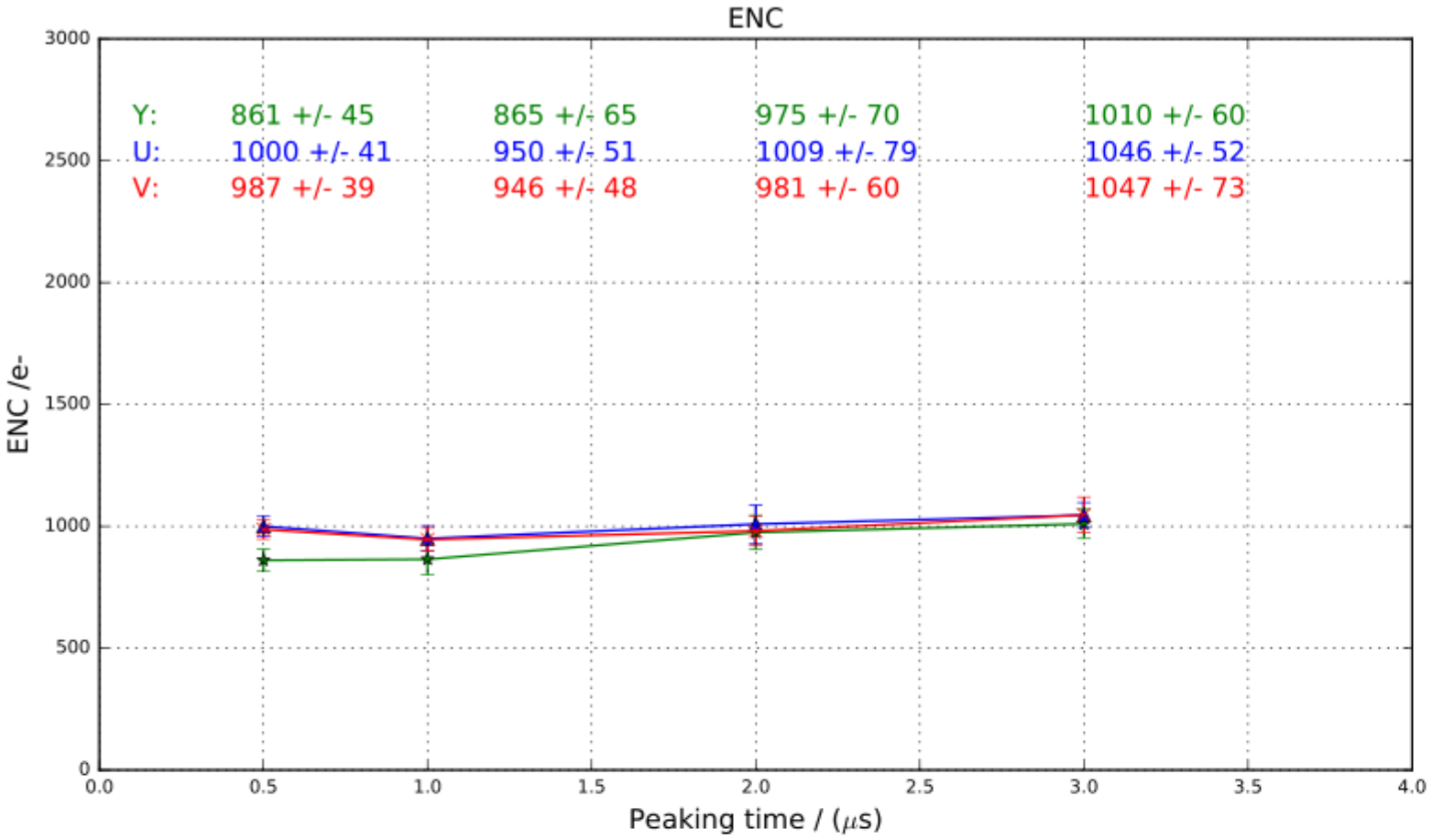
- 40% APA in cold box at BNL
- Full prototype CE system readout
  - WIB/PTC/PTB in WIEC
  - Wiener LV power supply delivering 12V to V1 PTC
  - V1 WIB readout via optical fiber to DAQ PC
    - Internal clock on WIB
  - Prototype CE flange
    - Purge port and SHV connectors on warm side
    - Flange PCB and squash plate on cold side
  - Cold LV and data 7m cable bundles to FEMB attached to APA wires
    - Maximum 4m wire length
- Grounding scheme for low noise performance has been developed
  - Data from LN2 cycle in next few weeks

Hi-Bay Grounding Scheme



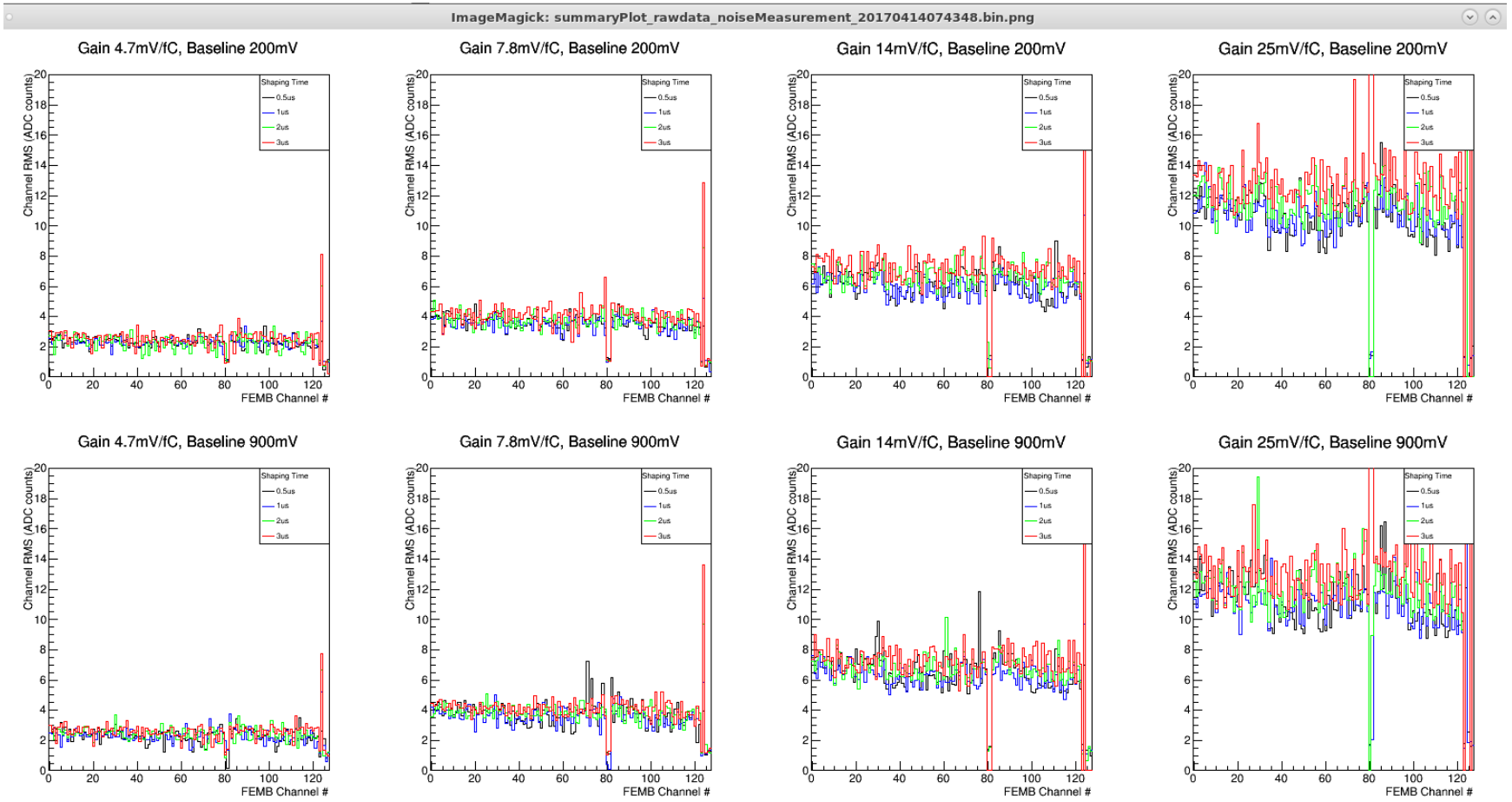
40% APA ENC performance

- Room temperature result with SBND FEMB



Screen Room RMS performance

- Similar result with SBND FEMB at RT in Fermilab Screen Room



Conclusions

- All electronics schematics and layout complete
  - Expect WIB V2 to be completed in next few weeks
- Final prototypes in process of being obtained
  - Will place orders for V2 WIB following review
- QC plan for production electronics in place
  - Results from QA on integration teststand indicate current design meets DUNE requirements
- Process for labeling and tracking being developed
  - Travellers will be part of QC database
- Plans for shipping and installing at CERN being developed
  - see CE Installation and QC, DUNE DocDB 3285
- Production orders can be placed to meet installation schedule