Cold Electronics QA/QC for ProtoDUNE-SP

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Contents

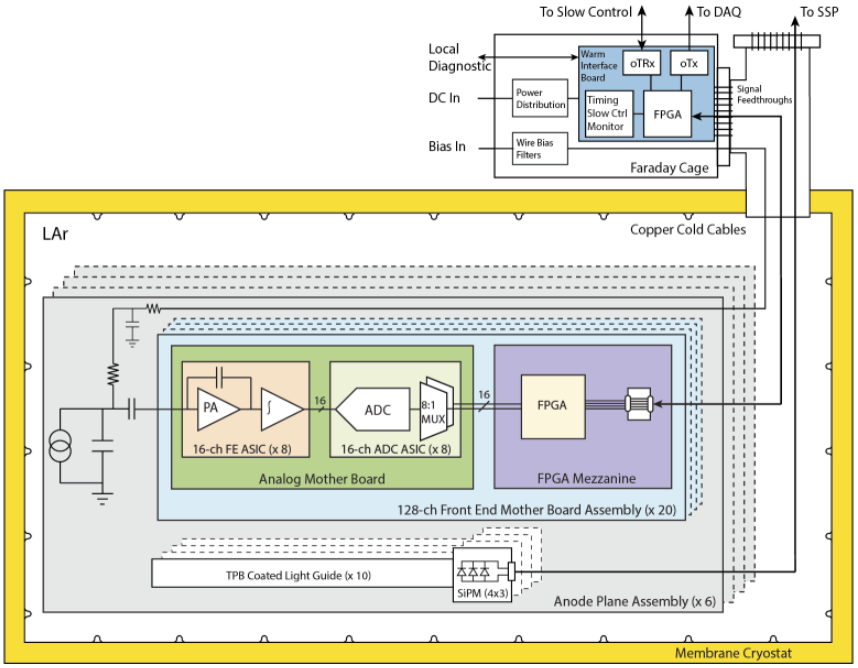

Figure 1: Overview of the ProtoDUNE-SP cold electronics readout system. Components for the ProtoDUNE-SP system are listed in Table 1.

1 Introduction

The Deep Underground Neutrino Experiment (DUNE) consists of a neutrino beam from the Fermilab accelerator complex to the Sanford Underground Research Facility (SURF) in South Dakota, a near detector at Fermilab, and four 10 kton fiducial volume Liquid Argon Time Projection Chamber (LArTPC) far detector modules approximately 1 mile underground at SURF [1] [2]. The ProtoDUNE Single Phase (SP) experiment is a ∼700 ton LArTPC detector which will be deployed at CERN in a test beam in 2018 [3]. ProtoDUNE-SP is a critical prototype for the first 10 kton DUNE far detector module.

Particles in the DUNE and ProtoDUNE-SP detectors are observed by drifting ionization electrons created by particle interactions in the active volume of the LArTPC from a cathode to anode-plane assemblies (APAs). Each APA contains wires which collect charge from the drift electrons, either by inducing a current on the wire as the electron drifts past, or collecting the electron charge directly on the wire. The charge signals on the wires are processed, digitized, and read out by the TPC cold electronics.

The ProtoDUNE-SP TPC cold electronics readout chain consists of the cold Front-End (FE) and ADC ASICs which are mounted on front-end motherboard (FEMB) assemblies, copper cold cable, warm flanges mounted on cryostat signal

Component	Description	Temp	QTY
FE ASIC	Wire charge amplification and shaping	LAr	960
ADC ASIC	Charge digitization and serialization	LAr	960
FEMB	8 FE and 8 ADC ASICs and transmission of data to CE flange; enclosed in CE Box	LAr	120
Cold cable bundles	12 twin-axial data lines/bundle; 18 twisted-pair LV wires/bundle	LAr/ room	120
Cold SHV cable	SHV coaxial cablel HV for wire-bias, FC termination and electron diverters	LAr/ room	48
Signal feed-through	Tee pipe with 3×14" Conflat flanges; internal cable support structure; GAr flow control	GAr	6
Warm flange	Connection between cold cable and warm electronics	room	6
WIB	Pass LV power and clock/control to the FEMB; pass data from FEMB to DAQ	room	30
PTC	Pass LV power and clock/control to the WIBs; return clock	room	6
PTB	LV power and clock/control distribution in WIEC	room	6
WIEC	Contains 1 PTC, 1 PTB, 5 WIBs/flange; provides Faraday shield and cooling	room	6

Table 1: Overview of the cold electronics system components.

feed-throughs, and warm interface electronics contained in a shielded Warm Interface Electronics Crate (WIEC), as shown for ProtoDUNE-SP in Figure 1. To ensure successful production and implementation of the cold electronics for both detectors, the electronics system design includes as few minor differences between each system as possible, as described in Table 1.

The TPC wire data from the cold electronics is transmitted on optical fiber from the warm interface electronics – Warm Interface Boards (WIBs) and Power and Timing Cards (PTC) – to each DAQ system: RCE or FELIX. The cold electronics transmits data continuously to the DAQ systems, where the data is buffered and any compression and trigger decisions are applied.

2 Front-End ASIC

The analog FE ASIC, the pre-amplifier of which is the first element in the TPC readout, shown in Figure 2, reads out 16 independently-configurable channels with a charge amplifier with a gain selectable from one of 4.7, 7.8, 14 and

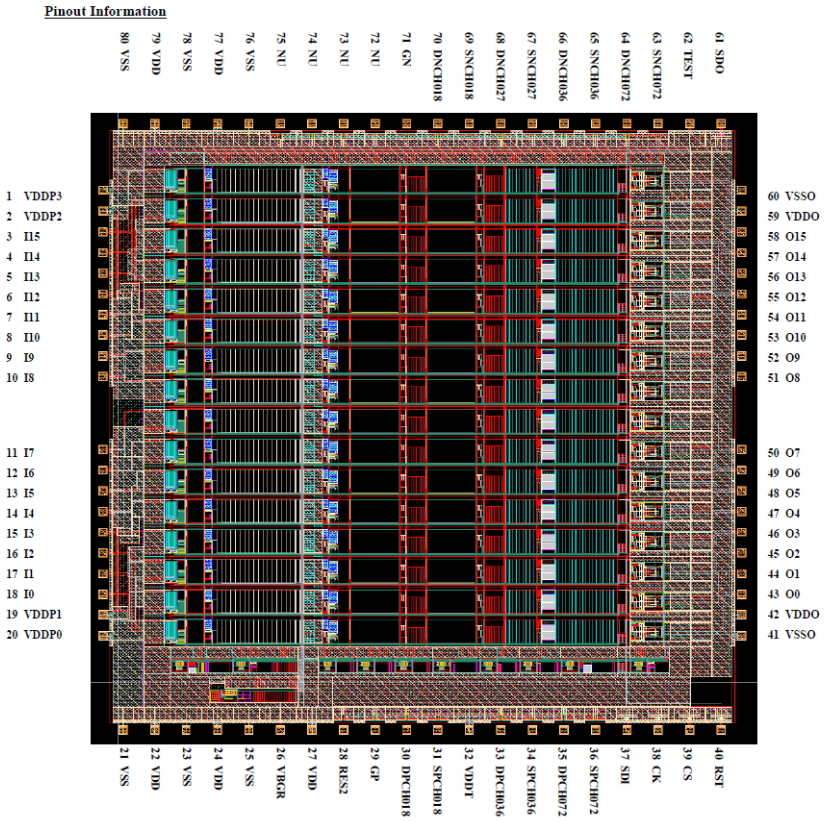

Figure 2: Pin mapping for the analog FE ASIC. The pin definitions are given in [4].

Parameter	Values	# of test cycles	Channel/ Global
Gain	4.7, 7.8, 14 and 25 mV/fC	4	CH
Filter peaking time	0.5, 1, 2, and 3 μs	4	CH
Baseline	200/900 mV	2	CH
Test capacitor	enable/disable	2	CH
Coupling	AC/DC	2	CH
Buffer	enable/disable	2	CH
Channel 1 setting	signal/monitor monitor = temperature or bandgap	3	GL
Leakage current	0.1, 0.5, 1.0, 5.0 nAmp	4	GL
Analog out	enable/disable	16	CH

Table 2: Summary of P2 FE ASIC parameter test cycles.

25 mV/fC (full scale charge of 55, 100, 180 and 300 fC), a high-order anti-aliasing filter with adjustable time constant (peaking time 0.5, 1, 2, and 3 μs), an option to enable AC coupling, and a baseline adjustment for operation with either the collecting (200 mV) or the non-collecting (900 mV) wires [4]. The FE ASIC is fabricated in a commercial CMOS process (0.18 μm and 1.8V), as described in detail in [5].

2.1 Quality Assurance

The V4* version of this chip has been implemented in LAr by Michigan State University (MSU) for Long-Bo and the LArIAT LArTPC, and by Brookhaven National Laboratory (BNL) for the MicroBooNE LArTPC [6] and the 35ton LArTPC prototype detector at Fermi National Laboratory (Fermilab) [7]. The experience gained through operation of the FE ASIC in these applications has been fed-back into the production of prototypes for DUNE and is guiding the Quality Assurance (QA) evaluation of them. The FE ASIC channels of analog charge amplifier and filter are controlled by six channel-specific parameters (gain, filter, baseline, test-input capacitor, coupling, buffer), three global parameters (leakage current, monitor temperature/bandgap (channel 1 only), high-filter (channel 16 only)) and a DAC controlled onboard pulser, all set by registers loaded via serial communication.

To ensure high-quality performance of the FE ASIC prior to production in 2017, QA will test the FE ASIC both warm and cold. The operation of the channel specific parameters will be tested: gains (4), filter peaking times (4), collection/induction baselines, test-capacitance enable/disable, and the DC or AC coupling with its buffer on or off. Also tested will be the global parameters: channel 1 signal or monitor, monitor band-gap or temperature, and leakage

current values (4 tests), as summarized in Table 2. The test capacitance enable will be cycled (2 tests) and when enabled, all combinations of gain, peaking time, and baseline will be cycled with all channels active (32 tests), and with a single setting of gain and peaking time with one channel at a time (16 tests) for a cross-talk measurement. The other parameters will be tested with a typical gain and peaking time (4 tests).

While some testing of the onboard pulser will be included to verify performance of the pulser for *in situ* detector calibration during detector commissioning and operation, the QA testing will use an external pulse generator with control of amplitude, rise/fall time, and pulse width. Experience has indicated that other areas will demand close attention during QA evaluation of prototypes: the sensitivity of the serial communications to a noise source, stability of the analog operation following a large or wide input signals with various gains, and characteristics of the baseline restoration with various gains. With each test taking about 5 seconds, the full characterization of the prototype chips can be completed in about 10 minutes per ASIC. The design of the cryostat is aiming at a warm/cold/warm cycle to take only a few minutes.

In collaboration with BNL, MSU is building test facilities for the QA evaluation of prototype FE ASIC chips at room temperature and at 77K. These will employ an inexpensive commercial ADC on each channel. These facilities can be duplicated, in particular for the QC stage of the final FE ASIC chips produced for the protoDUNE-SP APAs. The key element in performing QA is implementing a Cryogenic Test System (CTS) that will enable the cold testing of a large number of chips in a short period of time while avoiding physical damage in handling and preventing at all times the formation of water condensation on the chips or cryostat.

The chips are small, 1.4×1.4 cm^2 and can be held in a clamp 3.2×5 cm^2 that has been shown to maintain contact with the surface mount pins at 77K. The clamp is mounted on a printed circuit board that brings all communication lines outside a foam cryostat's walls that enclose the clamp from above and below the circuit board, with liquid Nitrogen (LN2) entering and leaving the cryostat via inlet/outlet and vent pipes into the lower half of the foam cryostat, as shown conceptually in Figure 3. The circuit board and lower half of the cryostat will be fixed with only the upper half removable and with flexible gaskets making the liquid seal. Heater strips are mounted on the circuit board at the outer circumference of the foam to maintain the outer portion of the seals at room temperature. The warming and cooling cycles may be sufficient to keep the outer surface of the cryostat from reaching the dew point temperature, or surface heaters can be included.

A working prototype has been developed at MSU and demonstrated at BNL and is shown in Figure 4.

2.2 Quality Control

The Quality Control (QC) to validate the FE ASICs for production components requires a rigorous test procedure. Once the QA teststands at MSU and BNL

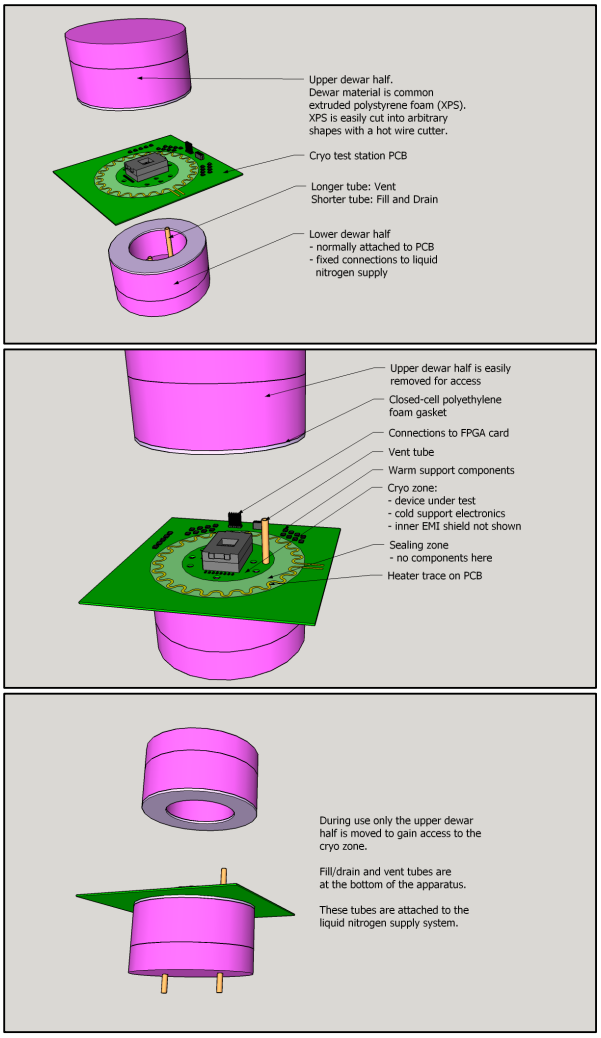

Figure 3: Three views of a conceptual design for a QA/QC CTS for the FE ASIC, a) three sections identified, b) PC board details, c) underside showing fill and vent tube connections.

Figure 4: Prototype Cryogenic Testing System (CTS) developed at MSU.

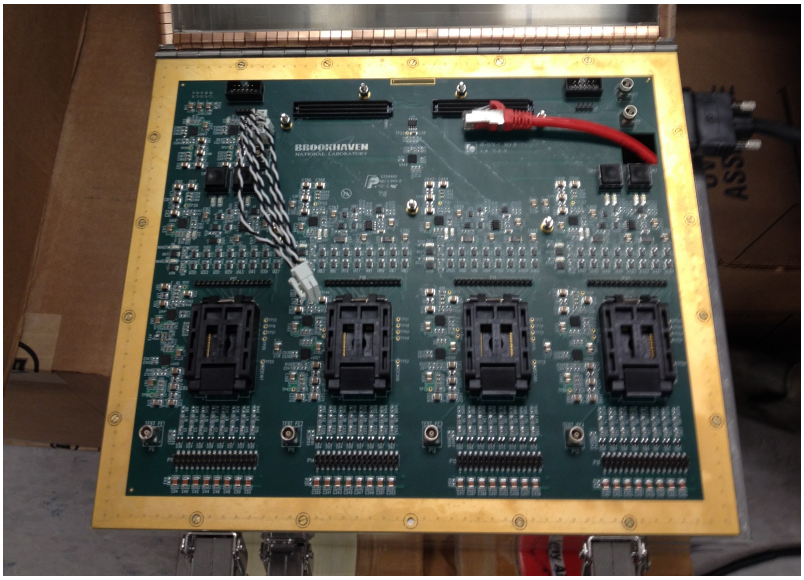

Figure 5: Quad-socket FE ASIC testboard without FPGA mezzanine. An FPGA mezzanine is attached to the testboard for readout and control.

have been fully developed, production versions will be installed at BNL for final validation. In order to meet the aggressive schedule for ProtoDUNE-SP discussed in Section 8, all final validation will take place at BNL, with test stand operators working in shifts under the supervision of a QC leader. The shifters will run the teststands with a version controlled revision of the QC software and database outlined in Section 7.1.

Since the V4* version, two prototype cycles, P1 and P2, have been designed, fabricated, and tested. The production FE ASICs for ProtoDUNE-SP are the P2 FE version. All production FE ASICs will be tested at room temperature. A cryogenic yield test of approximately 10% of the ASICs will be tested submerged in LN2, due to the short time available for QC. If the result of the cryogenic yield test is sufficiently high (order $<$ 1%), all ASICs which pass the room temperature validation tests will be assembled onto FEMBs.

Approximately twice as many FE ASICs as needed for the final detector will be fabricated in the final production. Therefore, a failure rate at 77K can be tolerated up to $\sim$ 50%; if the yield test results in sufficiently high cryogenic failure (order 10%), it will become more efficient to test all ASICs cold before assembling onto FEMBs. The FEMB QC procedure includes tests of all ASIC functionality under multiple thermal cycles to cryogenic temperature, as described in Section 4.3; therefore, all production ASICs will be tested multiple times before installation into the ProtoDUNE-SP cryostat.

As discussed in Section 2.1, a full characterization of one chip includes all of the test cycles summarized in Table 2, plus a cross-talk measurement and

validation of internal FE ASIC pulser functionality. This characterization will be the baseline for each FE ASIC validation test, with the test data and results from each cycle saved in the QC database and a pass/fail determination reported by the test software to the test shifter.

QA tests show this takes approximately 10 min, with an estimated extra 5 min each for cool down and warm up for a cryogenic cycle. The current design of the FE ASIC testboard, which reads out 4 FE ASICs via commercial ADCs and is controlled and configured by an FPGA assembled on a separate mezzanine board is shown in Figure 5. With this testboard, 4 FE ASICs can be tested at room temperature in ∼10 min, and then again at 77K in another ∼20 min.

The ProtoDUNE-SP QC testing will need to validate several thousand production FE ASICs, as listed in Table 1 and including $> 40\%$ spare chips. This will require an estimated 200 hours of room temperature testing with another ∼20 hours of cryogenic testing. For two shifters working 8 hours/day, this will require an estimated 4 weeks of work to finish the FE ASIC QC. The production FE ASICs were ordered from Taiwan Semiconductor Manufacturing Company, Limited (TSMC) via the MOSIS Service and are expected to be packaged by MOSIS/ASE and delivered to BNL in late June. They will be tested in batches to allow for several rounds of assembling onto FEMB to match the staged ProtoDUNE-SP APA delivery schedule.

3 ADC ASIC

The ADC ASIC, shown in Figure 6, contains an ADC block which digitizes 16 channels with 12-bit resolution at up to 2 MS/s sampling rate, and a built-in FIFO block 192 bits wide (16 x 12) and 32 bits deep with two 8:1 or one 16:1 multiplexed serial LVDS outputs [8]. The operating input range of the ADC ASIC channels is ∼0.2-1.6 Volts, for an approximate conversion factor of ∼0.34 mV/count. Like the FE ASIC, the ADC ASIC is fabricated in a commercial CMOS process (0.18 μm and 1.8V), as described in detail in [5].

3.1 Qualtiy Assurance

The V6 version of this chip has been implemented in LAr by BNL for the 35ton detector at Fermilab [7]. The experience gained through operation of the ADC ASIC in these applications has been fed-back into the production of prototypes for DUNE and is guiding the QA evaluation of them. Since the V6 version, two prototype cycles, V* and P1, have been designed, fabricated, and tested. The QA of the V* and P1 versions revealed several issues as described in detail in [9]:

- **Stuck code** An instability results in an accumulation of ADC counts populating the least significant six bits of the ADC, with values pulled out of nearby counts and encoded as xxxxxx000000 or xxxxxx111111. This

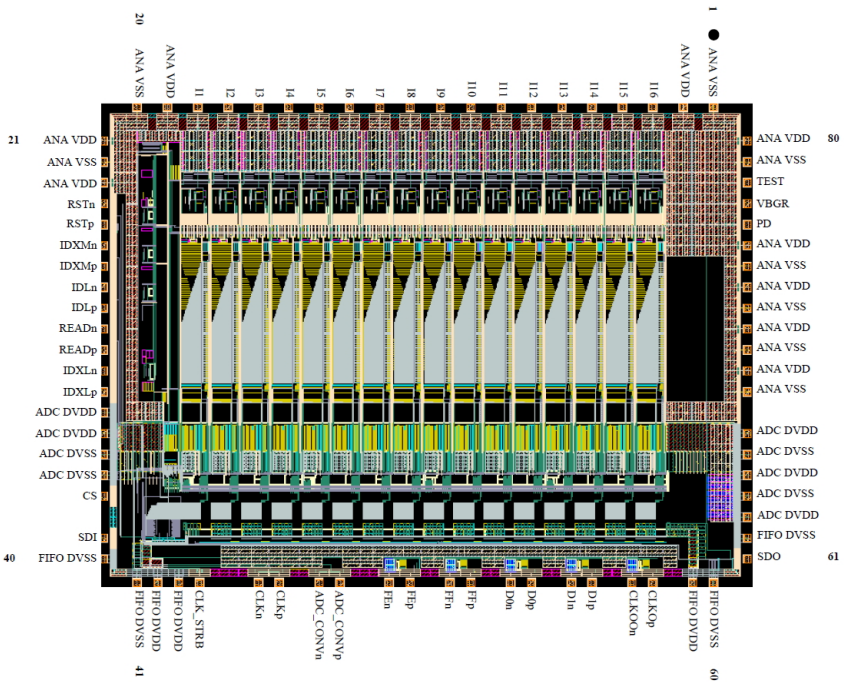

Figure 6: Pin mapping for the ADC ASIC. The pin definitions are given in [8].

Source	Values/Test	# of test cycles
Digitize clock	external 1.0 and 2.0 MHz internal	4
FE ASIC	multiple FE ASIC settings normal operation of ADC	32
External ramp	Stuck code, saturation, roll-back, & linearity	1

Table 3: Summary of ADC ASIC parameter test cycles.

results in an differential non-linearity in the ADC. This effect has been shown at some level in all channels of the V6, V* and P1 ADCs, both in warm and at a higher level in cold.

- **Early saturation** The V* ADC saturated before reaching the end of the dynamic range at 4096 counts. This effect is more severe in cold where about 50% of the channels saturate at values as low as 3200 counts.
- **Rollback** Additionally for V*, a rollback effect may occur where the ADC counts start decreasing after saturation. This effect has been shown to depend on the ADC conversion time.

The outcome of these effects is an ADC which is not uni-valued. The measurement of all three effects is done with a high-precision ramp pulser injecting voltage over the dynamic range of the ADC. The linearity of the ADC in mV/count is measured with a step voltage pulser over the dynamic range of the ADC, as summarized in Table 3.

To ensure high-quality performance of the ADC ASIC prior to production in 2017, QA will test the ADC ASIC both warm and cold. The operation of the digitize clock source (external or 0.5, 1.0, and 2.0 MHz interal) is tested (4) with multiple input source types: FE ASIC and external ramp pulser, as summarized in Table 3. This QA regimen, undertaken at BNL, has shown that the V* early saturation and rollback effects have been fixed in the P1 ADC version. However, the stuck code issue remains. The QA testing has also identified the preferred operational mode for the P1 ADC ASIC, with the full steering current (the ADC has an internal option selectable between full and partial current) and external control clocks.

3.2 Quality Control

The QC to validate the ADC ASICs for production components requires a rigorous test procedure. The ADC ASIC QC will be very similar to the FE ASIC QC described in Section 2.2, with production versions of the QA teststands at BNL for all final validation and test stand operators working in shifts under the supervision of a QC leader.

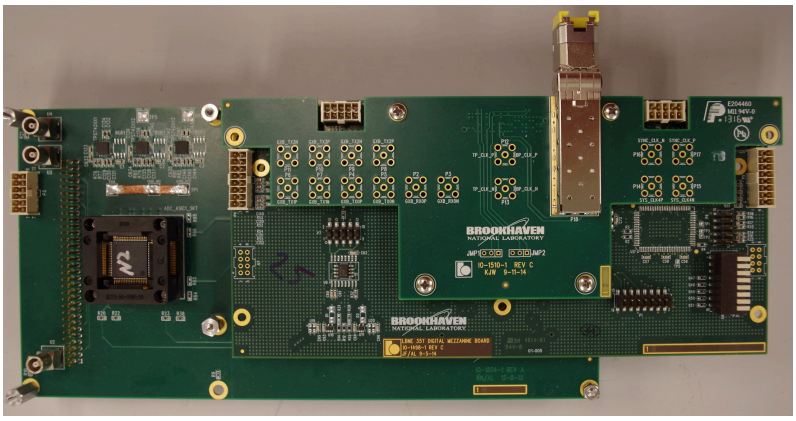

Figure 7: Single chip ADC ASIC testboard with FPGA mezzanine. A four ASIC testboard is under design.

Although the stuck code is a known design issue, because of the tight protoDUNE schedule described in Section 8, the production ADC ASICs for ProtoDUNE-SP are the P1 ADC version. To screen out ADCs with the highest fraction of stuck codes, which are observed at a higher level in LN2 than RT, all production ADC ASICs will be tested at room temperature and LN2 prior to assembly onto FEMBs.

The final FEMB QC procedure includes tests of all ASIC functionality under multiple thermal cycles to cryogenic temperature; therefore, as with the FE ASIC, all production ADC ASICs assembled onto FEMB will be tested multiple times before installation into the ProtoDUNE-SP cryostat.

As discussed in Section 3.1, a full characterization of one chip includes all of the test cycles summarized in Table 3. This characterization will be the baseline for each ADC ASIC validation test, with the test data and results from each cycle saved in the QC database and a pass/fail determination reported by the test software to the shifter.

QA tests on the prototype ADC testboard at BNL show this takes approximately 10 min, with an estimated extra 5 min each for cool down and warm up for a cryogenic cycle, assuming a similar technique is used as described for the FE ASIC in Section 2.1. The current design of the ADC ASIC testboard, which reads out one ADC with an external pulser input and is controlled and configured by an FPGA assembled on a separate mezzanine board is shown in Figure 7. A design of a four ADC testboard is ongoing at BNL. With this testboard, 4 ADC ASICs can be tested at room temperature in ∼10 min, and then again at 77K in another ∼20 min.

The ProtoDUNE-SP QC testing will need to validate several thousand production ADC ASICs, as listed in Table 1 and including $> 40\%$ spare chips. This will require an estimated 100 hours of room temperature testing with another ∼200 hours of cryogenic testing. For two shifters working 8 hours/day, this will

require an estimated 6 weeks of work to finish the ADC ASIC QC. The production ADC ASICs were ordered from TSMC via the MOSIS Service and are expected to be packaged by MOSIS/ASE and delivered to BNL in late June. They will be tested in batches to allow for several rounds of assembling onto FEMB to match the staged ProtoDUNE-SP APA delivery schedule.

4 FEMB

The FEMB consists of an analog motherboard, shown in Figure 8, and FPGA mezzanine board, shown in Figure 9. Each analog motherboard contains 8 FE and 8 ADC ASICs, which provide 128 channels of digitized wire readout. The FEMB schematics, board layout, and Bill of Materials (BOM) are in DUNE DocDB 1419 [10].

The FEMB will be contained in CE Boxes that provide protection and cable strain relief when installed on the APA. The FEMB and CE Box assembly attaches to the capacitor-resistor (CR) board on the APA via an adapter board designed by PSL, as described in detail in the *Cold Electronics QA/QC Mechanicals Plan* [11]. The FEMB then connects to the warm interface electronics at the flange via two bundles of cold copper cable: one for LV power and one for data/clock/control/JTAG.

The FPGA is emulating the activity of 2 COLDATA ASICs which are being developed for low-power consumption in the LAr for the DUNE far detectors, but which will not be ready on the ProtoDUNE-SP schedule. The FPGA receives the clock and control IO from the WIB, configures the FE and ADC ASICs, and transmits the digitized wire data over 4 $\sim$1 Gbps serial links to the WIB, as described in detail in [12].

In addition to the FPGA and ASICs, the FEMB contains an onboard flash EEPROM to load the FPGA firmware upon power up. It also allows for backup JTAG programming in case the EEPROM fails to both the FPGA and EEPROM. It contains onboard crystal oscillator chips to supply a backup clock to the FPGA state machine in case the system clock from the warm electronics is lost. Power to all ASICs, including the bias voltage to the input to the FE ASIC pre-amplifier, is provided by onboard cold linear regulator (CLR) chips. The FE ASIC also contains a test capacitor that enables a connection to the input of the pre-amplifier allowing injecting a test charge either from the FE ASIC itself, the FPGA, or an external pulser.

4.1 Functionality

To validate the functionality requires testing the following features of the FEMB both at room temperature and under multiple thermal cycles in LN2:

- successful loading of the FPGA programming from the onboard EEPROM;
- ability to program the FPGA and EEPROM over the backup JTAG links in the cold data cable bundle;

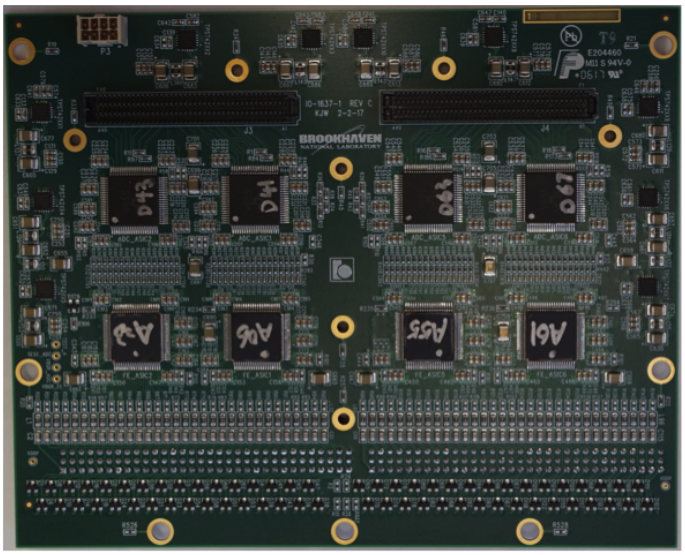

Figure 8: FEMB analog motherboard. 4 FE and 4 ADC ASICs are shown on the top of the motherboard; additionally 4 FE and 4 ADC ASICs are mounted on the motherboard bottom.

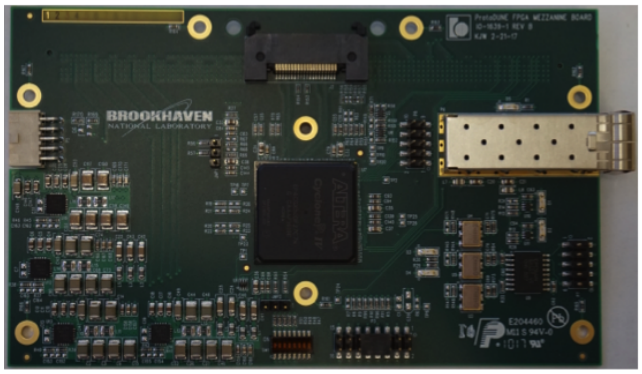

Figure 9: FEMB FPGA mezzanine card, which mounts directly on top of analog motherboard.

- ability to set the control registers on the FPGA via the I^2C control IO links;
- confirmation that the backup onboard oscillators can generate the clock for the FPGA state machine in case the clock from the system is lost;
- confirmation that the FPGA can configure all 16 ASICs on the analog motherboard via SPI interface and synchronize the data from all serial links from the ADCs (either 16:1 or 8:1 multiplexing on each ADC ASIC);
- verify that in the state with all ASICs configured, the current drawn by the CLR for all LV power inputs are nominal, indicating the FPGA is programmed and ASICs operational;
- confirmation that all channels observe both the FPGA internal pulser and an external pulser with the FE test capacitor enabled;
- confirmation that all channels observe the FE ASCI internal pulser;
- successful transmission of all digitized waveform data over all 4 ∼1.2 Gbps links at sufficiently low Bit Error Rate (BER).

In addition to validating all of the FEMB functionality, each FEMB must have its dead or bad channels entered in the QC database. Dead/bad channels that are a result of single ASIC failures will be mitigated by testing all ASICs prior to assembly onto FEMBs, and replacement on the FEMB if a failure is identified after assembly. Single bad channels will have to be identified on the FEMB QC teststand as channels that fail a set of cuts that will be developed as prototype FEMB are tested on the QA test bench.

Cuts that will used to quantify "bad" channels, some of which were implemented during QC tests for the 35ton detector, which read out 2048 channels of digitized wire charge over 4 APAs with 16 128-channel FEMBs (4/APA), are given in Table 4 [13]. For the 35ton prototype, cuts were made on minimum and manxiumum channel pedestal to ensure uniformity, pedestal RMS to remove noisy channels, pulser RMS to identify channels unresponsive to the internal FPGA calibration pulser, and average pulse height to ensure uniform response to the calibration pulser; the number of channels identified by these requirements are given in Table 4.

For the 35ton detector, no requirements were placed on ADC linearity. Figure 10 shows an ADC linearity fit for a recent revision of the ADC ASIC in Volts as a function of FPGA input calibration DAC value. For all ProtoDUNE-SP channels, cuts will be used to quantify the ADC performance on the linearity fit value and χ^2 of the fit, as shown in Table 4.

4.2 Noise

To ensure that each FEMB satisfies the per-channel Equivalent Noise Charge (ENC) requirement specified in [14] of ENC < 650 e^- at LAr temperatures

Quantity	Requirement Cut	% bad 35t channels
Pedestal (Ped^{ADC})	$Ped^{ADC} > \overline{Ped^{ADC}_{allchan}} - 4.2\sigma(Ped^{ADC}_{allchan})$ $Ped^{ADC} < 4.2\sigma(Ped^{ADC}_{allchan}) + \overline{Ped^{ADC}_{allchan}}$ where $\sigma(Ped^{ADC}_{allchan}) \sim$ 35 ADC counts	2.5%
Pedestal RMS (RMS^{ADC}_{ped})	$RMS^{ADC}_{ped} <$ 20 ADC counts	0.3%
Pulser RMS (RMS^{ADC}_{pulse})	$60 < RMS^{ADC}_{pulse} <$ 120 ADC counts	0.7%
Pulse height (Pul^{ADC})	$\overline{Pul^{ADC}} >$ 400 ADC counts	0.05%
		3.6% total
ADC linearity (ADC_{fit})	$ADC^{maximum}_{fit} > ADC_{fit} > ADC^{minimum}_{fit}$	NA
ADC χ^2	ADC χ^2/NDF $< \chi^2$/NDF$\times\sigma_{ADC}$	NA

Table 4: Bad channel cuts to be studied during FEMB QA and cut parameters fixed for final QC validation.

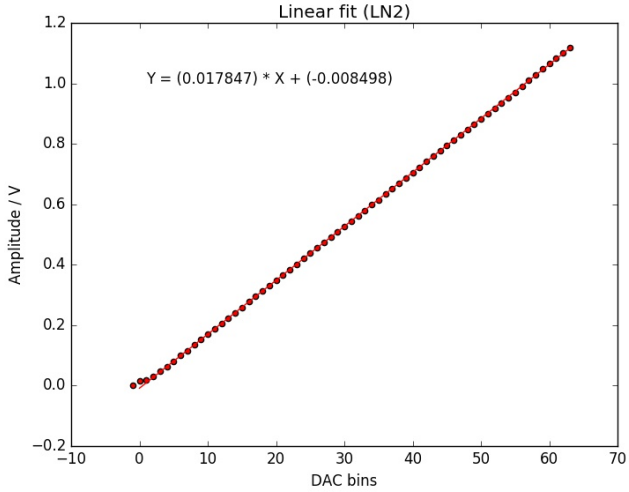

Figure 10: ADC value in Volts as a function of FPGA calibration pulse DAC value.

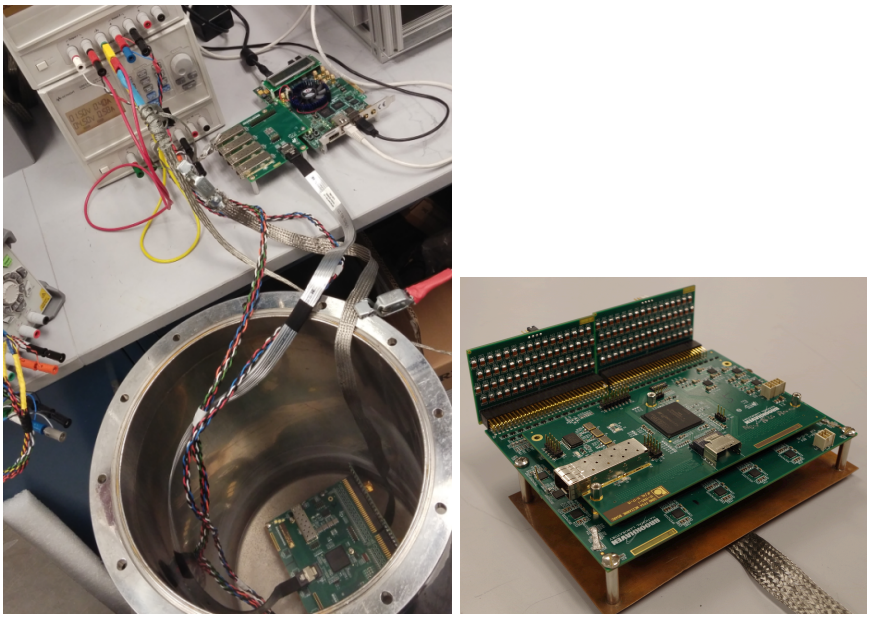

Figure 11: Left: FEMB teststand with shielded Dewar. Right: FEMB with toy TPC capacitance board attached.

requires testing with an equivalent wire capacitance in a shielded Dewar with well understood grounding and shielding. A prototype teststand for FEMB noise testing has been developed at BNL and is shown in Figure 11.

To measure the ENC as if the input pre-amplifier of each FE ASIC channel on the FEMB was connected to an APA wire, and "toy TPC" capacitance board is connected to the input pins of the FEMB, as shown in Figure 11. The toy TPC allows simulation of wire capacitance at both room temperature and 77K tests. For the current QA, the toy TPC provides 150 pF input capacitance per channel, which corresponds to the wire length and spacing expected in the DUNE far detector modules. The result of noise QA tests with the latest version of the ProtoDUNE-SP prototype FEMB is shown in Figure 12: it shows average noise in ENC (e^-) over all channels as a function of FE filter peaking time at 25 mV/fC gain and 150 pF input capacitance at both room and cryogenic temperatures.

The current prototype ProtoDUNE-SP FEMB are expected to have identical response to noise with a toy TPC simulating wire capacitance. Therefore, we expect all FEMB to observe ENC < 650 e^- at LAr temperatures for all filter peaking times; this result has been observed at all FE gain settings.

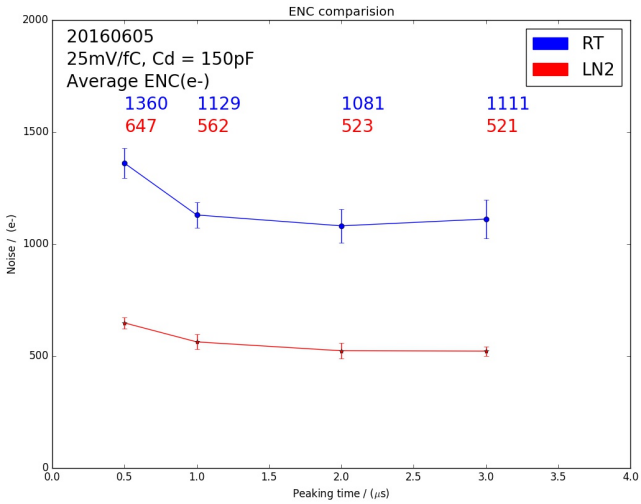

Figure 12: Average noise in ENC (e^-) over all channels for a prototype ProtoDUNE-SP FEMB as a function of FE filter peaking time at 25 mV/fC gain and 150 pF input capacitance at both room temperature (RT) and in liquid Nitrogen (LN2).

4.3 QC

Since the 35ton FEMB version, two major prototype cycles of the FEMB have been designed, fabricated, and tested: the P1 "SBND" version, which was designed with P1 FE and V* ADC ASICs, and the P2 version, which was designed with P2 FE and P1 ADC ASICs. The P2 FEMB will be the final production version for ProtoDUNE-SP.

Production versions of the QA teststands shown in Figure 11 will be installed at BNL for all final FEMB validation, operated by test stand shifters working under the supervision of a QC leader. All production FEMBs will be tested under multiple thermal cycles between room temperature and 77K.

Based on QA tests for the prototype FEMB, and the QC validation conducted for the 35ton FEMB, full characterization of one board therefore includes: a full verification of the FEMB functionality as described in Section 4.1; the FE ASIC test cycles summarized in Table 2; the ADC ASIC test cycles summarized in Table 3; and finally a noise measurement on all channels of ENC$<$ 650 e^- at LN2 temperatures for all filter peaking times. This characterization will be the baseline for each FEMB validation test, with the test data and results from each cycle saved in the QC database and a pass/fail determination reported by the test software to the shifter. Bad channels that do not disqualify a FEMB from installation, as determined by the requirement cuts under study in Table 4 will also be saved in the QC database.

FEMB QC will proceed in 2 stages. The first will be a full suite of the characterization tests with a bare FEMB at room and LN2 temperature. This will allow for easy rework and/or replacement of components which fail at cryogenic temperature. FEMB which pass the first round of QC will be "dressed" at BNL into a CE Box with cold cable and PSL adapter board attached. The second stage will be the dressed FEMB repeating a complete suite of the characterization tests and both room and LN2 temperature. Additionally, each FEMB/CE Box/adapter unit will be inspected for loose hardware or evidence of stress to the FEMB PCB after each thermal cycle in LN2.

QA tests on the prototype FEMB teststand at BNL show that a full validation takes approximately 30 min, with an estimated extra 5 min each for cool down and warm up for a cryogenic cycle. The ProtoDUNE-SP QC testing will need to validate 150 production FEMB, as listed in Table 1 and including 25% spare boards. This will require an estimated 130 hours of room temperature testing with another ∼520 hours of cryogenic testing, assuming each FEMB is fully thermal cycled an average of three times. For two shifters working 8 hours/day, this will require an estimated 2 months of work to finish the FEMB QC. The ProtoDUNE-SP schedule described in Section 8 budgets ∼2.5 months for QC validation of the production FEMB. If necessary, the rate of testing can be increased by adding shifters and teststands.

4.4 Production

Three P2 FEMB are undergoing QA testing at BNL. Once the FEMB are validated, 25-30 more FEMB will be assembled from already existing PCB with FE and ADC ASICs expected to arrive at BNL in mid-May. These FEMB are scheduled to install on APA1. The remaining production of 150 FEMB AM and FM PCB will also be ordered. When the full production ASICs are tested at BNL in July and August, they will be assembled in batches onto the final FEMB PCB. All FEMB assembly will be done by an experienced vendor local to BNL who has assembled the prototype FEMB.

FEMB units with box, cable and PSL adapter board will be shipped to CERN in custom containers designed and built by the same team at BNL that delivered the MicroBooBE electronics to Fermilab. To protect the electronics against ESD damage, the FEMB will be protected in anti-static bags and detached from the 7 m long cable bundles during shipping. The acceptance tests at CERN will be a visual inspection for damage and a repeat of the suite of FEMB QC tests at room temperature. Criteria for passing acceptance will be identical electronics performance to the measurements made at BNL during QC testing.

5 Warm Interface Electronics

The ProtoDUNE-SP warm interface electronics are housed the Warm Interface Electronic Crate (WIEC) attached directly to the cryostat flange. The WIEC

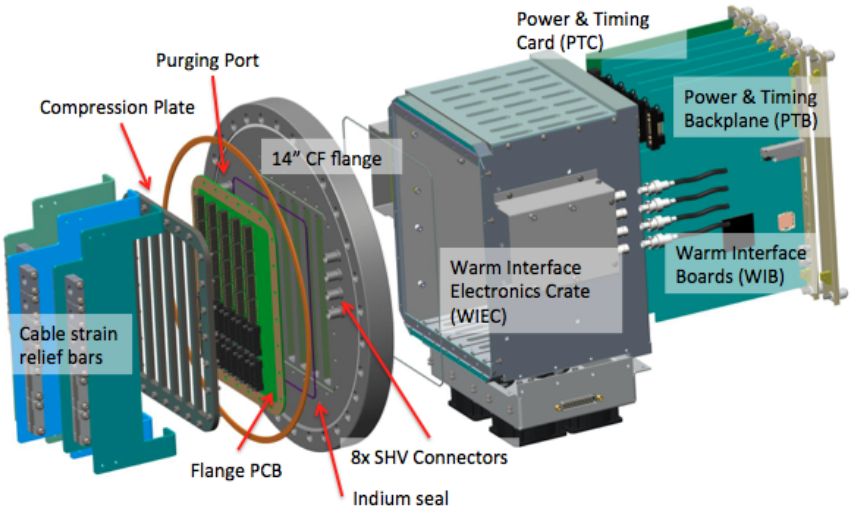

Figure 13: ProtoDUNE-SP TPC readout electronics flange, containing 5 WIB, 1 PTC, and 1 PTB.

contains one PTC, up to five or six WIBs, respectively, and a passive Power and Timing Backplane (PTB) which fans out signals and LV power from the PTC to the WIBs.

The WIB is the interface between the DAQ system (the RCE or FELIX systems for ProtoDUNE-SP) and up to four FEMBs. It receives the system clock timing and control signals from the timing system and provides processing and fan-out to the four FEMBs. The WIB also receives the high-speed data from the four FEMBs and transmits it to the DAQ system over optical fiber. Figure 13 shows the TPC warm electronics flange. The WIBs are attached directly to the TPC readout electronics flange on the cryostat feed-through. The flange board is a PCB with connectors to the cold signal and LV cables fitted between the compression plate on the cryostat side, and sockets for the WIB on the warm side. Cable strain relief is also provided directly on the flange, which is mounted vertically to the cryostat feed-through.

5.1 Power and Timing Card and Backplane

In addition to the WIBs, the warm interface electronics contains a Power and Timing Card (PTC). The PTC design was initiated at BNL, and developed and finalized for ProtoDUNE-SP by UC Davis; the V2 PTC schematics, board layout, and BOM are in DUNE DocDB 2988 [15]. The PTC provides an optical fiber interface from the ProtoDUNE-SP Bristol clock system to the CE warm interface electronics. The clock stream is separately fanned-out to the WIBs via the PTB (shown in Figure 13) in the WIEC. A diagram of the ProtoDUNE-SP

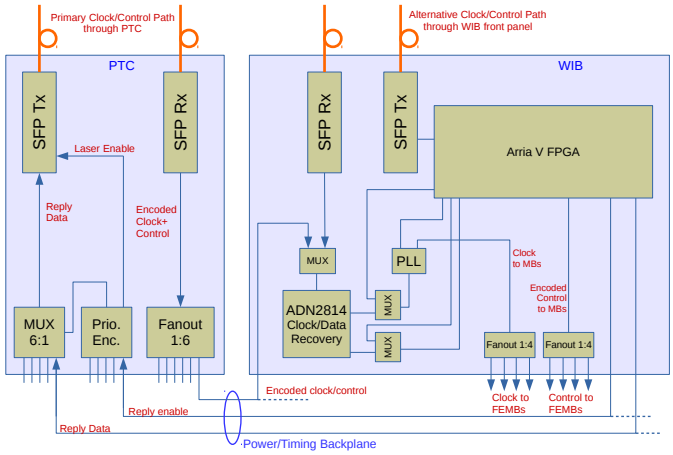

Figure 14: ProtoDUNE-SP PTC and timing distribution to the WIB and FEMBs.

timing distribution is shown in Figure 14.

The PTC also receives the low voltage power for the entire cold electronics connected to that flange, approximately 250W at 48V for a fully-loaded flange (5 WIB + 20 FEMB). The LV power is stepped down from 48V to 12V onboard the PTC, then fanned out on the PTB to each WIB, which provides further DC/DC conversion and fans the LV power out to each of the cold FEMBs supplied by that WIB, as shown in Figure 15. The majority of the 250W drawn by a full flange is dissipated in the LAr by the cold FEMB.

The PTB is a passive backplane that distributes the 12V power and timing clock from the PTC to the WIB. PTB schematics, board layout, and BOM are in DUNE DocDB 3327 [16].

ProtoDUNE-SP requires a total of 6 PTC and PTB, one each for each signal-feedthrough. The PTC and PTB will have to be tested for functionality prior to installation at CERN and FNAL. To validate the functionality requires testing the following features of the PTC:

- input of all LV channels at 12V from the power supplies;
- input of the encoded system clock on the optical fiber from the timing system;
- fan-out of all LV and timing distribution to the WIB over the WIEC backplane;

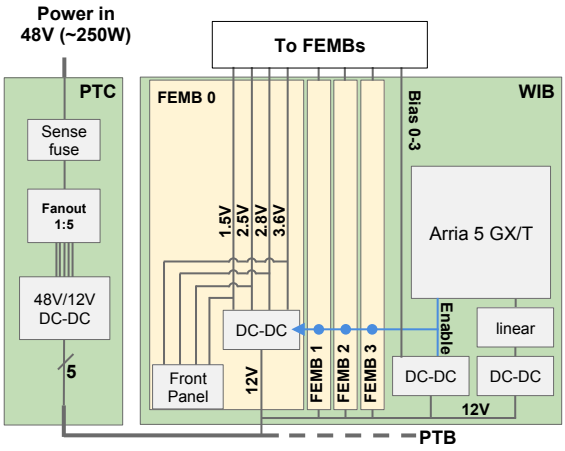

Figure 15: PTC and LV power distribution to the WIB and FEMBs. 250W is for a fully-loaded WIEC with the majority of the power dissipated by the 20 cold FEMBs in the LAr.

- return of the timing pulse from each WIB and transmission to the timing system during synchronization checks.

V1 PTC prototypes, shown in Figure 16, are being used in QA testing at BNL as part of the integration teststand described in Section 6, and will be shipped to Boston University as part of the ProtoDUNE-SP WIB-RCE-timing integration tests. However, the PTC will not require a dedicated QC teststand: for final QC validation the production boards will be tested in the already well-validated integration teststand at BNL.

The PTB QC will consist of inspecting connectors and PCB for damage and the electrical connections checked at BNL prior to installation into the WIEC. Once the PTB is installed in the WIEC, it will be part of the QC tests described in CE Mechanicals QC for ProtoDUNE-SP [11], and not removed.

5.2 Warm Interface Board

The WIB receives the encoded clock and the LV power from the backplane as shown in Figure 17. Each WIB, the V1 version shown in Figure 16, contains a clock/data separator to receive the system clock and a PLL to clean the jitter before transmitting the clock to the FEMBs. The WIB schematics, board layout, and BOM are in DUNE DocDB 3327 [16]. The WIB are a joint project between BNL (hardware) and Boston University (firmware and software).

Each WIB also contains a unique IP address for its UDP slow control interface. The IP address for the WIB is derived from a crate and slot address: the crate address is generated on the PTC board via dipswitches and the slot address is generated by the backplane slot. Note that the WIB also has connec-

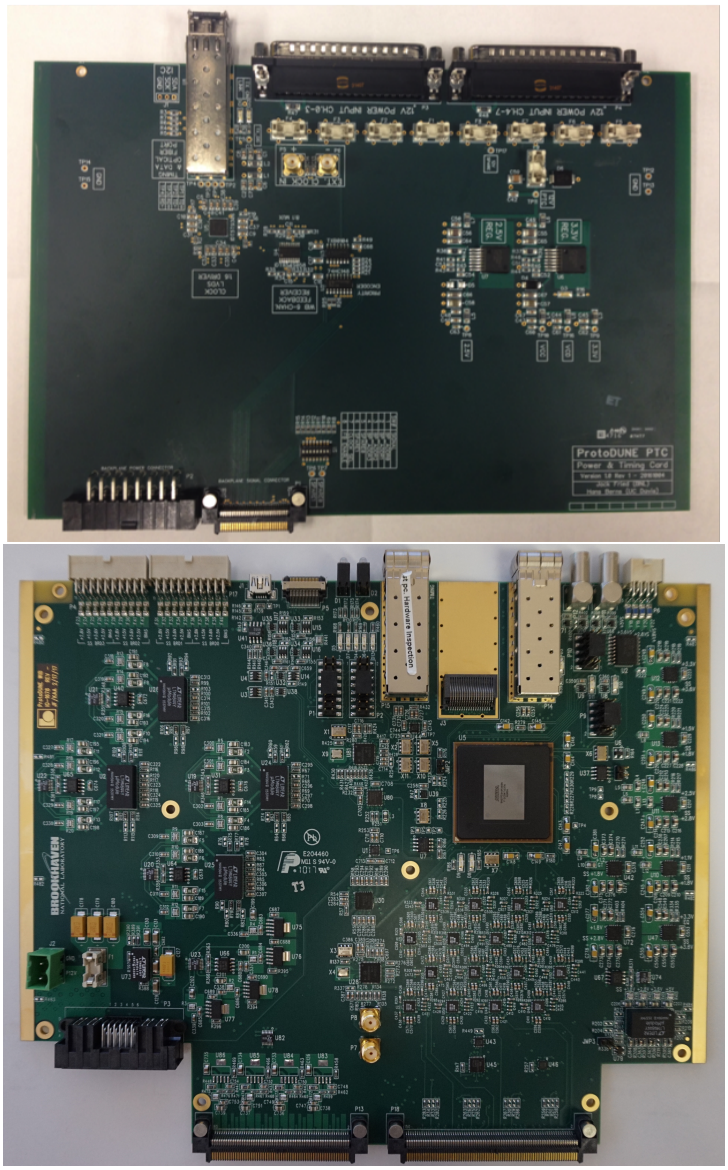

Figure 16: Top: V1 version of the ProtoDUNE Power and Timing Card (PTC); bottom: V1 version of the Warm Interface Board (WIB).

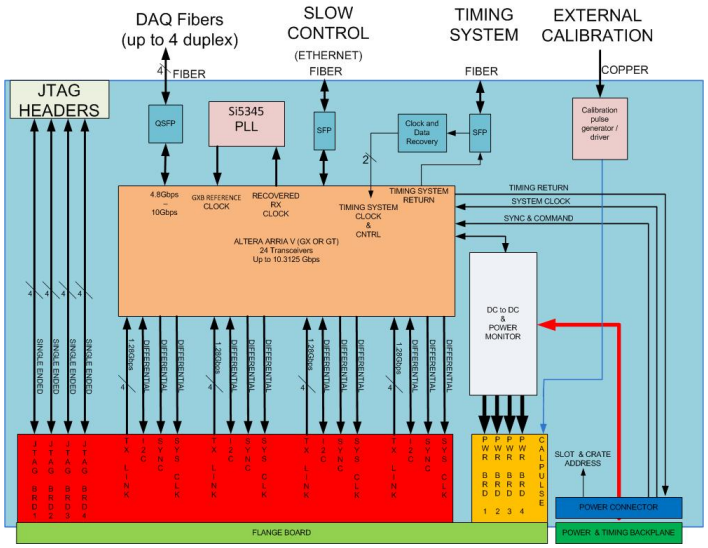

Figure 17: WIB clock, data and power paths. Note that front panel inputs will include a LEMO connector and alternate inputs for LV power.

tors to receive LV power and encoded system clock (shown in Figure 14) on its front panel, bypassing the PTC for debugging purposes.

The clock will be divided by two using either the FPGA or an on-board clock synthesizer chip to provide the 100 MHz clock required by the cold electronics. The clean clock and processed control stream is fanned out to up to four FEMBs. Each WIB also contains optional commercial active equalizer chips to recover the LVDS data. These are only expected to be required to recover the data over the longest cable lengths anticipated in the DUNE far detector: 25 meters. For the $\sim$7 m cable in ProtoDUNE-SP, the equalizers are not necessary, but will be used to test the expected DUNE data path.

The FPGA on the WIB is an Altera Arria V, which requires a 125 MHz clock for its state machine which is provided by crystal oscillators onboard the WIB. The ProtoDUNE-SP WIB uses the Altera V FPGA GT variant which can handle the 10 Gbps data rate needed by the FELIX DAQ and an QSFP connector for the optical data fiber.

The WIBs will be tested for functionality prior to installation at CERN. To validate the functionality requires testing the following features of the WIB:

- input of the 12V LV power and encoded system clock over the WIEC backplane;
- input of LV power and encoded system clock over the backup connectors on the front panel of the WIB;
- decoding of the system clock and return over the backplane of the timing

clock for each WIB during synchronization checks;

- DC-to-DC conversion of the 12V power at a sufficiently low noise injection into the LAr cryostat;
- all LV power voltages provided to four FEMB within the operational tolerance of the FEMB;
- all clock and control IO distributed to four FEMB, including all FEMB functionality listed in Section 4.1 operational;
- 16 ∼1 Gbps data links from four FEMB operational at a sufficiently low BER, with and without active equalization of the differential LVDS data;
- 2 1 Gbps Ethernet output for testing and local diagnostic testing;
- 2 or 4 high-speed data links operational to the different DAQ systems for ProtoDUNE-SP.

WIB prototypes are being used in QA testing at Fermilab and BNL as part of their integration teststands described in Section 6, and at Boston University as part of the ProtoDUNE-SP WIB-DAQ integration tests. However, the WIB will not require a dedicated QC teststand: for final QC validation the production boards will be tested in the already well-validated integration teststand at BNL.

5.3 Production

Two V1 PTC have been tested at BNL, with no issues found. The V2 PTC fabrication and assembly has been ordered from the experienced vendor selected by the board designer at UC Davis. They will be tested at BNL and a selection made between the V2-A and V2-B versions based on noise performance for final fabrication.

Two V1 WIB are being validated at BNL. One will be shipped to Boston for continued development of firmware and software. Several modifications to the WIB design are necessary. A V2 WIB will be designed and tested by late July. Following that, the final production order will be submitted.

The WIB and PTC will be shipped to CERN individually in anti-static bags, in shipping containers already available at BNL.

The final PTB production order will be submitted after testing the prototype PTB with the final WIEC prototypes that have been ordered and are expected back at BNL in May. The final PTB will be tested as part of the WIEC assembly and shipped to CERN in assembled WIEC/flange units in custom shipping containers designed and built at BNL, as described in CE Mechanicals QA/QC Plan, DUNE DocDB 1809 [11].

6 Integration and Noise

The physics goals of the DUNE program [2] require the LArTPC to be very low noise environments, with an ENC < 650 e^- for the induction wires at LAr temperatures as discussed in Section 4.2. To achieve this, the ProtoDUNE-SP grounding design, described in [17], require that:

- the mechanical support structure of the APA will be constructed in such a way that the APAs remain isolated from the top plate and any other conductive support infrastructure;
- the APA ground reference will come via the cabling used for the cold FE electronics, and be connected to detector ground at the cold electronics flange;
- there will be no side to side electrical contact between APAs hanging in the same planes.

The result of this design is that each APA with its cold electronics and signal-feed-through/flange will be a single integrated LArTPC read-out unit with local diagnostics provided by the warm electronics at the flange. The cryostat will also function as a Faraday shield for the TPC readout, with its own detector ground separate from the external building ground of the facility.

To study the effects of noise and system performance on this larger integrated detector scale, beyond the individual component testing, several integrated teststands are under construction, one at Fermilab and one at BNL. These teststands will both take digitized wire data from multiple FEMB attached to prototype versions of the APA via a cold electronics flange and full warm interface electronics readout.

6.1 Fermilab

A warm vertical slice test of the APA wire readout is being set up at Fermilab. An RF copper screen shielded room is being repurposed for this application. The RF room will serve to mock up the shielded cryostat environment and be large enough to allow us to install a 35ton APA frame. The screen room has a door which allows easy access for personnel to enter and modify the test environment. A pass through plate on the side of the screen room will serve to mock up the warm feedthrough found in the cryostat. The screen room is shown in Figure 18.

Proper AC distribution and grounding play a critical role in the performance of low noise electronics. The screen room gives us a special opportunity to examine and study some of these aspects. We plan on being able to supply power to the electronics (1) via a battery/UPS unit, (2) via the normal building power, and (3) via an isolated detector power and ground. Option (3) will model what we expect for infrastructure at ProtoDUNE-SP [17].

A special feature is being built into this room which will allow us to study AC coupling between the building ground and the isolated ground of the detector.

Figure 18: RF copper screen shielded room.

We will model this by lifting the screen room a few feet from the concrete floor and placing a metal sheet connected to building ground under the screen room, but electrically isolated from it. The metal sheet can be raised or lowered with respect to the bottom of the screen room. Small signals can be injected onto this sheet to mock up stray building currents and we can study the effects of capacitive coupling between the metal sheet and the electronics inside the screen room.

The vertical slice test conducted in the screen room is meant to test the newer protoDUNE-SP wire readout electronics. The three phases of the testing to be done at Fermilab are described in [18]. The test phases are structured to reflect the timeline in which we expect to have access to the screen room and when we expect to receive the prototype versions of the ProtoDUNE-SP electronics.

Phase one of the testing, shown in Figure 19, involves having the screen room in place along with a 35ton APA frame, the prototype FEMB and a standalone readout system supplied by BNL. It also provides the three types of power we wish to use to study noise levels. The APA frame and the FEMB(s) will be located inside the screen room. Cables which are intended to be the same type and length as are used at ProtoDUNE will penetrate the screen room and connect to power supplies and a readout system outside of the shielded enclosure. We will verify we can establish the expected low noise environment and study the effects of the different power/ground conditions described above.

The electronics setup for phase one is complete, with a full prototype CE readout chain installed on a 35ton APA: V1 "SBND" FEMB, cold cable, flange PCB to penetrate the screen room, and WIB.

As more prototype equipment becomes available, we will progress to the final stage of testing shown in Figure 20. The final testing phase will include

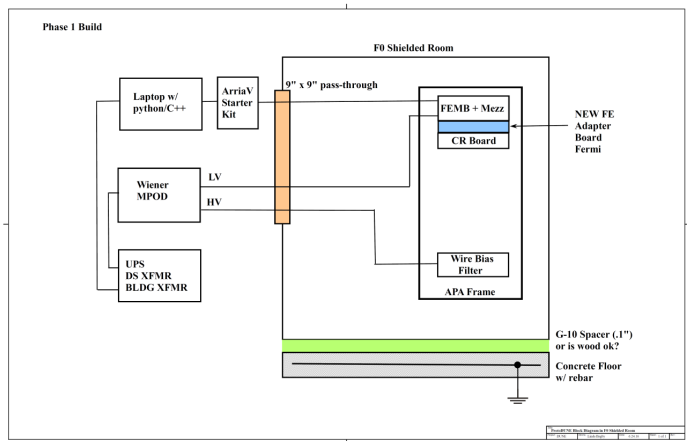

Figure 19: Phase one of the RF copper screen shielded room setup at Fermilab.

a full vertical slice. One to four FEMBs will be installed on a 35T APA wire frame. ProtoDUNE-SP cables be run between the feedthrough port of the screen room to supply power and provide signal paths for control and data. At the feedthrough port of the screen room, we expect to have a WIEC installed which will be very similar or identical to the one which will be used at the feedthrough ports of ProtoDUNE-SP at CERN. These crates will contain the Flange PCB Board, PTC, and WIB. The system can be readout with the RCE system or with a standalone DAQ.

We believe this system will provide an effective way for us to study many possible system noise effects and react to them prior to installing final production components at ProtoDUNE. The warm screen room application gives us easy access to the electronics, which will make any debugging of electronics or system issues much easier than when the electronics are located in a cryostat or cold box. The drawback of this system is that we cannot test at LAr temperatures. However, these cold tests can be performed at the test stands planned at BNL and CERN.

6.2 BNL

The BNL integrated noise teststand will uses a 40% "mini-APA" from PSL which can accommodate up to four FEMB. It is inserted into an insulated cold box, which will be capable of submerging the cold electronics in cryogenic liquid. The cold box will also provide Faraday shielding and access to the electronics via a signal-feedthrough and flange that is identical to the cold electronics flanges for ProtoDUNE-SP, shown in Figure 21. A WIEC houses the WIB, PTC, and PTB directly on the flange and provide real-time local diagnostics and readout.

Up to four FEMB can be attached to the APA via adapter PCB which also contain the RC filtering circuit needed to provide the wire bias voltage to the

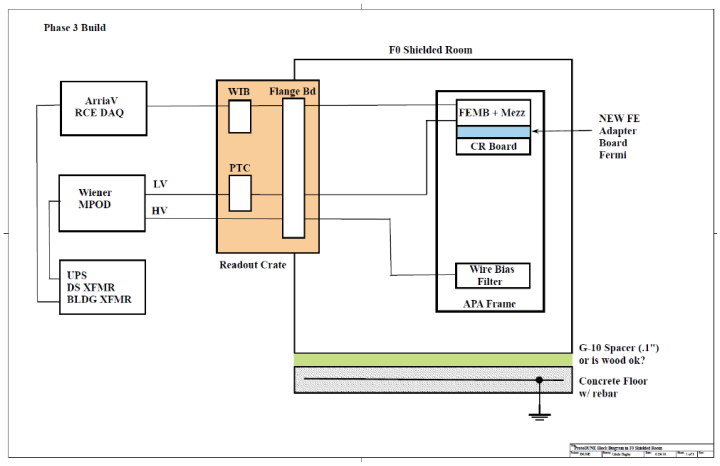

Figure 20: Final phase of the RF copper screen shielded room setup at Fermilab.

APA wires. The APA wires will be biased to the bias voltage specifications for ProtoDUNE-SP given in [3]. However, there will be no drift HV provided in the cold box.

The FEMB will be read out, controlled, and powered via the same 7 m long data and LV power cable bundles that will be used in ProtoDUNE-SP, and are candidates to be used in the 10 kton DUNE far detectors at SURF. The cables will penetrate the cold box at the signal-feedthrough and connect at the cold electronics flange to the WIBs. The WIBs will provide readout to the DAQ, and clock, control and timing to the FEMB. Thus, the 40% APA teststand will be a single integrated readout unit with the cold electronics operating at cryogenic temperature.

In order to carefully study the noise of the integrated 40% APA readout unit, the cold box will follow the ProtoDUNE-SP specifications for power distribution and grounding described in [17]. This allows detailed testing of noise sources and their impact on the TPC wire data. Some, but not all, of the planned tests are summarized in Table 5.

One specific noise source which was observed in the 35ton detector is the "high-noise state," in which the data from the 35ton wires showed low amplitude (relative to the FE dynamic range) oscillations in the range of 100-900 kHz over the entire detector (4 APAs with 4 FEMB each), as described in [7]. The 35ton high-noise state was only observed when the cryostat was filled with LAr with the FE electronics submerged, and never conclusively measured on individual FEMB testing. However, multiple violations of the grounding and shielding plan for the 35ton detector were made during installation and commissioning [7]. Thus, operating multiple FEMB simultaneously while submerged in cryogenic liquid in an environment with well understood grounding and shielding is an important test of whether or not the high-noise state is intrinsic to the electronics

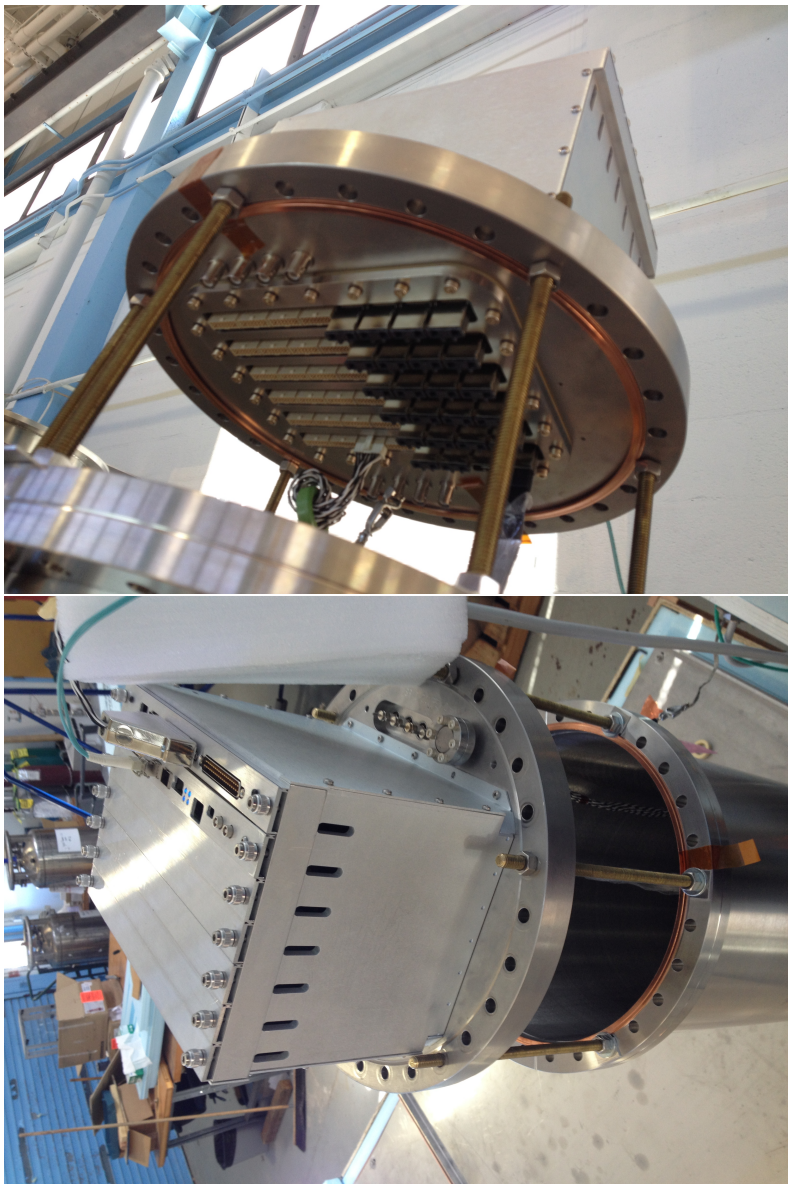

Figure 21: Cold box signal feed-through for 40% APA integration test at BNL. Top: flange PCB on cold side of CE flange; bottom: WIEC attached to warm side of CE flange containing PTC, WIB, and PTB.

Test	Implementation	Goal
Readout functionality	Read out the full CE chain to a local DAQ for data analysis: measure baseline, RMS noise, and linearity on all channels.	Validate baseline operation of full CE chain.
Cable noise injection	Study RMS noise levels with multiple LV and data cable configurations and shielding.	Validate cable selection, shielding, and design.
External noise injection	Study RMS noise levels under multiple external noise signals including shorted grounds, ground loops, and external sources near the WIEC .	Study and analyse effects of ground scheme failures and validate warm electronics shielding.
High-noise state	Operate in similar configurations to the 35ton detector including multiple FEMB in cryogenic liquid but with well understood grounding and shielding.	Study high-noise (or lack) in a cryogenic, multiple FEMB teststand.
Warm interface noise	Operate a full warm electronics readout on a flange near cold FE electronics and wires with all functionality (*e.g.* DC-to-DC converters powering the FEMB).	Validate that low noise operation is achieved with the current WIB design.

Table 5: Overview of the testing in the BNL 40% APA teststand.

or from the failures of the 35ton implementation.

7 QC Teststands

Dedicated teststands for QC validation of all components have been set up at BNL. There are 4 PC workstations dedicated to ASIC and FEMB qualification, shown in Figure 22. Each workstation will have a Cryogenic Test System (CTS) for rapidly cycling the electronics from room to LN2 temperature without exposing the electronics to condensation. Individual workstations will also have ASIC testboards and LV power supplies, or cables for FEMB testing depending on the function of each workstation.

Each workstation will have one shift operator, who will be responsible for the QC testing at that workstation. Two shift leaders will be responsible for the overall running of the day to day operations in the lab.

The workstations are connected to a network via two server PCs. Tagged releases of the QC software to control ASIC or FEMB testing are installed on the servers and pushed to the testing PCs. Shift operators will not have the ability to modify the tagged software for testing.

Figure 22:

Additionally 2 PC workstations have been set up as (1) a warm electronics integration teststand, and (2) a DAQ for the 40% APA noise and integration teststand. These workstations will usually be operated by experts for testing and debugging hardware that fails the QC validation.

7.1 Software and Database

The large number of cold electronics will require multiple quality control test stands running in parallel. Standardized methodology and software is needed to evaluate whether cold electronic components meet operating and performance requirements in a consistent fashion. Test methods and the associated data analysis need to be automated as much as possible to process the production electronics and meet the ProtoDUNE-SP schedule discussed in Section 8.

The cold electronics control and data acquisition interface is based on a simple Python package [19], allowing physicists to easily modify and develop additional tests. Basing the test-stand software in python makes integrating table-top instruments, data-processing packages like ROOT and database interfaces straightforward. A simple graphical user interface (GUI) is also defined for debugging purposes, a beta version of which is shown for a FEMB teststand in Figure 23. Each specific quality control test will have a dedicated GUI and software package. All digital logic firmware, data acquisition software and analysis code must be committed to a repository and under version control.

Automated data analysis and database archival of results are important test stand requirements. Most analyses involving test stand data are simple and can be performed while the test is underway. This allows faster detection of potential problems with electronic components and additional debugging. Including the database archival of results as part of the testing process will reduce notekeeping requirements and ensure that a complete record of quality control tests is available. Online monitoring software that interfaces with the quality control database will monitor testing progress and identify any systematic problems.

The design of the GUI is important as test stand operators may not be familiar with the electronic components or analysis software. The minimum required

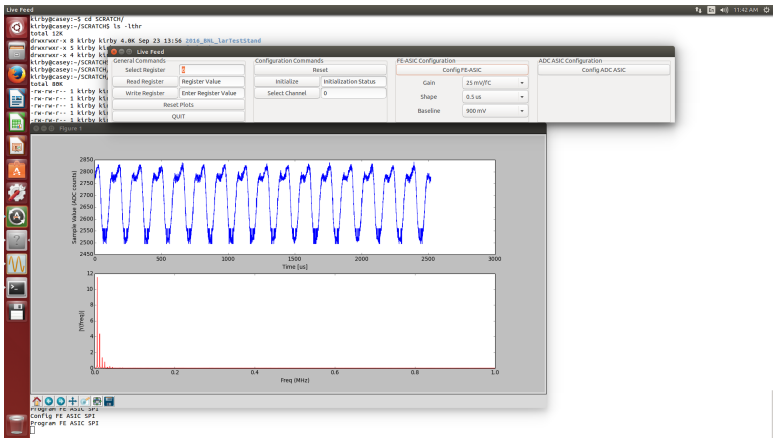

Figure 23: GUI interface to an FEMB.

set of operations includes; verifying the test stand is operational, performing the test and recording associated data, analyzing the data and reviewing summary information, and archiving the results in a database. More elaborate tests where the test stand operator has to interact with the setup would result in additional steps and associated checks.

8 Schedule

ProtoDUNE-SP cold electronics is scheduled to install beginning in August 2017 through early 2018 for data-taking in the CERN test beam in the fall of 2018, prior to the long shutdown at CERN.

The driver of the ProtoDUNE-SP installation schedule is the production of the final FE and ADC ASICs, expected to be complete in June 2017. The assembly and testing of the FEMB must follow the ASIC QC validation, and first FEMB components must arrive at CERN by August 2017. To complete this, the schedule shown in Figure 24 has been developed. The construction of components such as the signal-feedthrough, CE flange, and warm electronics, while vital, are not the critical drivers of this schedule.

9 Conclusion

The LArTPC cold electronics system for the ProtoDUNE-SP detector includes everything from receiving charge induced/collected on the APA wires at the FE pre-amplifer, through transmission of the digital wire data to the DAQ. A comprehensive set of QA tests are ongoing for all components to ensure operation in the ProtoDUNE-SP detector within the requirements specified in [14]. The result of this QA program will be a full suite of QC validation testing at BNL

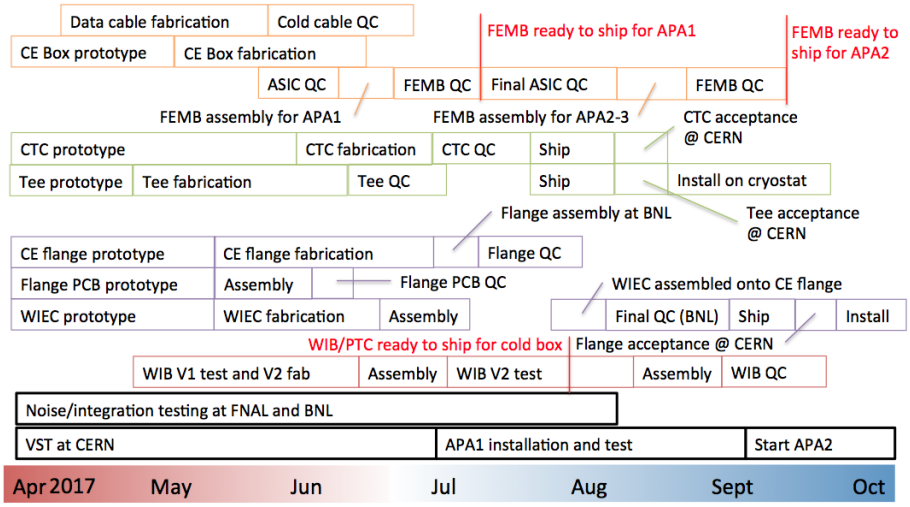

Figure 24: ProtoDUNE-SP component QA/QC testing schedule from April 2017 through October 2017.

during the summer of 2017, with all cold components validated under multiple thermal cycles to cryogenic temperatures.

Vendors for production of all electronics have been identified and nearly all prototypes have been produced and tested. Shipping of all final components will be handled by Interfreight, directly CERN. Interfreight is an experienced vendor with more than 10 years experience shipping components for the ATLAS LAr calorimeter. The schedule for installation and commissioning for the ProtoDUNE-SP cold electronics is aggressive, mostly due to the long shutdown at CERN driving the ProtoDUNE-SP detector construction and a QA/QC schedule to meet this goal has been developed.

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