ProtoDUNE-SP Cold Electronics

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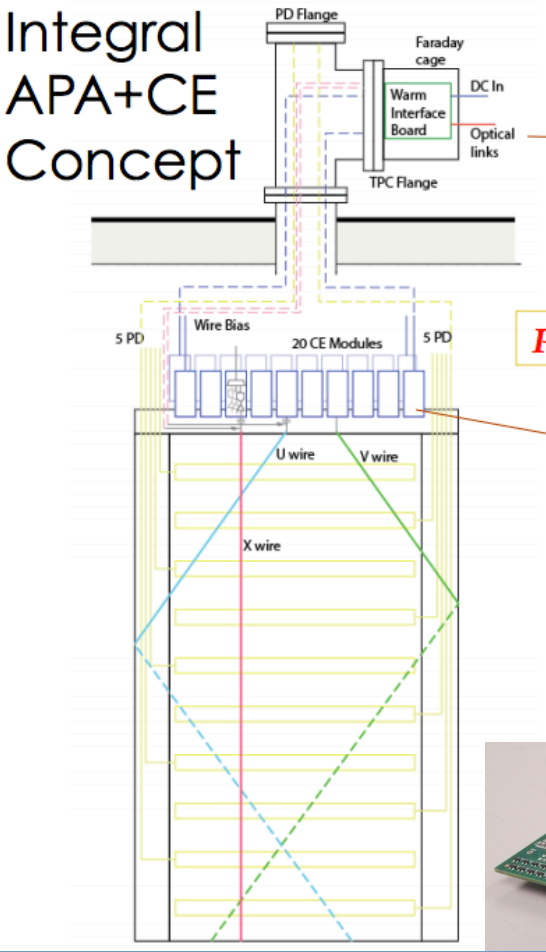
representing the Cold Electronics design team

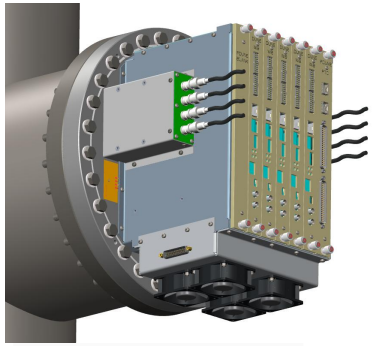
LBNC Review
6/23/17

Outline

- Cold electronics overview
- Components
  - Front-End and ADC ASICs
  - Front-End Motherboard
  - Signal feed-through
  - Warm electronics
  - CE flange and warm interface electronics crate
- System integration
- Schedule

Integrated LArTPC Cold Electronics

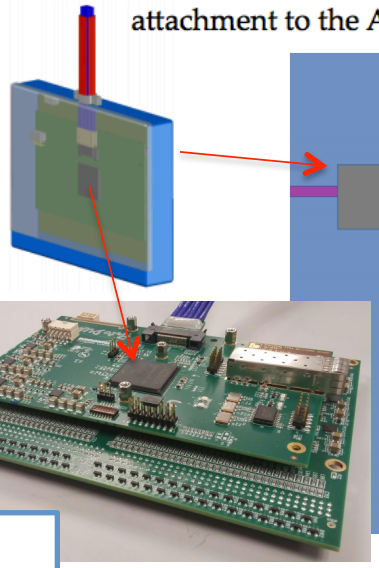


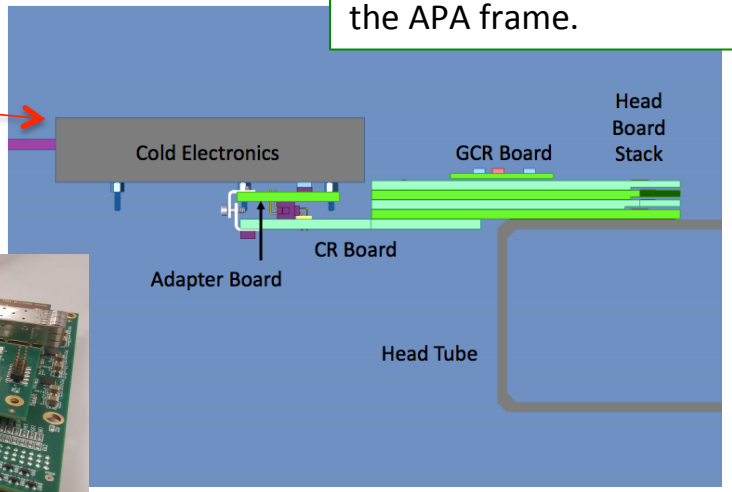


Warm Interface Electronics: interface between CE and DAQ/power with local real-time diagnostics.

ProtoDUNE-SP

Cold electronics module and its attachment to the APA frame



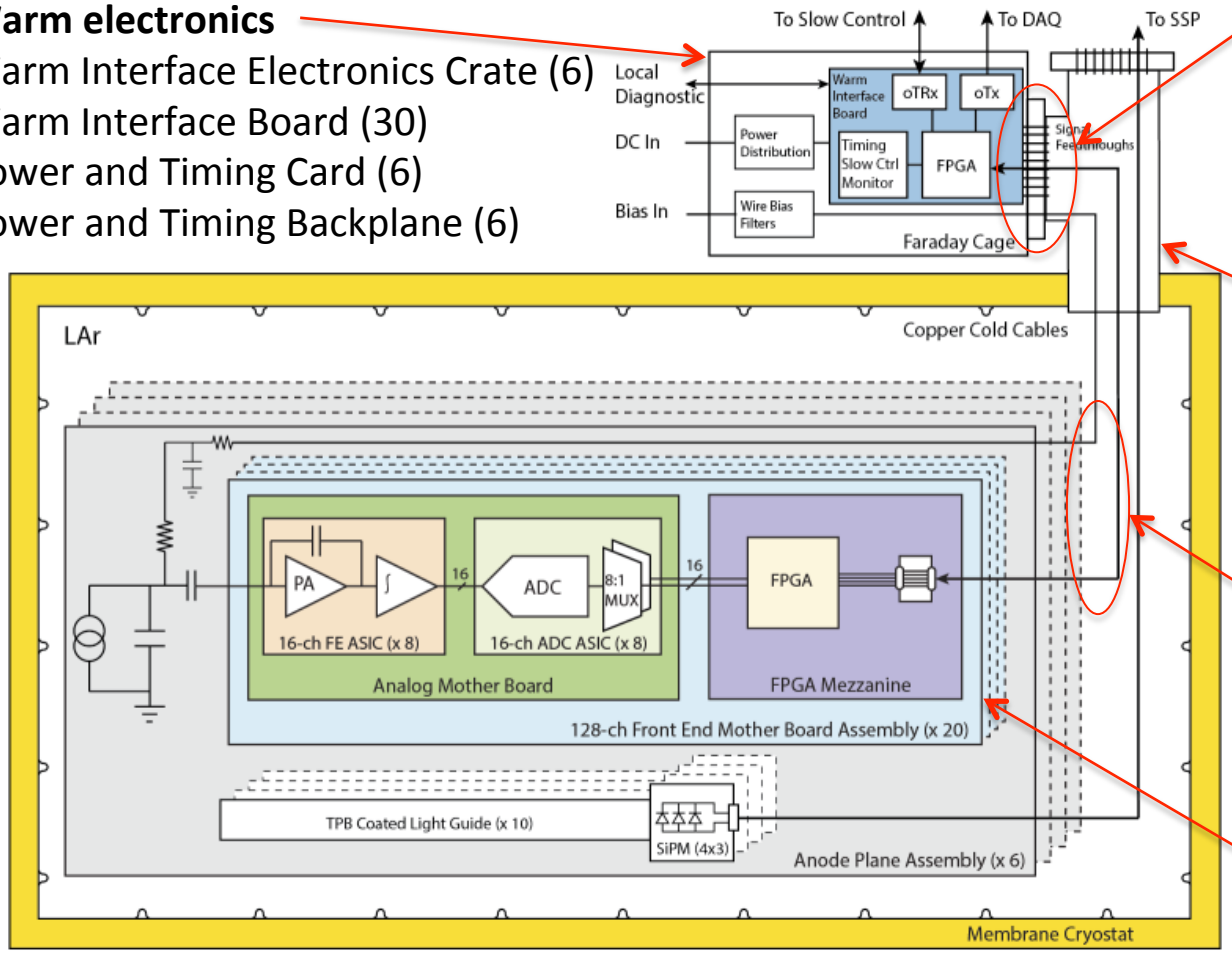


Common plane of all cold electronics must make low impedance connection to the APA frame.

Each APA must be isolated inside the cryostat and only connected to the cryostat at the flange.

ProtoDUNE-SP Cold Electronics

Warm electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable to FEMB
LV and data cable (120+120) and APA wire-bias SHV cable (48)

Front End Motherboard
(FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

Milestones

- APA/Cryostat
  - Deliver V1 WIB to CERN for vertical slice in late June
  - 25 FEMB for APA1 ship to CERN in early Aug
  - Feed-through (Tee pipe + CTC) install on cryostat in early Sept
  - CE flange + WIEC assembly install on Tees in early October
  - 50 FEMB for APA2-3 ship to CERN in mid October
  - Production WIB/PTC install in WIEC in late October
  - 75 FEMB for APA4-6 ship to CERN in November
- Cold Box
  - Components ship to CERN in late July
  - Full prototype Flange + WIEC assembly install in early Aug
  - Deliver V2 WIB/PTC for installation in WIEC in late Aug

Front End ASIC

- ~5mW/channel for long lifetime
- 16 independently programmable channels
  - 4 gains: 4.7, 7.8, 14, 25 mV/fC
  - 4 shaping times: 0.5, 1, 2, 3 µs
  - 2 baselines: 200 mV/900 mV
  - Analog test output
  - Internal 6-bit DAC for calibration
- 2012 design of front end (FE) ASIC deployed in multiple LAr TPCs:
  - MicroBooNE (**ENC ~400e-**), CAPTAIN, LArIAT, 35-ton, ARGONCUBE@Bern, ICARUS 50l TPC@CERN
- 2 subsequent revisions:
  - P1 version tested at MSU/BNL since July 2016
  - Current version (P2) has been at BNL since November 2016

Bandgap Reference

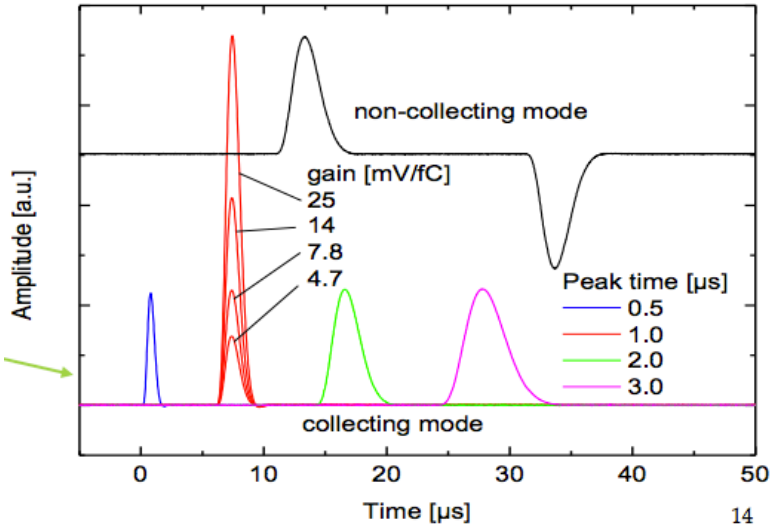
$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{at}\ 300\ ^\circ K \\ 1.164\ V \ \text{at}\ 77\ ^\circ K \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{at}\ 300\ ^\circ K \\ 259.3\ mV \ \text{at}\ 77\ ^\circ K \end{cases}$$

~ 2.86 mV / °K

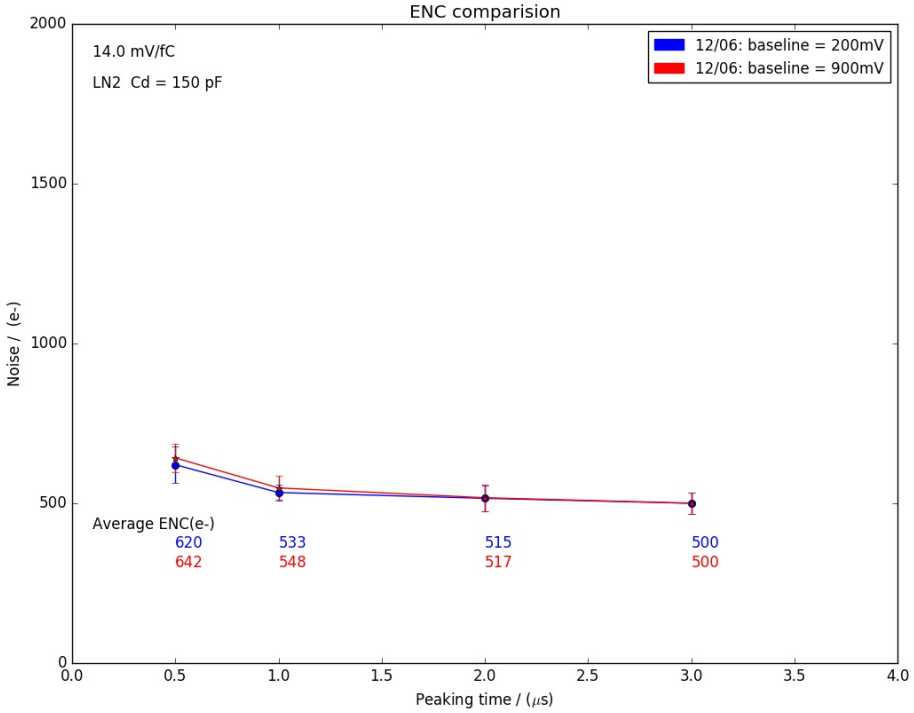


Datasheet: DUNE Doc 1484

FE ASIC Development

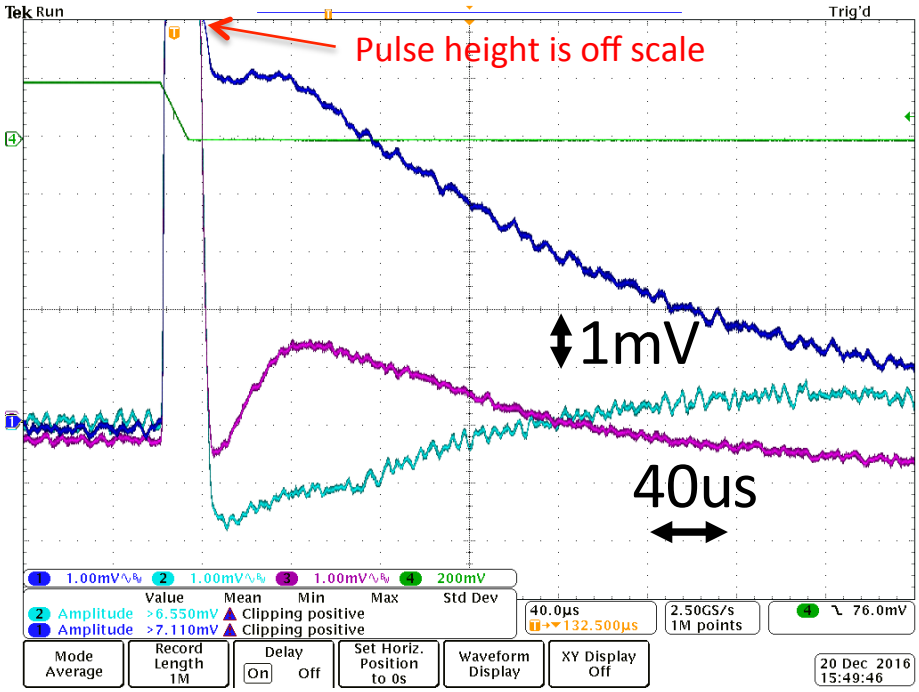
Version	Feature	Tested
P1	6-bit internal DAC	DNL < 0.2 LSB; INL < 0.5 LSB
P1	Buffer-off mode (ADCs onboard FEMB)	OK
P1	Add 1nA and 5nA leakage current capability	OK
P1	Add “smart” reset (2 pins instead of 1)	OK
P1	Revise BGR start-up circuit (~5% ASICs fail to power on in cryo)	No failures seen under 2000 thermal cycles
P1	Increase ESD protection on IO	OK
P2	Revise bias current design (removes need for external resistors to bring up every channel)	OK
P2	Address pole-zero cancellation	< 1.5% dispersion
P2	Add analog output	OK

P2 FE ASIC Evaluation



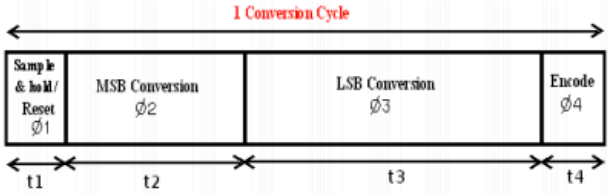
ENC < 550 e- at shaping times > 1 μsec
Measured on FEMB with V* ADCs
(stuck codes removed)
ENC = equivalent noise charge in electrons arriving at the pre-amplifier

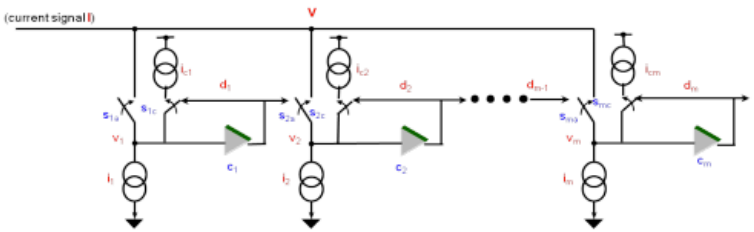
Pole-zero cancellation
P1 FE baseline recovery dispersed by ~5% of peak height ⟶ P2 FE ~1.5% PH

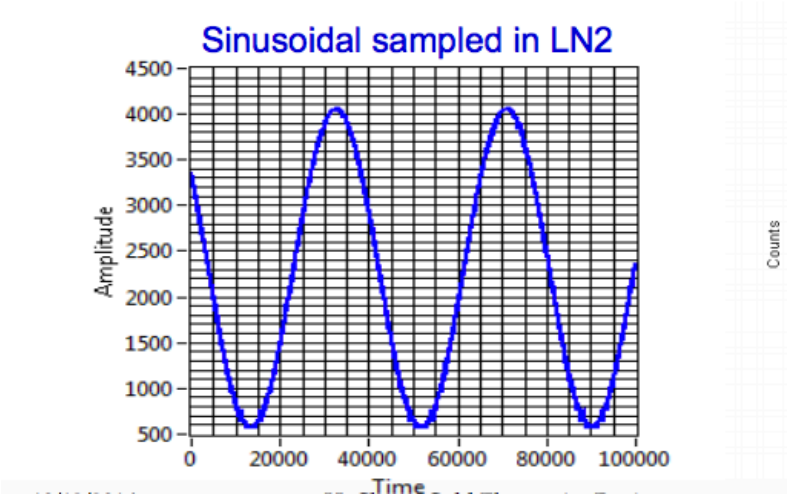


(Green: Calib Pulse); (Dark Blue: P1 chn14); (Light Blue: P2 chn2), (Pink: P2 chn14)

ADC ASIC







Datasheet: DUNE Doc 1485

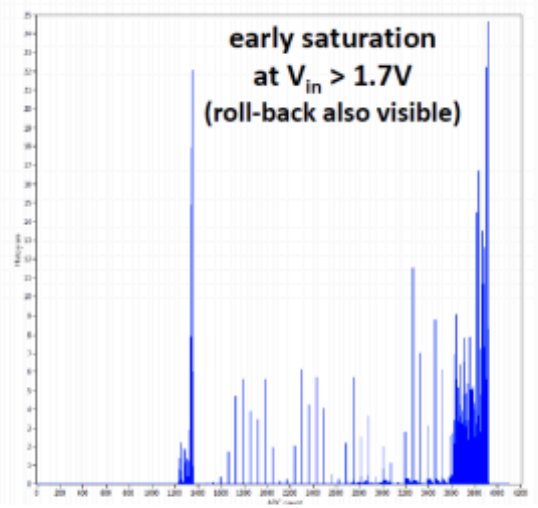
- ~5mW/channel for long lifetime
- Current-mode domino architecture with 4 phase operation
  - Sample/hold
  - 6 MSB conversion
  - 6 LSB conversion
  - encoding
- 16 programmable channels
- 12 bit ADC up to 2 MHz internal or externally-applied sampling clock
- 2014 version of ADC ASIC deployed in 35-ton prototype
  - Stuck codes observed
  - All high-speed digitized data links (2048 channels) functioned in LAr
- V* ADC tested at BNL since Jan 2016
  - Used to qualify FEMB prototypes up through P2 FEMB
- Current version (P1) ADC has been at BNL since October 2016

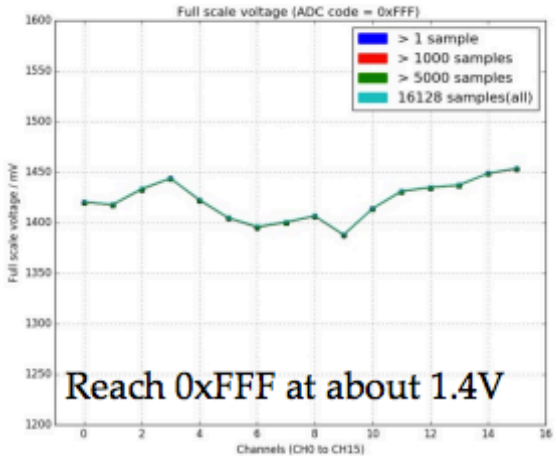
ADC ASIC Development

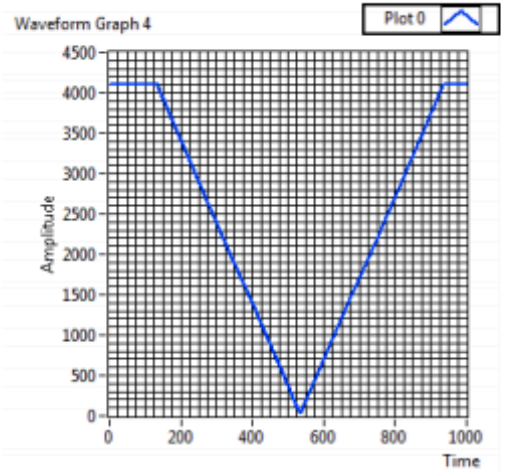
Version	Feature	Tested
V*	Partial fix to INL/DNL (stuck codes)	OK
V*	COLDATA compatible (external sampling clock and ADC-busy signal)	OK
P1	Add test-pattern and FIFO soft reset	OK
P1	Fix INL/DNL (stuck codes)	NO
P1	Fix early saturation and roll-back issues	OK
P1	Revise BGR start-up circuit	No failures seen in 2000 thermal cycles
P1	Increase ESD protection on IO	OK
P1	Modify configuration interface (from LVDS to single-ended for FE ASIC compatibility)	OK
P1	Default power ON in data collection mode	OK

P1 ADC ASIC Evaluation

- Early saturation (ADC not reaching 0xFFF) no longer present
- Roll-back (as input voltage increased above saturation, codes decrease) fixed
- DNL "stuck codes" are still observed
  - Approximately 5% in P1 (all channels) in LN2 averaged over entire dynamic range
  - Can be further mitigated by careful selection of operating mode
- Other design features verified







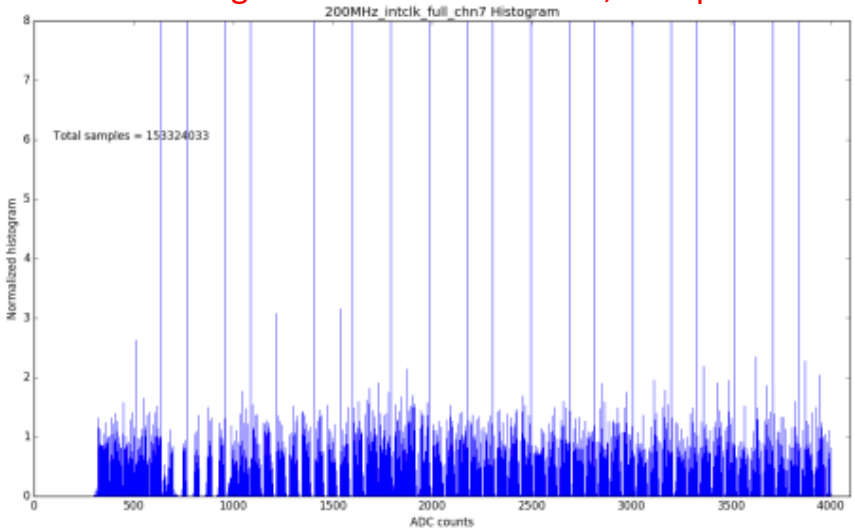
V* ADC with early saturation

Early-saturation & roll-back is fixed on P1 ADC

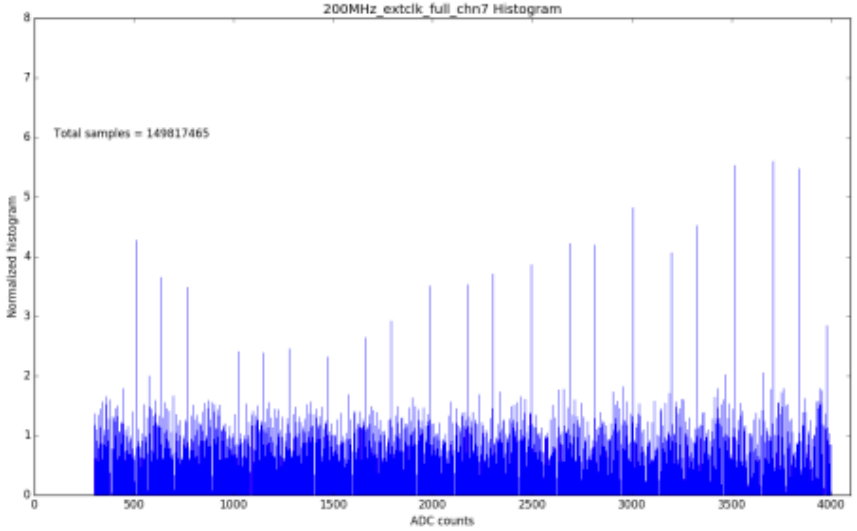
P1 ADC DNL “stuck codes”

- Test ADC with a high-precision ramp voltage in LN2:

Using 200 MHz internal clock, 2 Msps

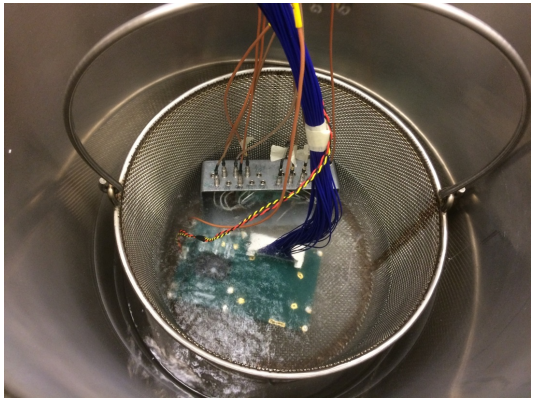


Externally generated 200 MHz clock, 2 Msps

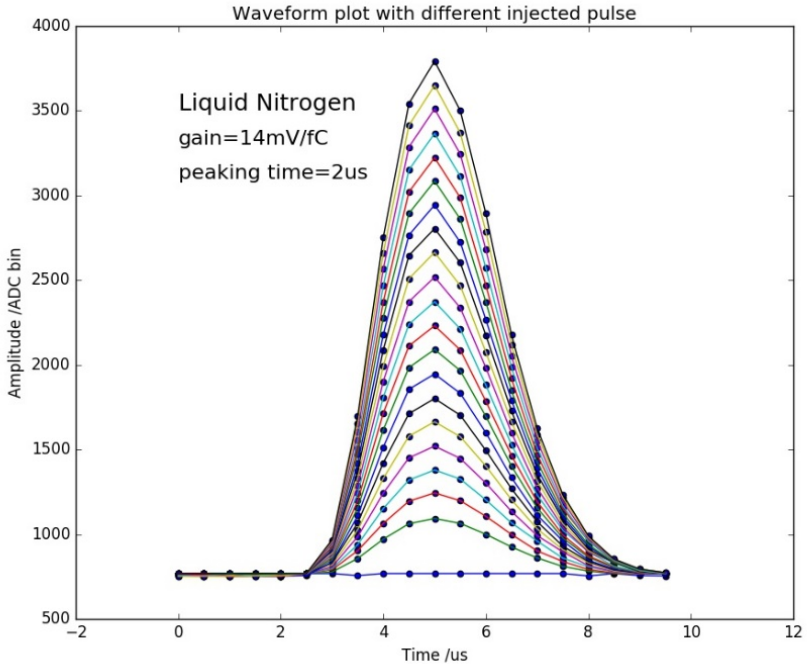


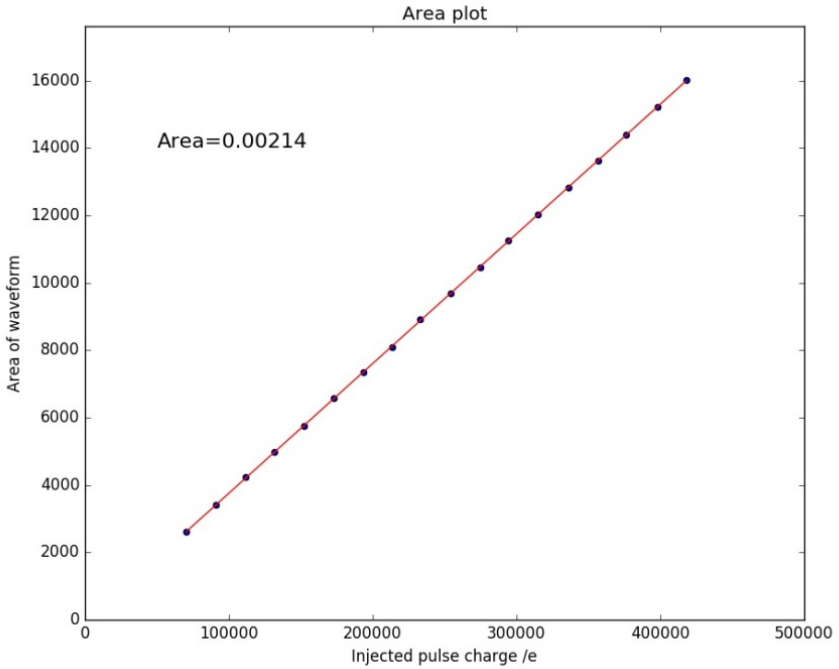
- Preferred operation mode of P1 ADC has been established
  - Full steering current
  - External control clocks with careful selection of clock phases
  - AC coupling with bias to eliminate low ADC range

P1 ADC ASIC Evaluation



- P2 FE + P1 ADC Test
  - Peak and area linearity test of P2 FE and P1 ADC in LN2
  - Same FE channel pulser is used to test 16 ADC channels
  - Both peak and area measurements show reasonable non-linearity (< 0.5%)
- FE 14mV/fC, 2us t_p + ADC 2Msps
  - Peak INL: 0.274+/- 0.050%
  - Area INL: 0.254 +/- 0.070%



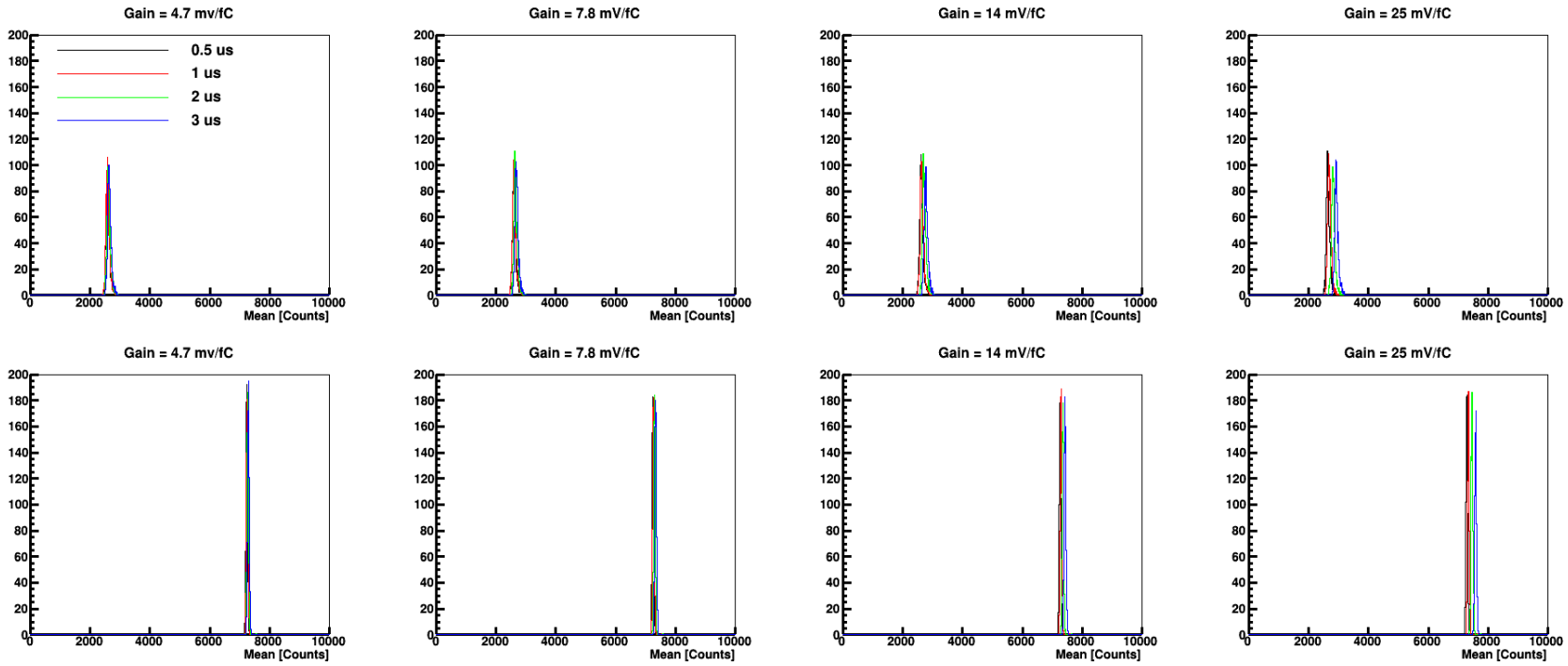


FE and ADC ASIC QC

- 268 P2 FE and 395 P1 ADC ASICs have been received at BNL for APA1
  - All ASICs will be qualified before assembly onto FEMB
  - FE: warm validation of all and cryo yield measured with ~10%
  - ADC: select ~250 of the best ADCs from ranking with cryo data
- 5 QC teststands are running at BNL: 2 FE and 3 ADC ASIC
  - Quad-socket FE ASIC testboard
  - Single-socket ADC ASIC testboard
- Shifters from DUNE institutions running the teststands
  - Training at BNL: no CE experience required
  - Supervised by BNL/SBU post-docs
  - Shifts expected to run from June-September 2017
- Collecting statistics with these ASICs for final selection of ASICs for APA2-6

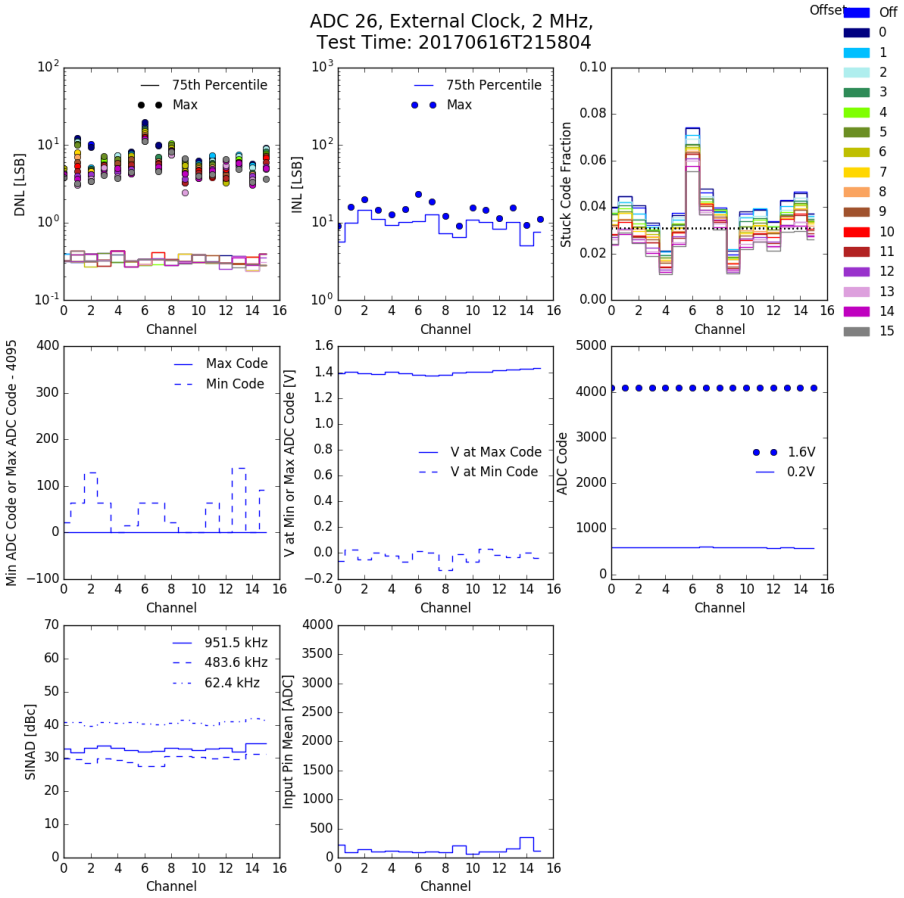
FE Baseline Summary: 6/8-9

All 268 FE ASICs have passed warm validation with no defective channels
All data taken with test runs very uniform: baseline, gain, and ENC
- 11/268 have at least one value out of the range of the preliminary selection cuts
- These 11 will be included in the cryo yield testing



Mean baseline, raw 14-bit ADC counts, all channels, top row: 200 mV; bottom 900 mV

ADC Performance Summary

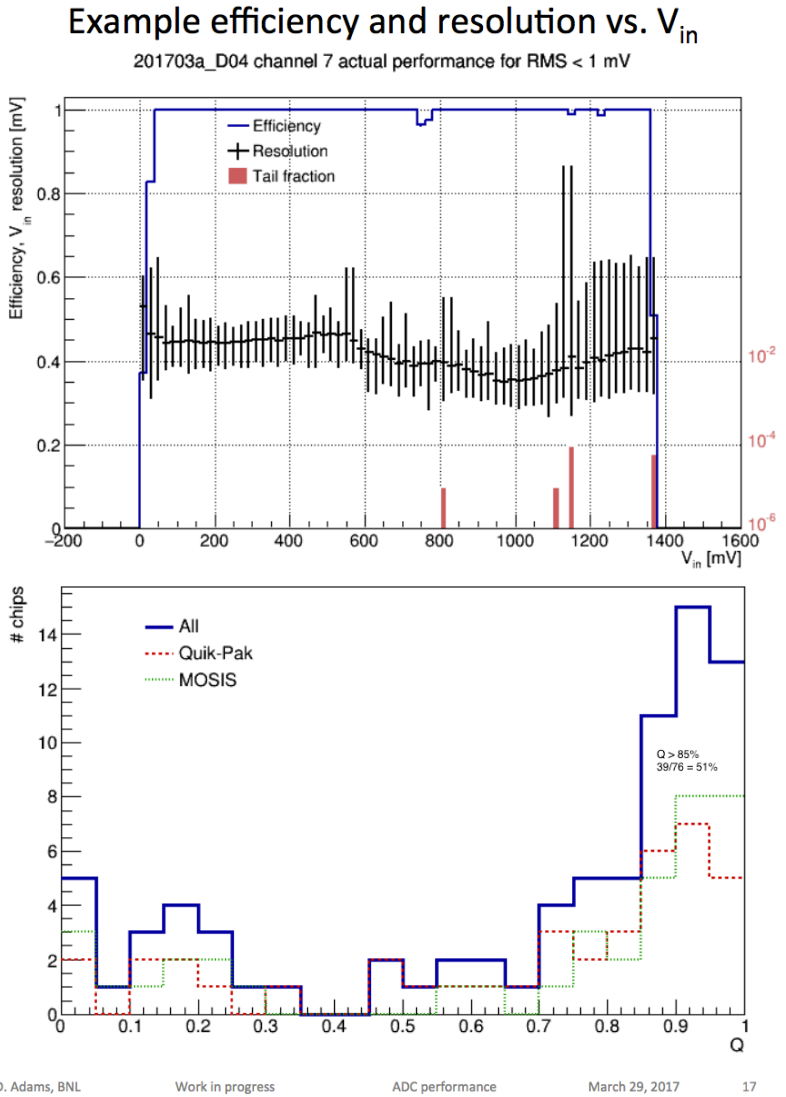


Summary plots from ADC26 at RT

- ADC ASIC QC teststand will make pass/fail decision with preliminary selection cuts
  - For internal and external clocks (all phase settings) and 1 and 2 MHz sampling
- As of 6/16, 14 ADCs have been tested warm with 1 failing the preliminary selection cuts
  - For this batch, all ADCs will be tested in LN2
  - Cuts will be adjusted as we gather statistics
- 2 ADCs have been tested cold and the data will be used to optimize the cold preliminary selection cuts

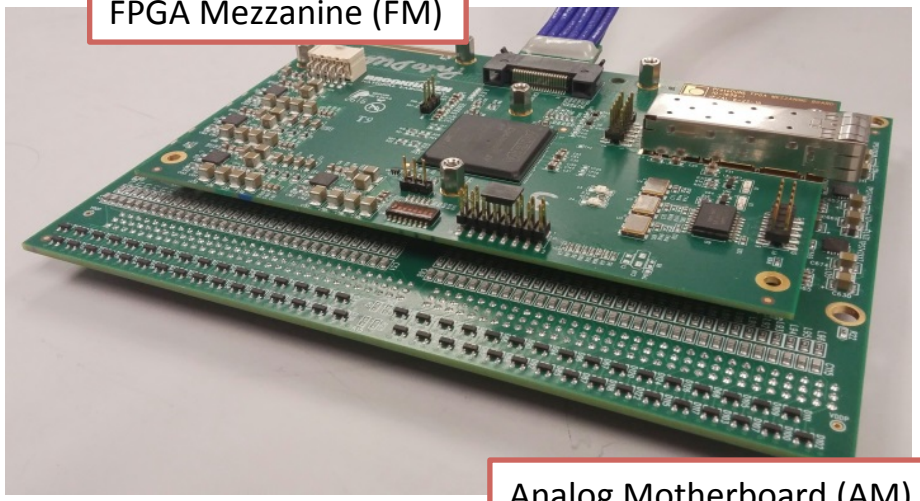
ADC ASIC Ranking

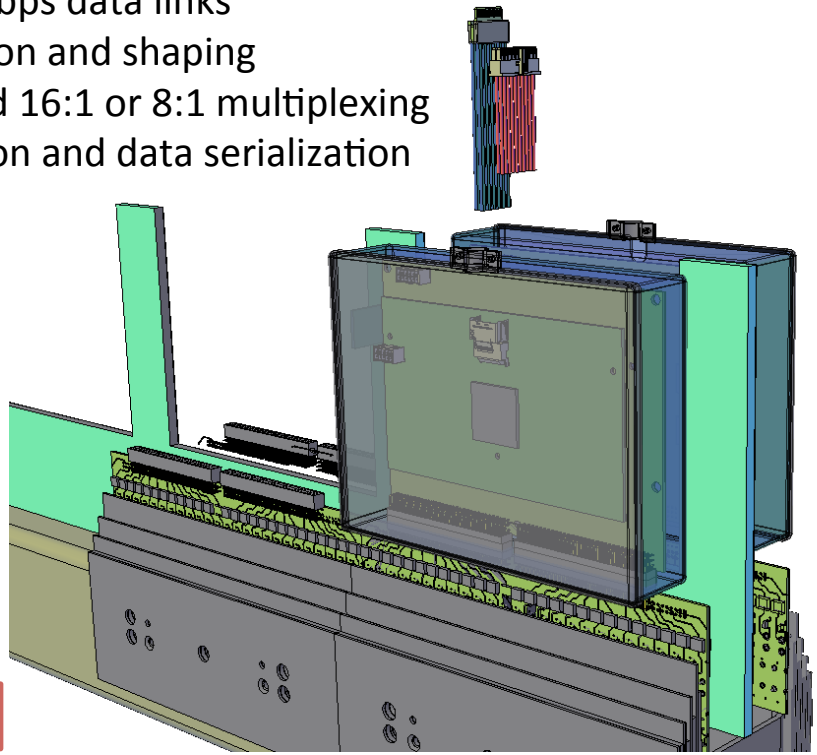
- External ramp input to ADC measures linearity, stuck code fraction, and effective ADC range (saturation and roll back)
  - Bin resolution is the RMS of voltages that populate an ADC bin after linearity correction
  - Efficiency is the fraction of mV input samples that land in bins with good resolution
  - ADC Q score is the efficiency for all input ranges in all channels multiplied
    - Q=1 if all input voltages land in good bins
- ADCs will be ranked by Q score on ramp data
  - DNL and stuck code fraction
  - Effective range



FEMB

- 128 channels of digitized wire readout, 4x1 Gbps data links
  - 8 16-channel FE ASICs: pulse amplification and shaping
  - 8 16-channel ADC ASICs: digitization and 16:1 or 8:1 multiplexing
- FPGA mezzanine for ASIC control/configuration and data serialization





FEMB individually enclosed in CE Box: 20 FEMB/APA

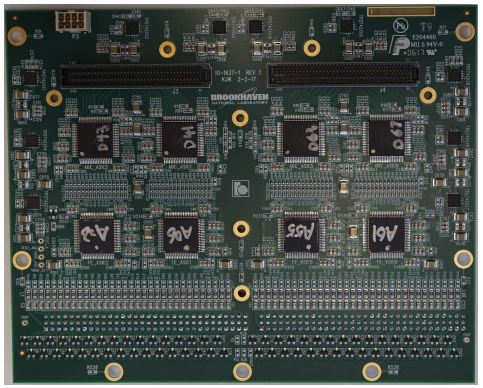
- Attaches to PSL APA adapter and incorporates built-in cable strain-relief
- Low impedance connection from FEMB ground to APA frame
  - Reinforced by copper braid from CE Box to APA mounting brackets

P2 FEMB contain P2 FE and P1 ADC

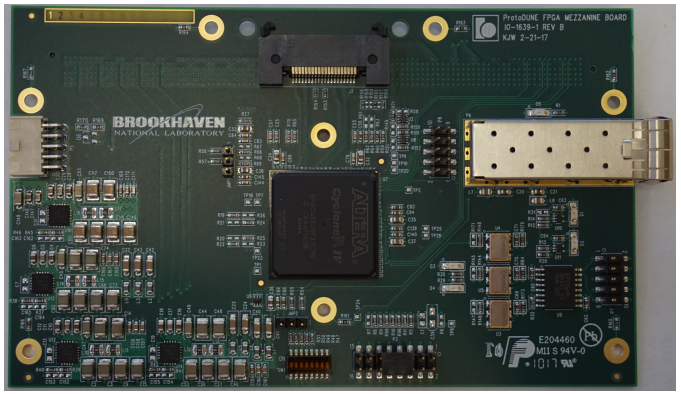
FEMB and Cold Cable

- 6 total P2 analog motherboards have been delivered to BNL
  - All tested and are working well
  - P2 FE ASICs, P1 ADCs with external clock
- 35 FPGA mezzanines have been delivered for APA1 and will be tested

P2 analog motherboard



P2 FPGA mezzanine

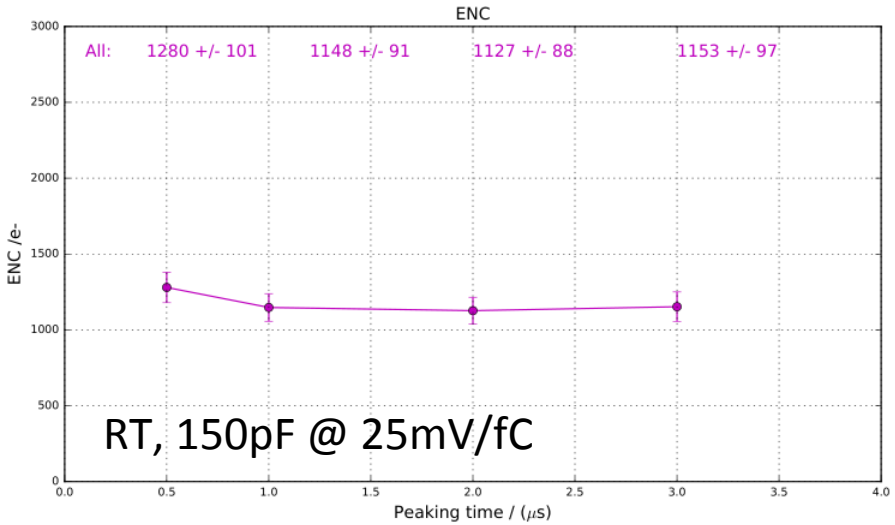


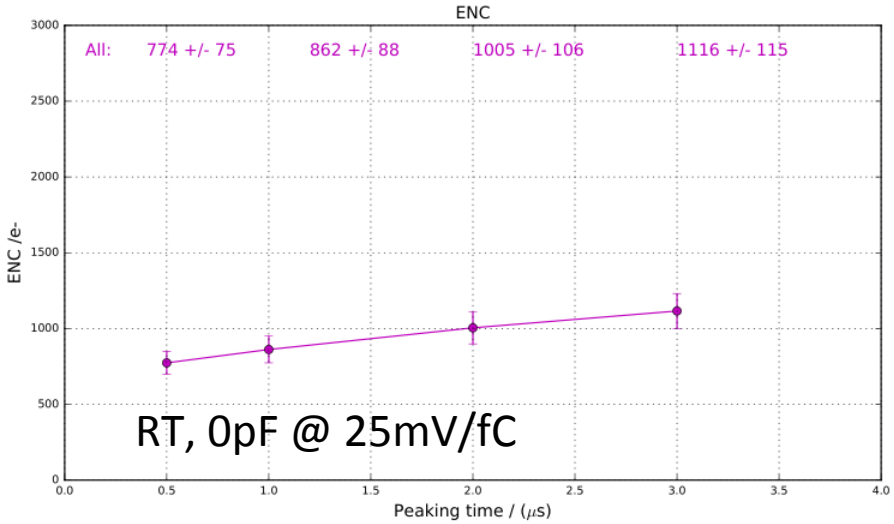
Cold data cable

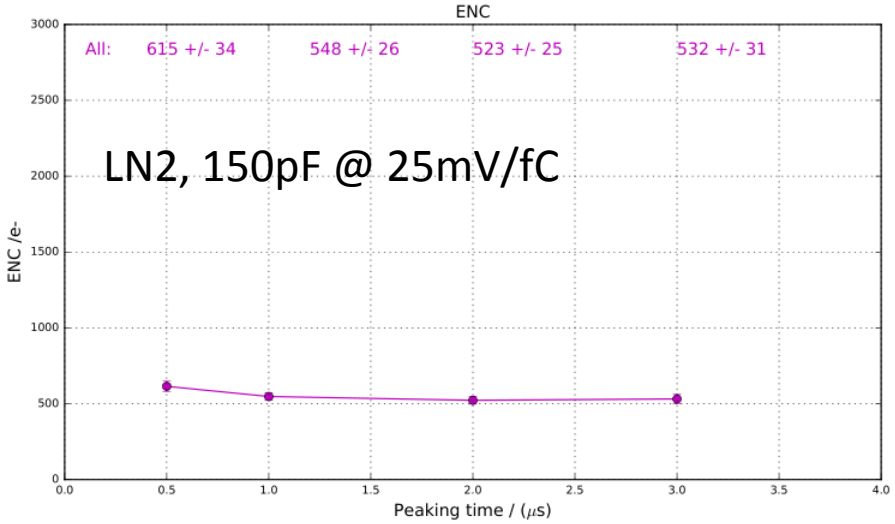
Cold LV cable

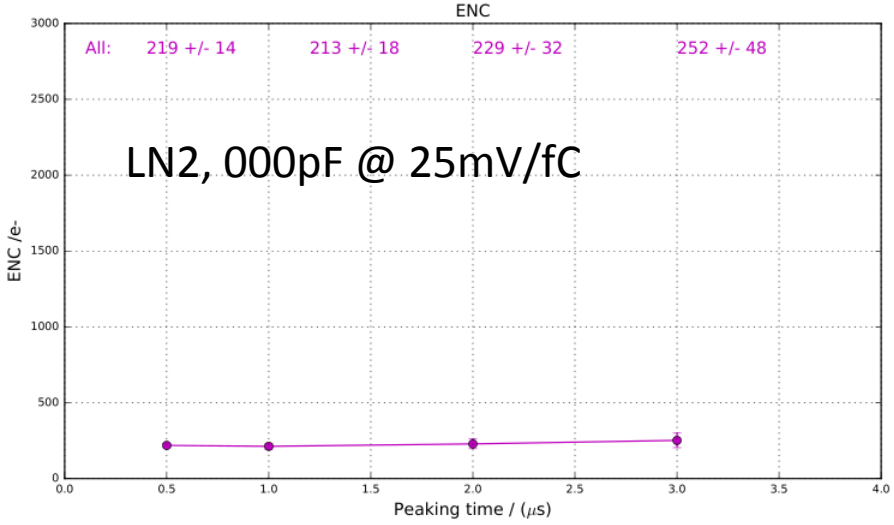
- Cold data cable bundle
  - 12 twin-axial 26 AWG copper alloy cables custom manufactured by Samtec
  - 4x1Gbps high speed data links: check up to ~1.3 Gbps at 10-13 bit error rate
  - Clock and control signals and backup JTAG programming for FPGA
- Cold LV cable bundle
  - 9 twisted-pair 20 AWG wires custom manufactured by Samtec
- 50 data/150 LV cold cable bundles have been delivered to BNL and will be cryotested (remaining data cable bundles have already been ordered)

P2 FEMB ENC Performance



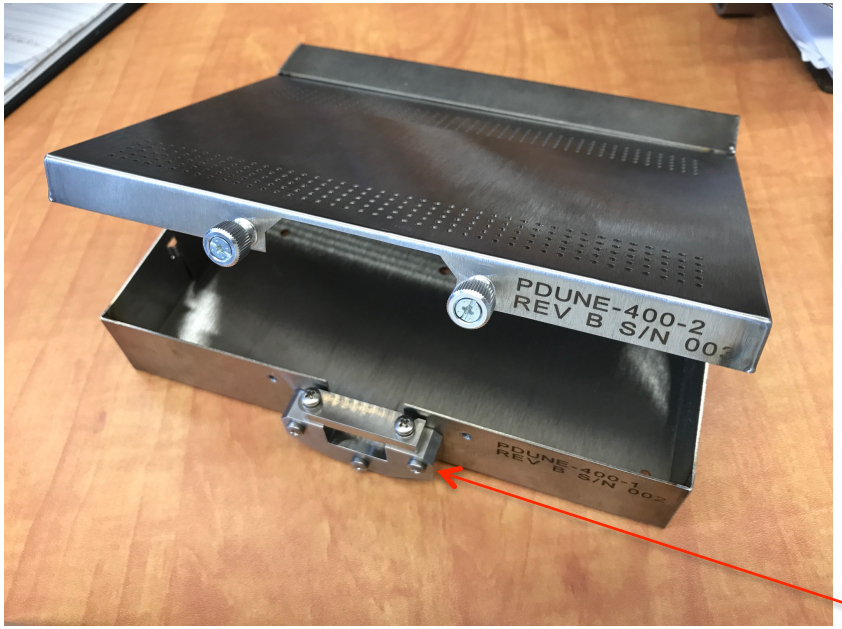




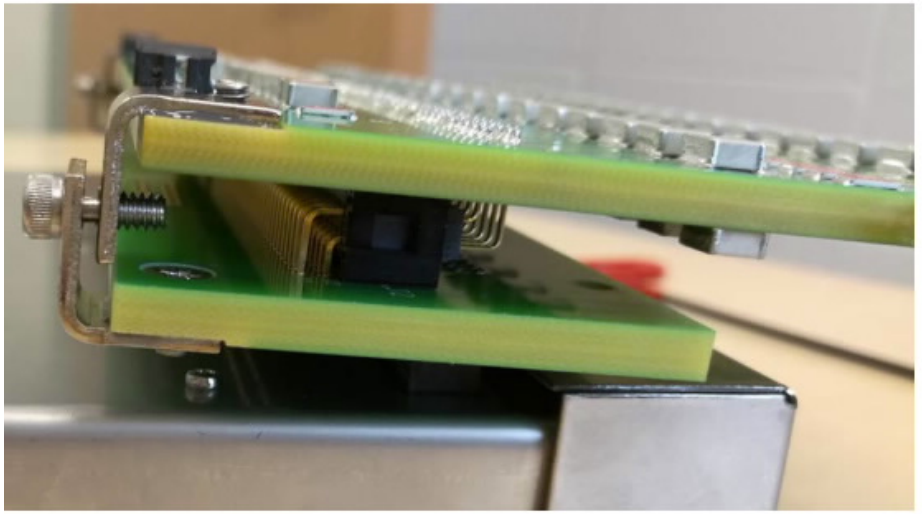


CE Box

- CE Box encloses FEMB and provides cable strain relief and attaches to APA
  - Drawings are complete and posted to DUNE DocDB 2611
  - 3 prototypes have been received at BNL
  - Will be tested under multiple thermal cycles for damage or loss of cable connectivity
- One prototype was machined at BNL and assembled with a CR board and PSL adapter
  - Passed six slow cold cycles and one thermal shock with no continuity issues at data connector



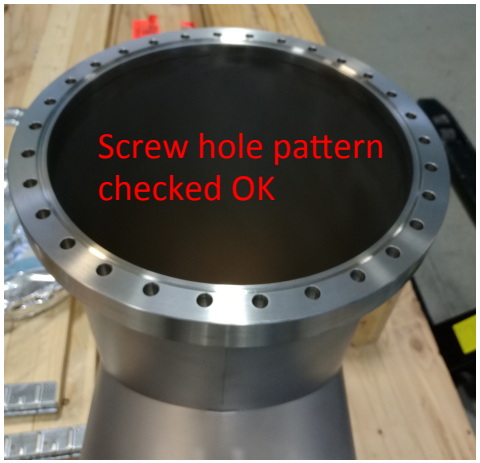
Clamp for data and LV cable

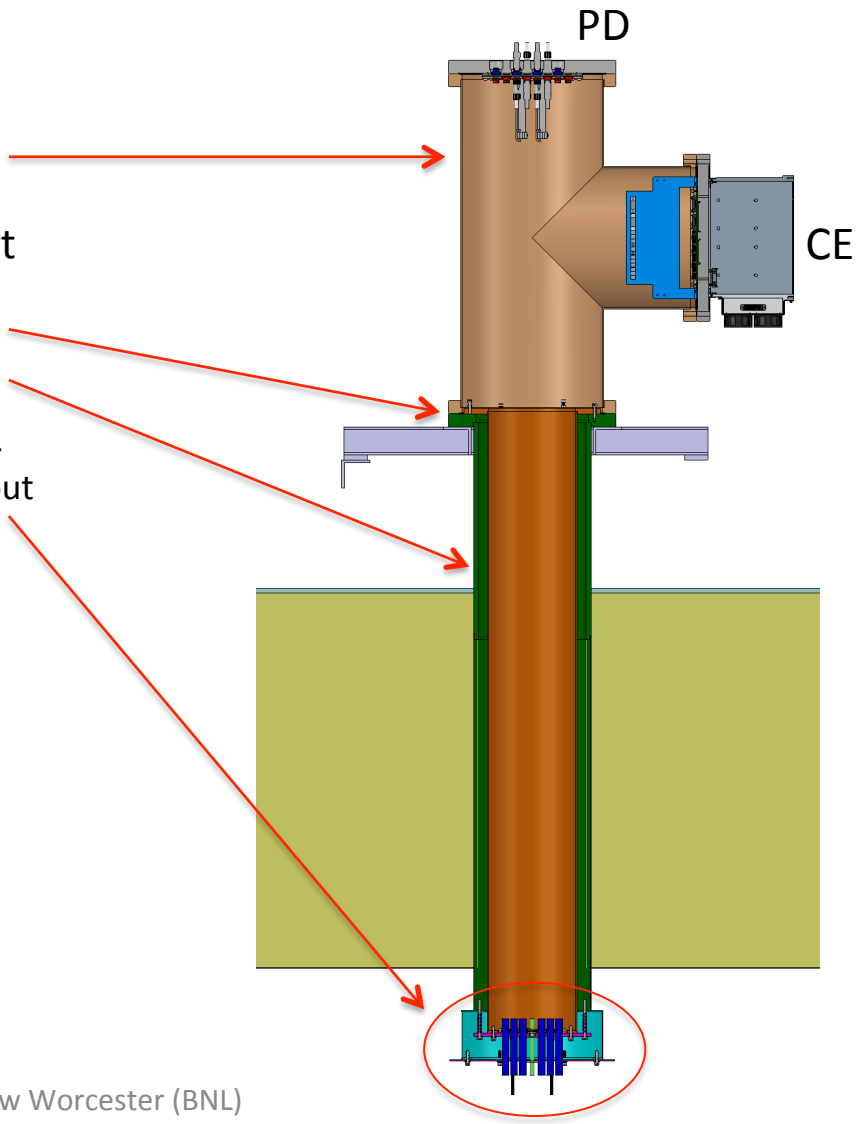


Top to bottom: CR board, PSL adapter, CE Box

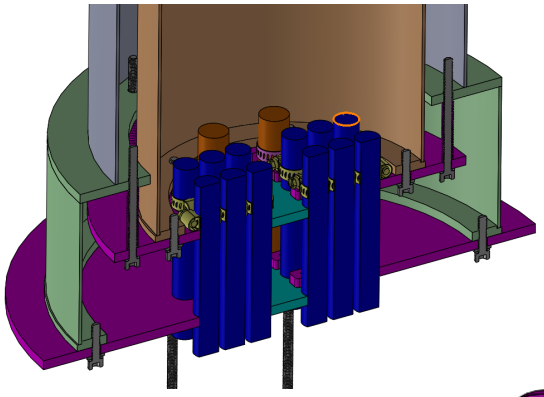
Signal Feed-through

- ProtoDUNE-SP signal feed-through has two major parts
  - Tee pipe with 14” Conflat flanges to attach CE and PD flanges
  - Crossing Tube Cable (CTC) support
    - Attaches the top of 14” Conflat flange of crossing tube from CERN
    - Thin inner tube also controls GAr flow in ullage
    - Provides cable strain relief at lower end of cryostat crossing tube without touching tube
- 10 final Tee pipes ordered





CTC Support



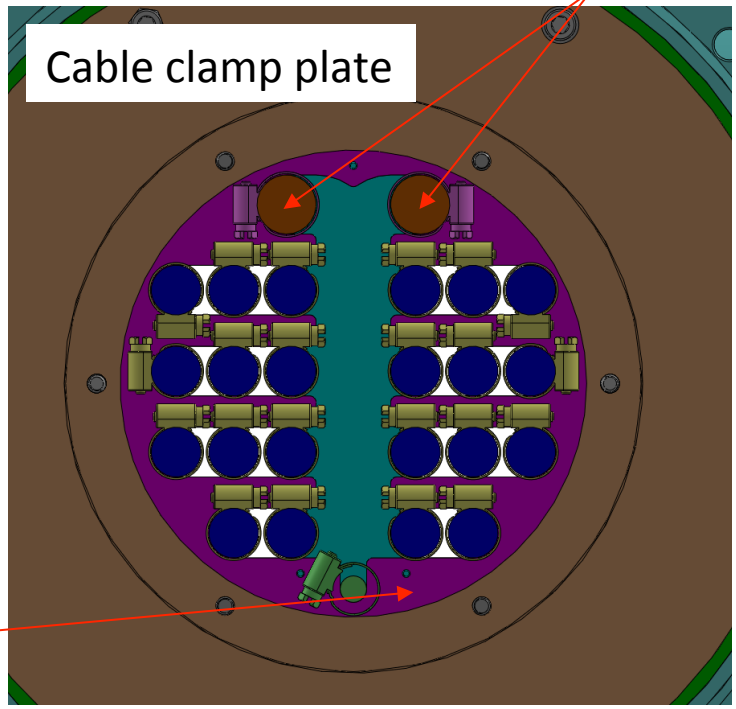
Assembled view

Exploded view of the lower end of the feed-through chimney

CTC drawings posted to [DUNE DocDB 2883](#)
2 prototypes ordered

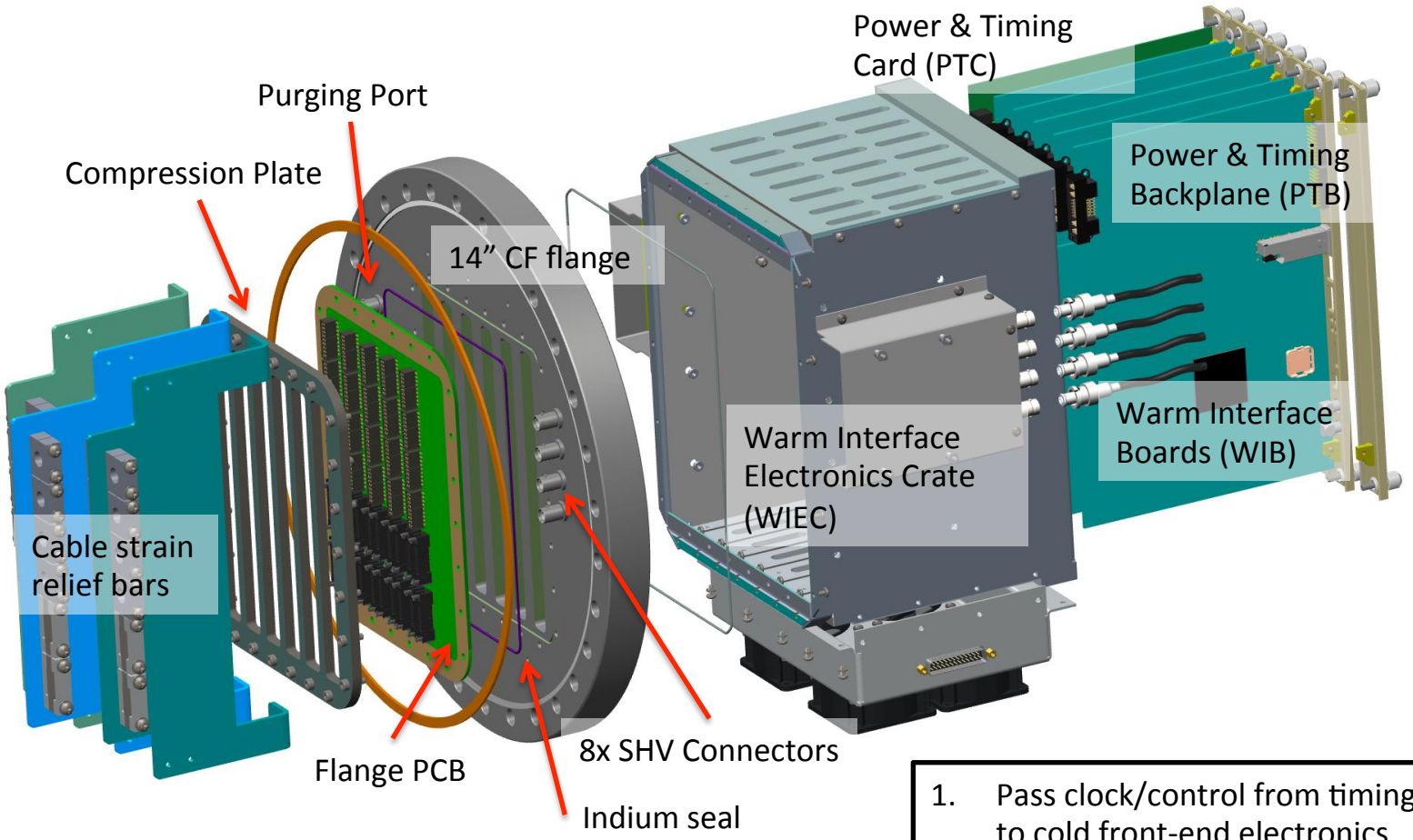
Looking down through inner tube at Clamping Plate:

PD cable bundles



HV cable bundle

CE Warm Components



1. Pass clock/control from timing system to cold front-end electronics
2. Deliver high-speed TPC wire data from cryostat to DAQ

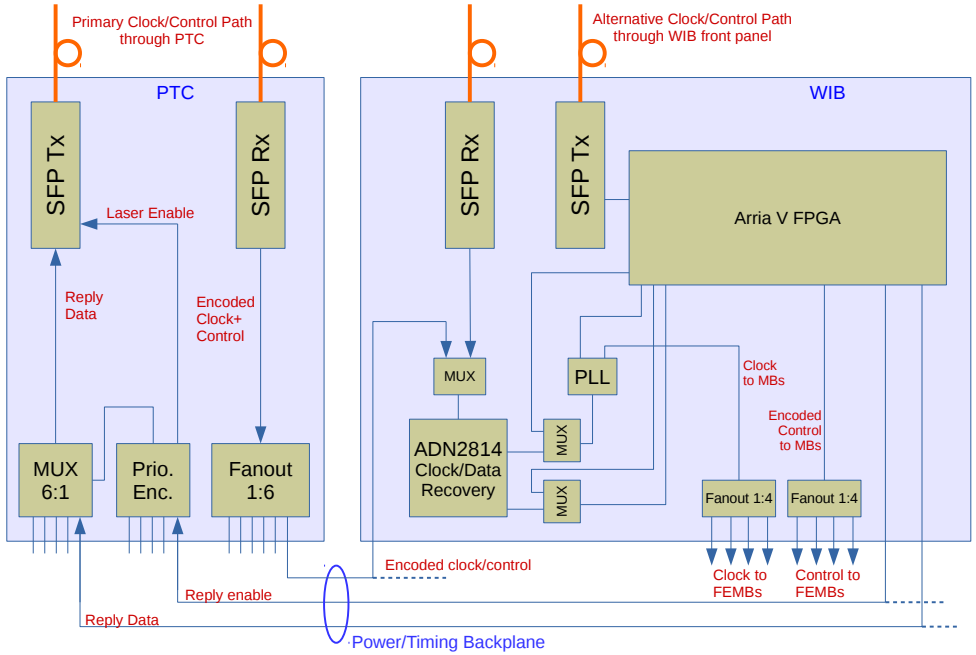
3. Connection to detector ground at CE flange
4. Pass wire-bias and FC HV to cryostat

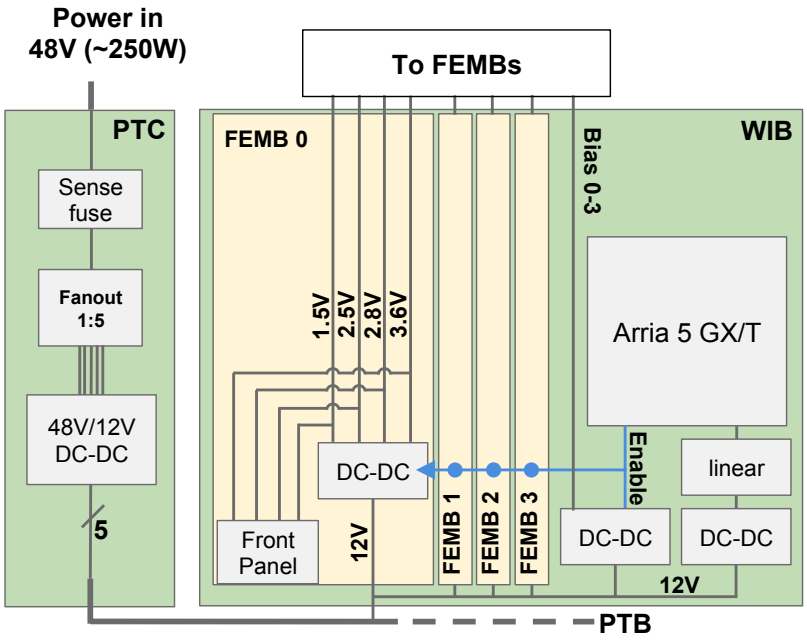
Warm Electronics

PTC receives the timing and control from the 50 MHz encoded system clock and fans it out to all WIB in WIEC over the PTB

WIB sends timing and control to 4 FEMBs and receives high-speed TPC data over cold data cable and transmits it to the DAQ systems over optical fiber

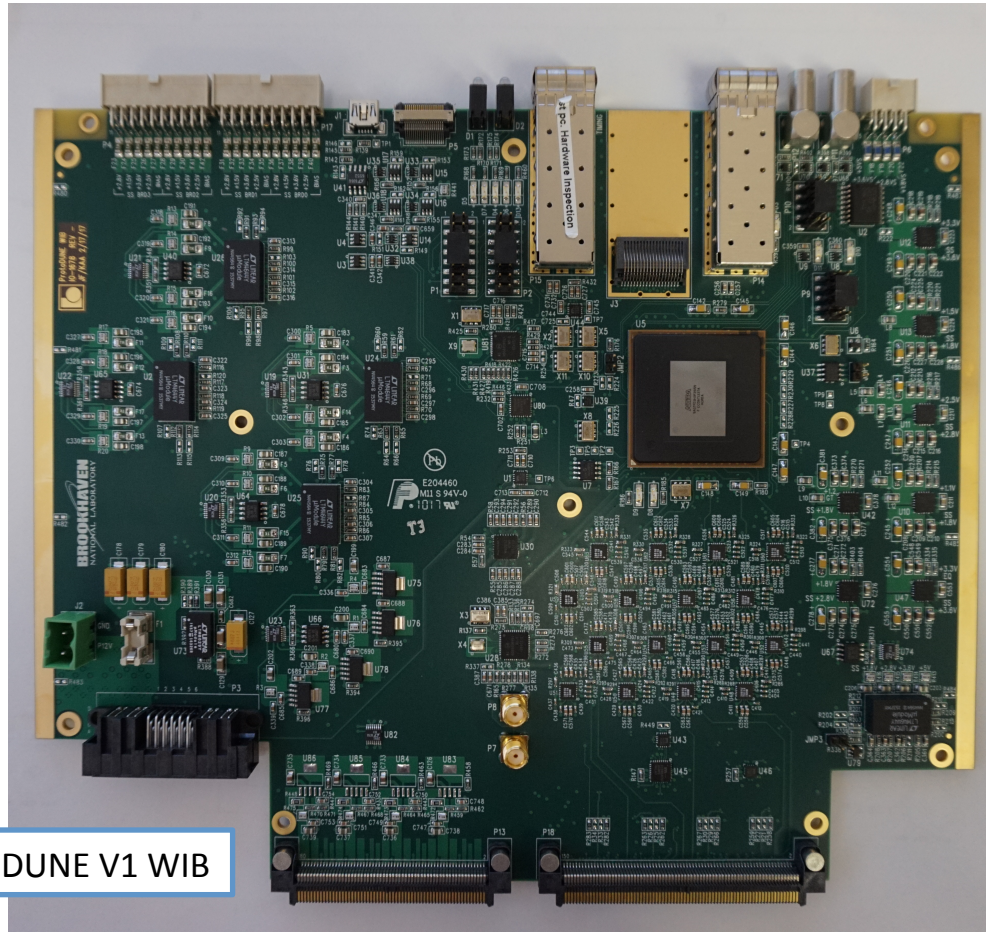
PTC receives 48VDC from LV power units, steps it down to 12VDC and fans it out to WIB over the PTB, WIB steps 12VDC down to VDC required for FEMB and provides LV power over cold LV cable





WIB

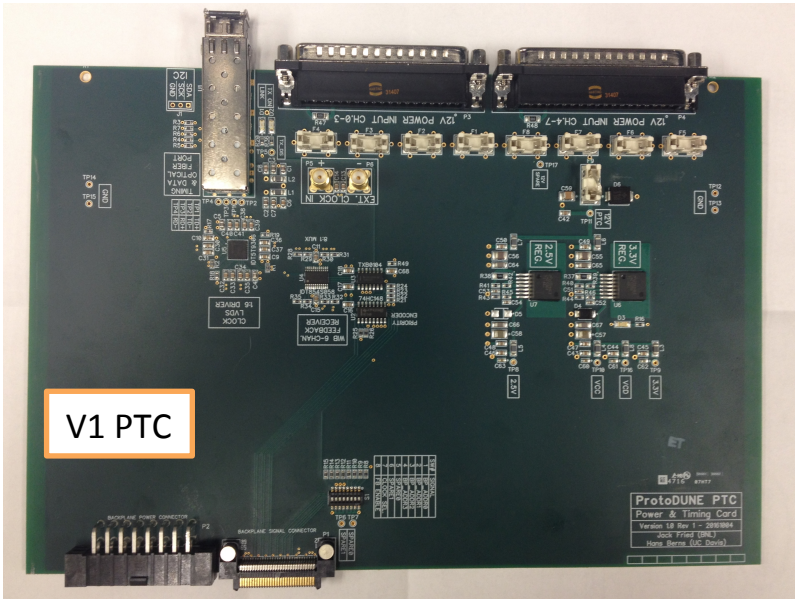
- Collaboration between BNL (hardware) and Boston University (firmware)
- V1 WIB schematics and layout in DUNE DocDB 3327
- Current status
  - Integration/noise measurements ongoing with SBND WIB at Fermilab and BNL
  - ProtoDUNE V1 WIB received and tested at BNL
    - Arria V GT variant FPGA (10 Gbps links)
    - ProtoDUNE clock/data separator
  - 1 WIB delivered to BU
    - Firmware development for communication with FEMB, DAQ and timing system
- V2 WIB with small improvements for noise performance in layout

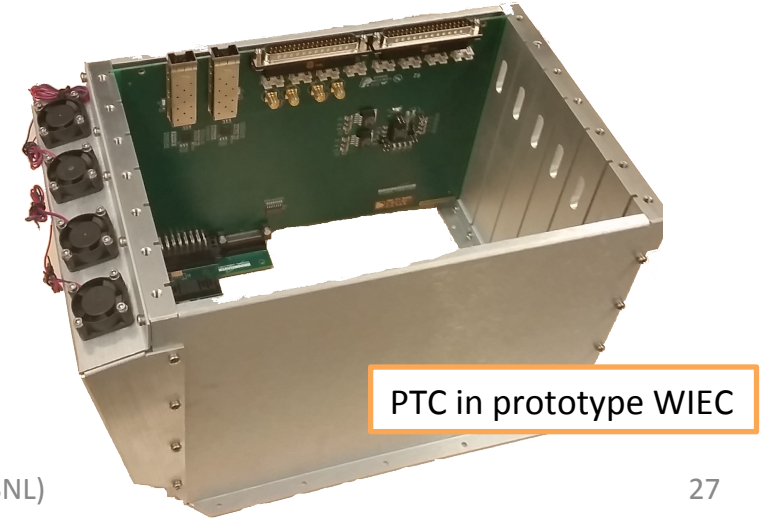


ProtoDUNE V1 WIB

PTC

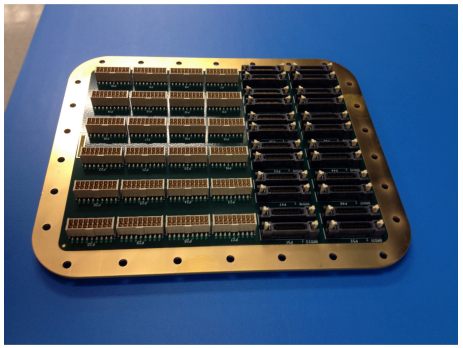
- V2 PTC schematics and layout in DUNE DocDB 2988 (UC Davis)
  - 2 variants for 2 options for 48/12V DC converters
    - V2-A: with Vicor "Cool Power" Pi3546
    - V2-B: with Linear Tech. LTM8064
- Current status
  - Integration/noise measurements ongoing with SBND WIB and V1 PTC at BNL
  - ProtoDUNE V1 PTC received and tested at BNL
  - V2 prototype order shipped 6/22
- PTB:

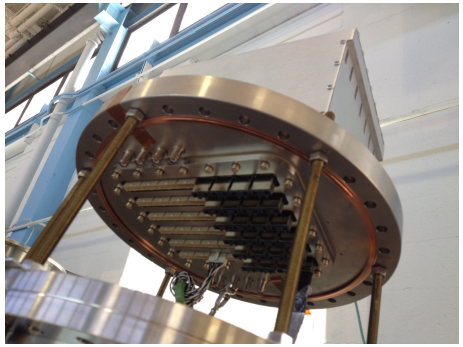


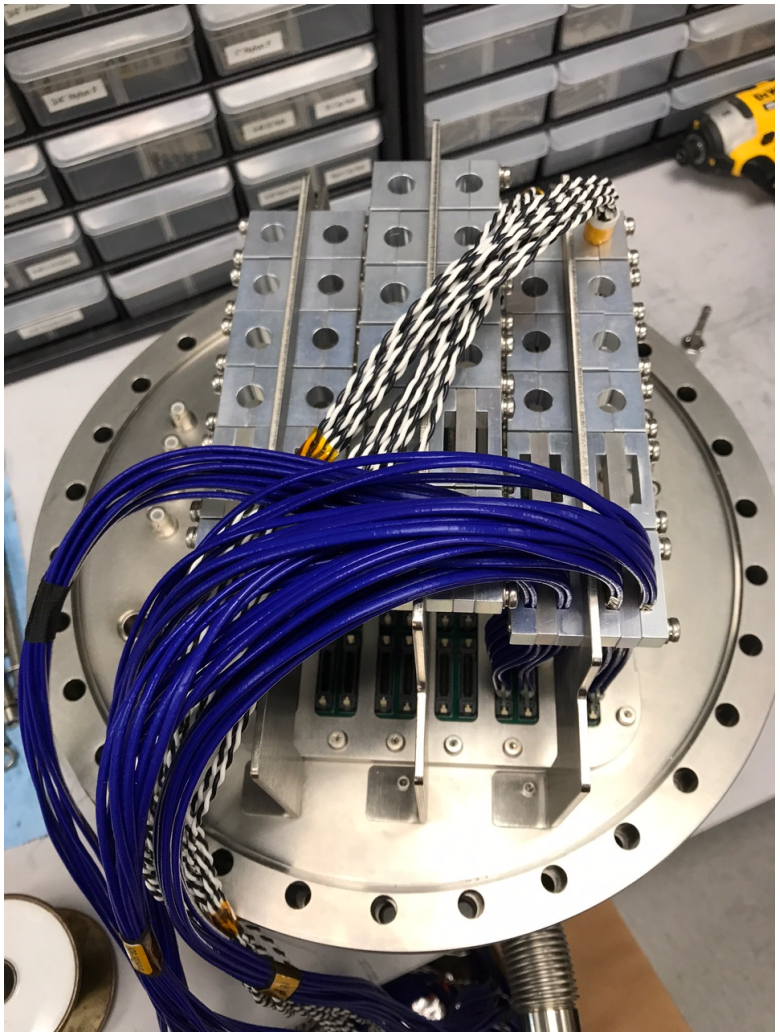


CE Warm Flange

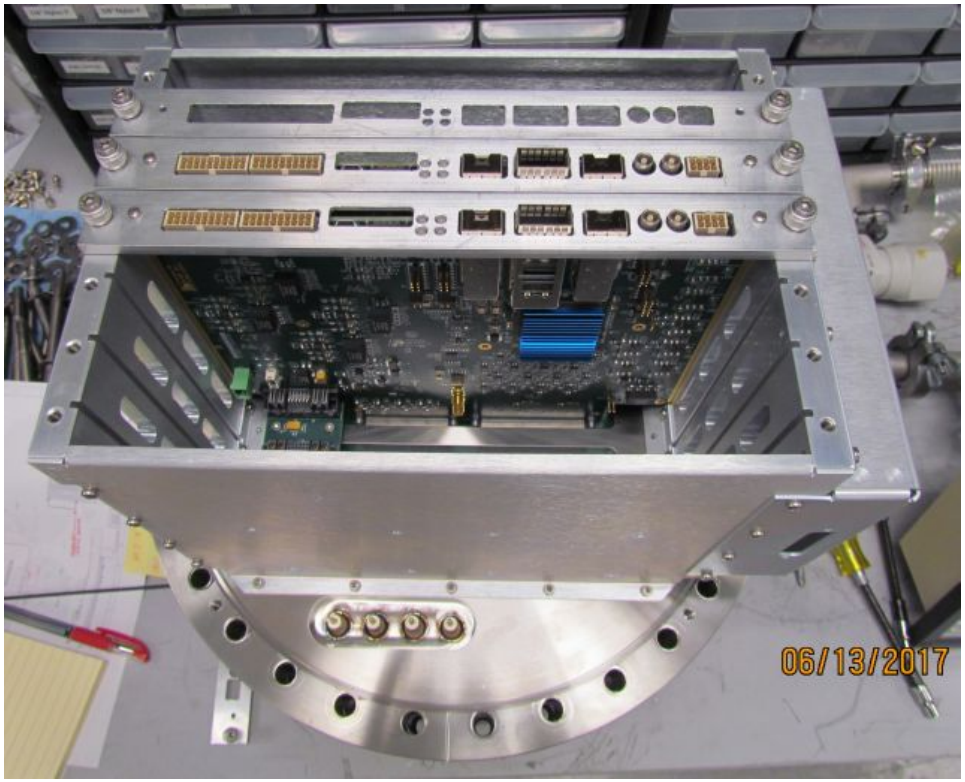
- Mechanical and assembly drawings in DUNE DocDB 2771
- Current status
  - Leakage tests passed up to 10^{-9} leakage rate with 5 PSI differential pressure applied to GAr side of the flange: DUNE DocDB 1809
  - 2 final prototypes have been received at BNL
  - Strain relief support hardware on the flange has been received
- Flange PCB schematics posted to DUNE Doc 2777
  - PCB fabrication done
  - 3 have been assembled



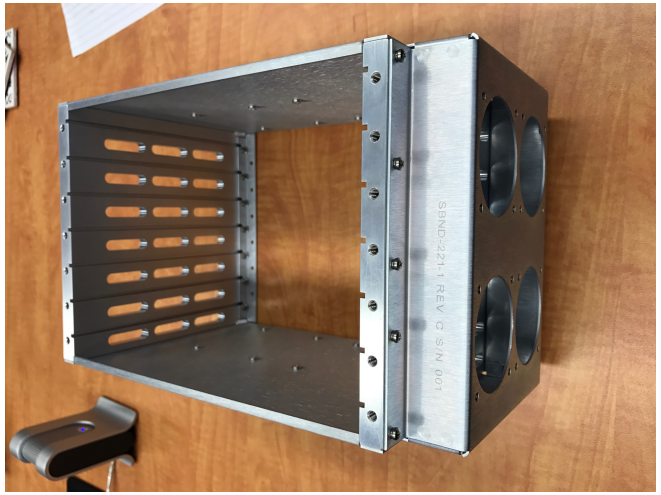




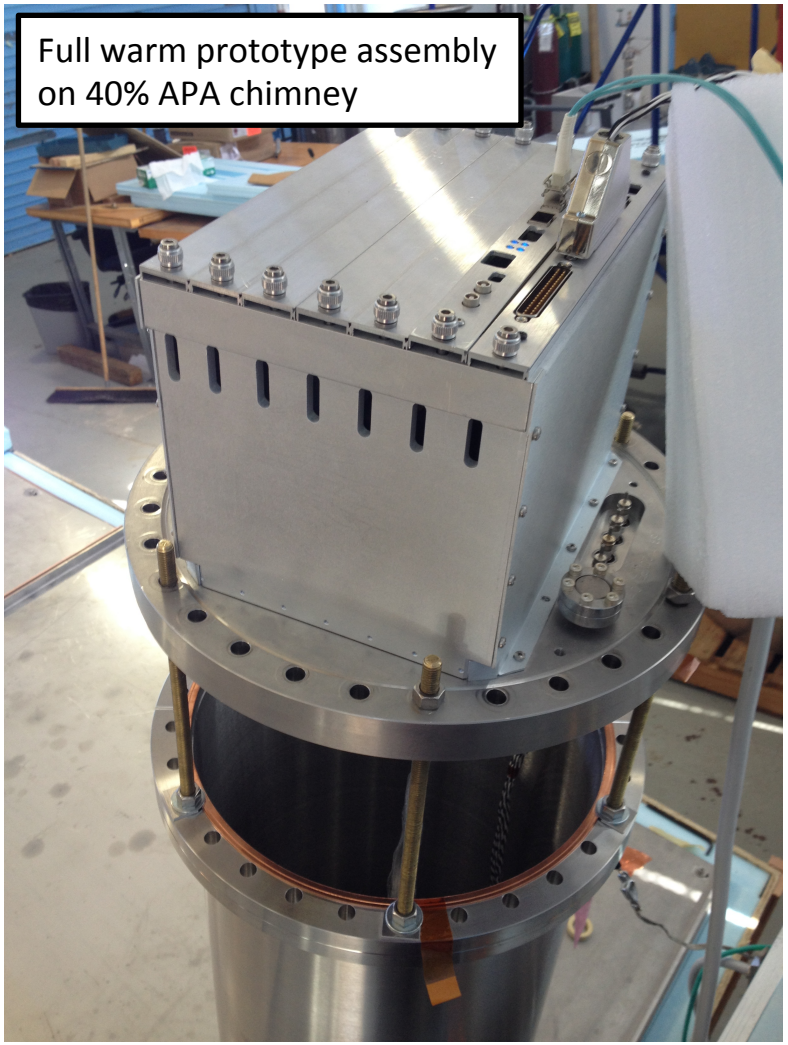
WIEC



- Mechanical and assembly drawings in DUNE DocDB 2774
- Current status
  - 1 prototype machined by Zober Industries and assembled and tested at BNL
  - System tests ongoing with full CE flange assembly and FEMB on the PSL 40% APA
  - 2 final prototypes delivered and one assembled and mechanically tested with WIB and PTC

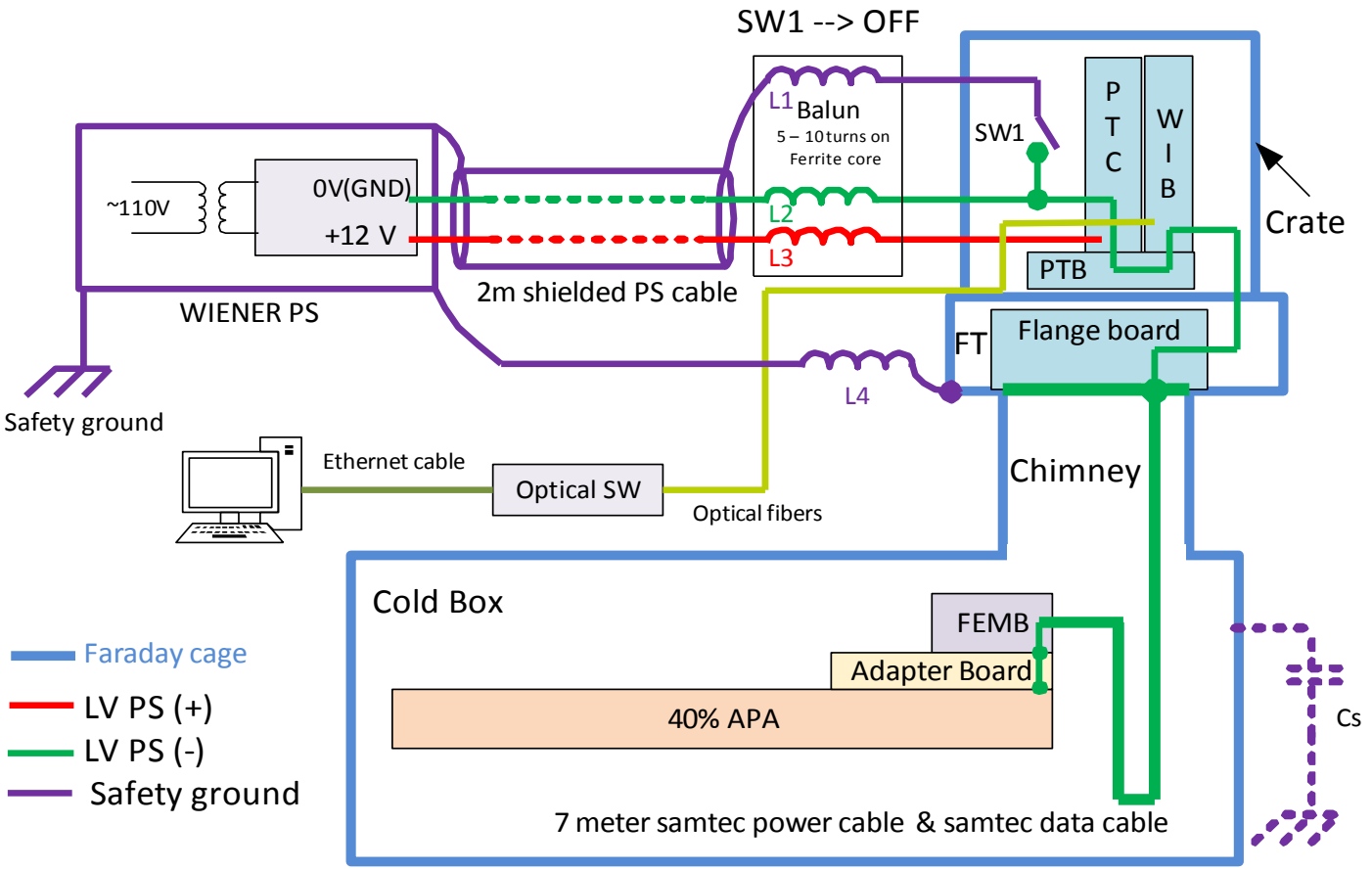


BNL Cold Integration Teststand



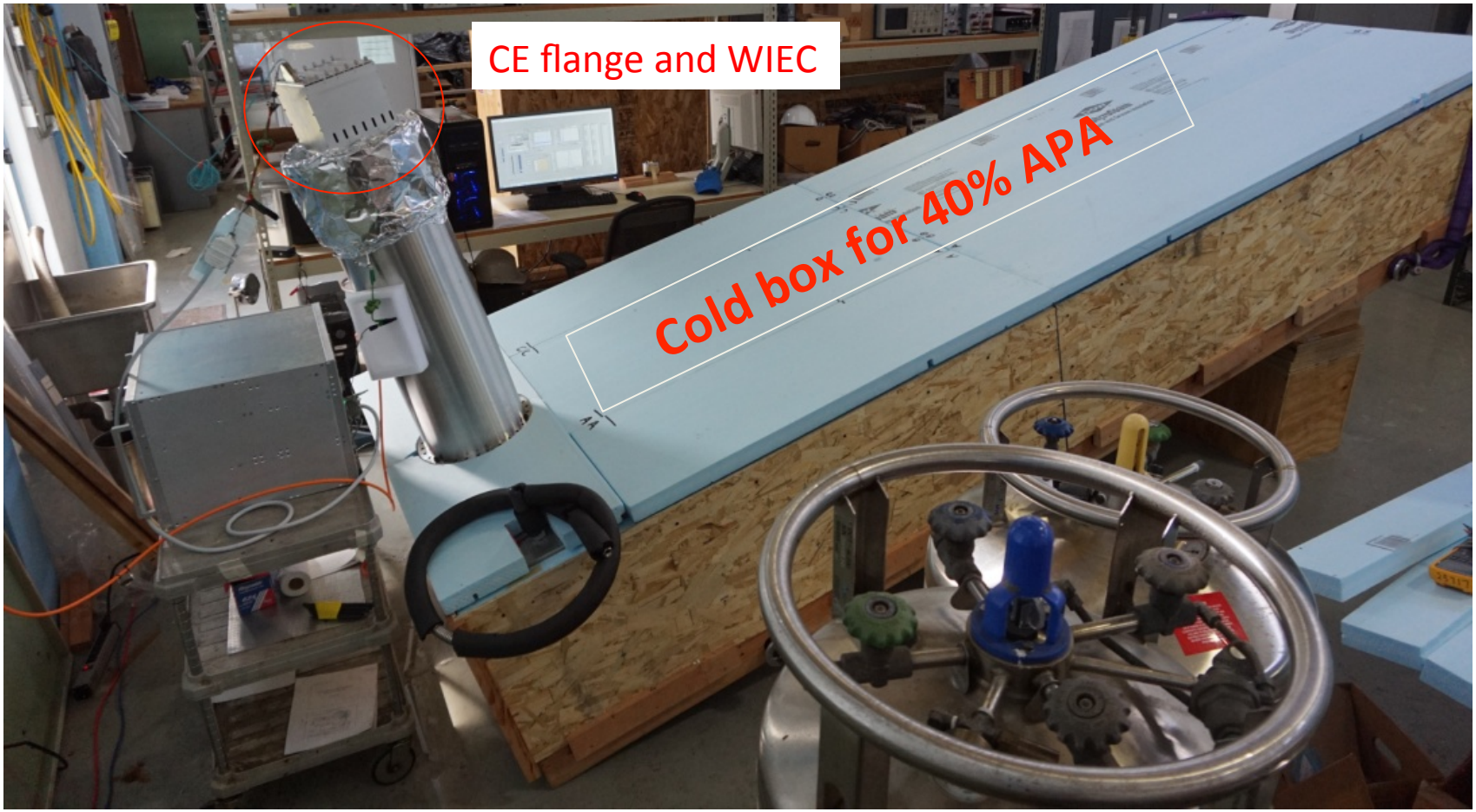
- 40% APA in cold box at BNL
- Full prototype CE system readout
  - WIB/PTC/PTB in WIEC
  - Wiener LV power supply delivering 12V to PTC
  - WIB readout via optical fiber to DAQ PC
    - Internal clock on WIB
  - Prototype CE flange
    - Purge port and SHV connectors on warm side
    - Flange PCB and squash plate on cold side
  - Cold LV and data cable bundles to FEMB on APA wires
    - Maximum 4m wire length
- Grounding scheme for low noise performance has been developed
  - LN2 cycle testing since late April
  - Improvement ongoing…

BNL Cold Integration Test Stand

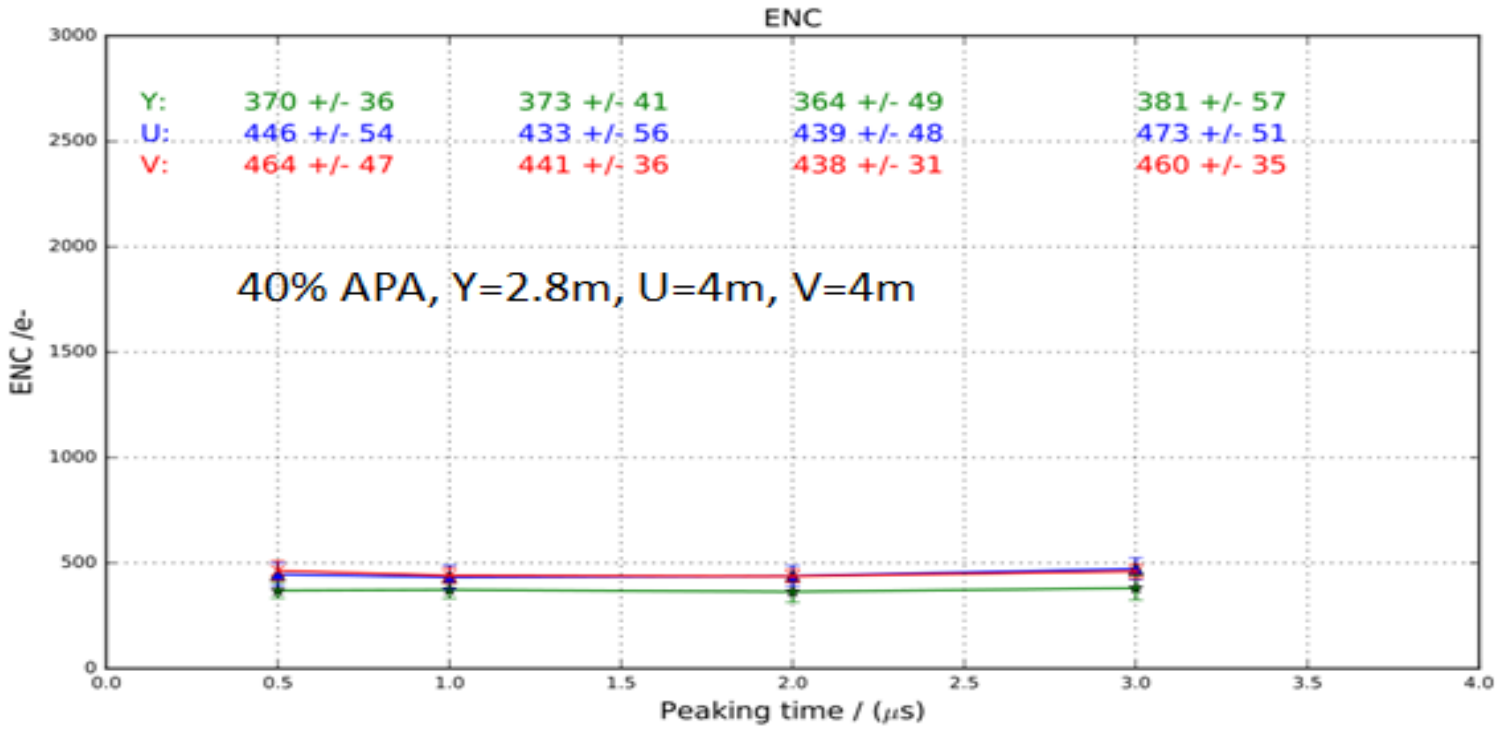


- Following grounding and isolation rules for ProtoDUNE-SP

BNL Cold Integration Test Stand



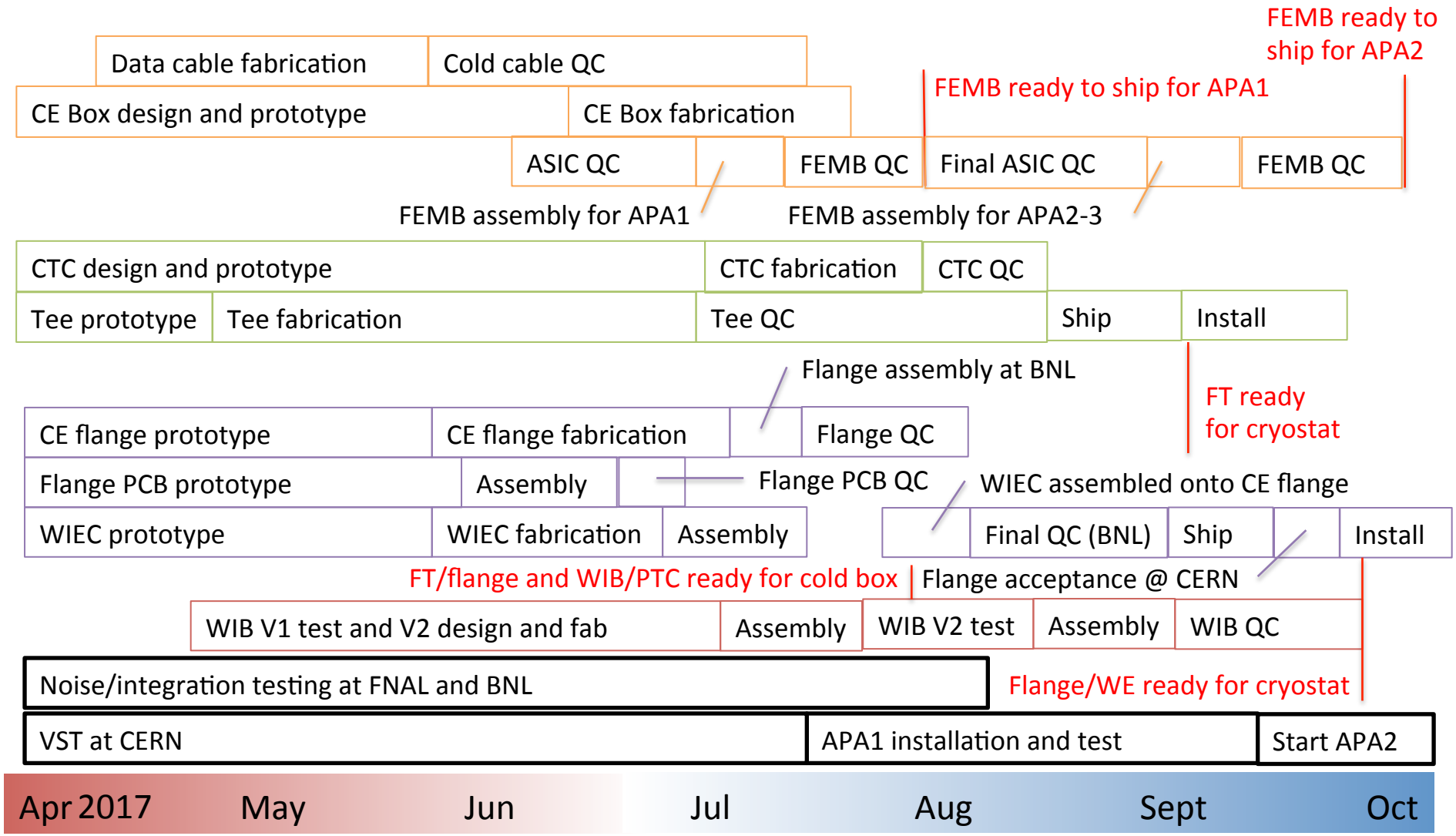
40% APA Preliminary Results



- 4 FEMB operating and all 7m cables submerged in LN2
  - APA wires in nitrogen gas
- Extrapolate to longest DUNE wire (7.5m): ENC < 900 e- at 1 µsec shaping time

CE installation
- APA1: 8/7
- APA2: 11/2
- APA3: 11/10

CE Schedule



Conclusions

- The APA+cold readout+Faraday Cage/Feedthrough with Warm Interface and Local Diagnostics should be treated as an integrated whole and installed as such
  - Coordinated TPC grounding and shielding between CE, PD, APA, CERN teams
- All components have final prototypes or are in fabrication
- QC plan for validation at BNL in place: DocDB 1809
- Installation steps have been mapped out and discussed at April installation workshop
- Shipping to CERN
  - Handled by Interfreight, an experienced broker, to CERN directly
  - Done for ATLAS LAr Calorimeter electronics for 10+ years
  - Custom packaging for FEMB and CE flange units will be designed and built by BNL team that installed MicroBooNE