

LIGHT READOUT ELECTRONICS CURRENT STATUS

Cayetano Santos

On behalf of the IN2P3 group - ACP/Omega/LAPP

WA105 Bi-weekly meeting - 10 April 2017

OUTLINE

1 SINCE LAST MEETING . . .

2 SUMMARY

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② SUMMARY

FMC MEZZANINE SCHEMATICS STATUS

- **Back-annotations needed to modify the schematics**
 - accommodate spare signals handling
 - pinout to facilitate routing
- Spare signals
 - Threshold set to 1.5 V and - 400 mV.
 - Software selectable
- Minor bug fixes

Status: done

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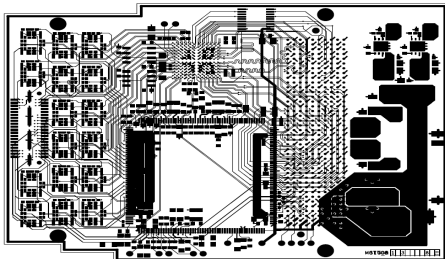
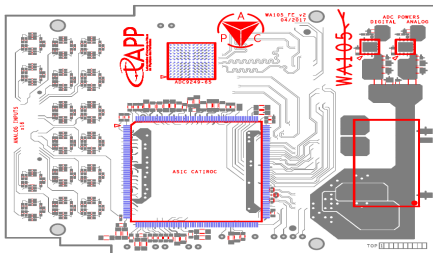
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FMC MEZZANINE ROUTING STATUS

- Delayed due to strong constraints
- Limited number of IOs
- Electric standards between FPGA banks and ADC outs
- Trace lengths, impedance matching, etc.
- VHDL capture code must be compatible with routing

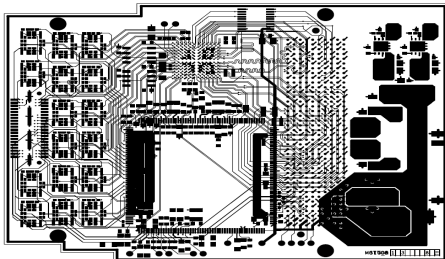
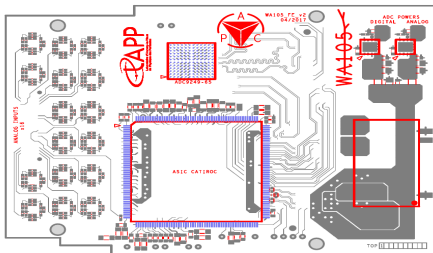
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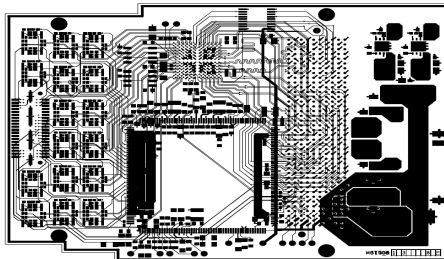
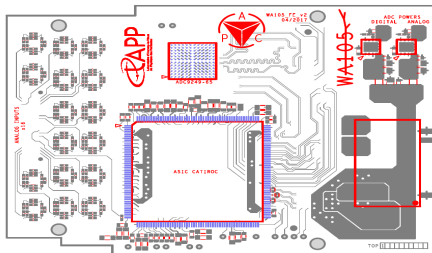
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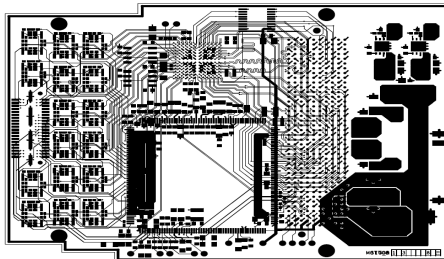
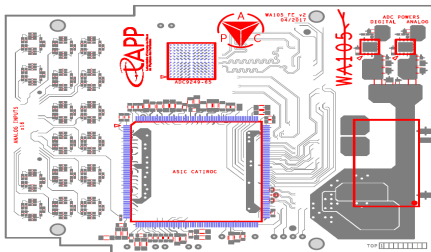
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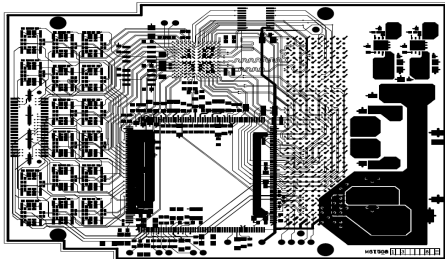
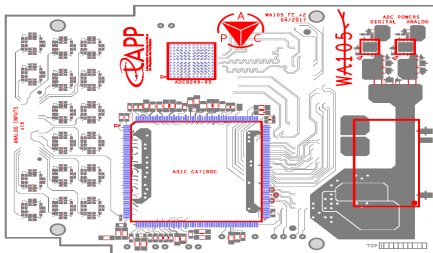
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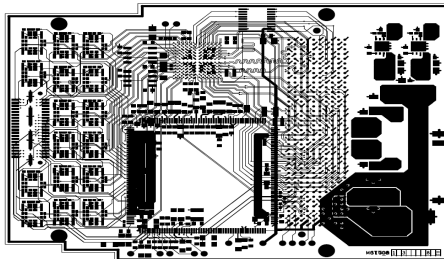
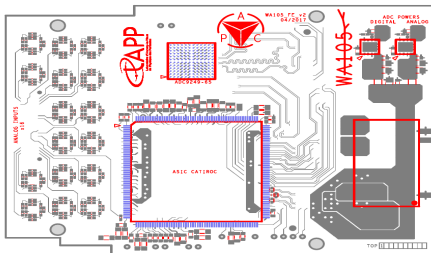
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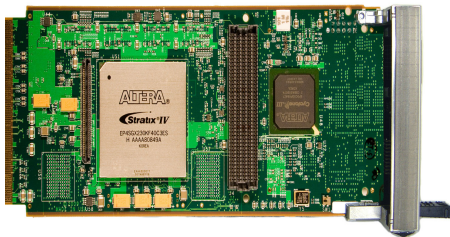
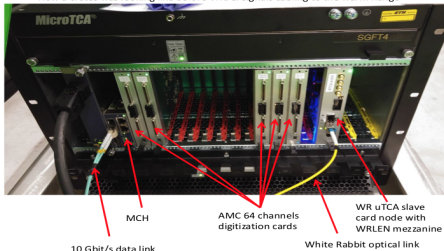
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DO THE SHOPPING

How a crates was looking like before VHDCI signals cabling to the warm flange



- New uTCA crate
- Third AMC from Bittware (3 times 12 channels)

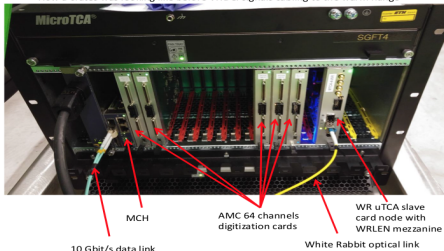
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- Samtec front panel connectors
- Parts for production

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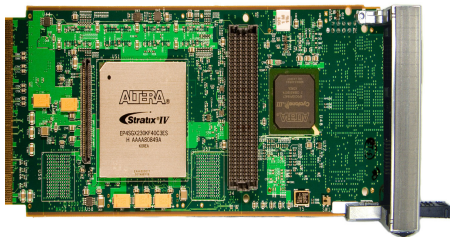


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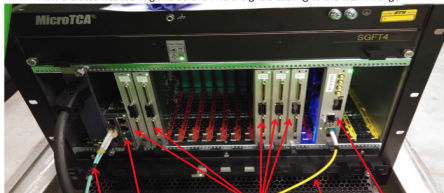
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AMC 64 channels
digitization cards

WR uTCA slave
card node with
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White Rabbit optical link

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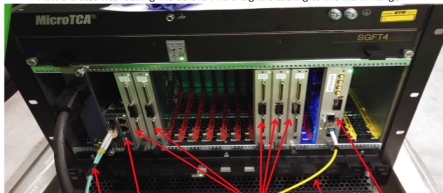


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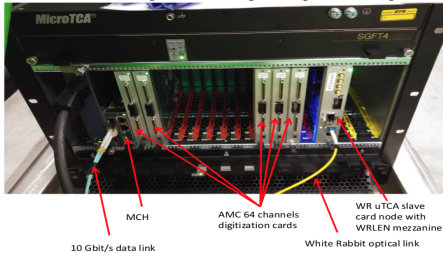
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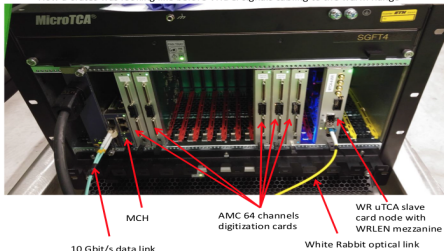


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ANY OTHER BUSINESS

Status: Almost there !

We will propably lend a CatiROC test board to CIEMAT

- Testing the new board

- Test the new board
- Test the board with the new board
- Test the board with the new board

- Firmware

- Implemented new functionality: new and merged trigger

ANY OTHER BUSINESS

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- asic alive
- board noise
- global behaviour

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