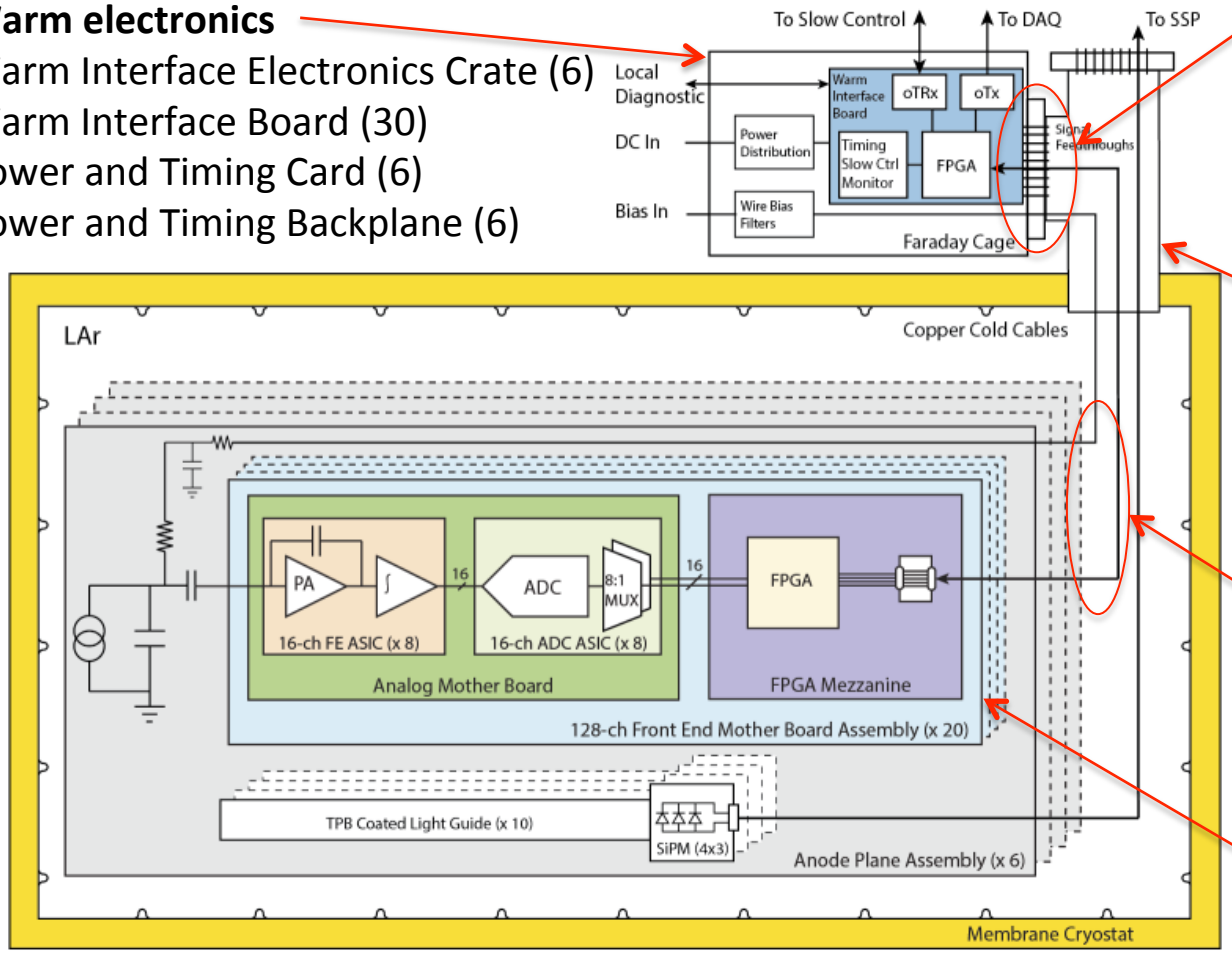
ProtoDUNE-SP CE Status Report

Matthew Worcester (BNL)

DUNE FD Cold Electronics Meeting
6/12/17

ProtoDUNE-SP Cold Electronics

Warm electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

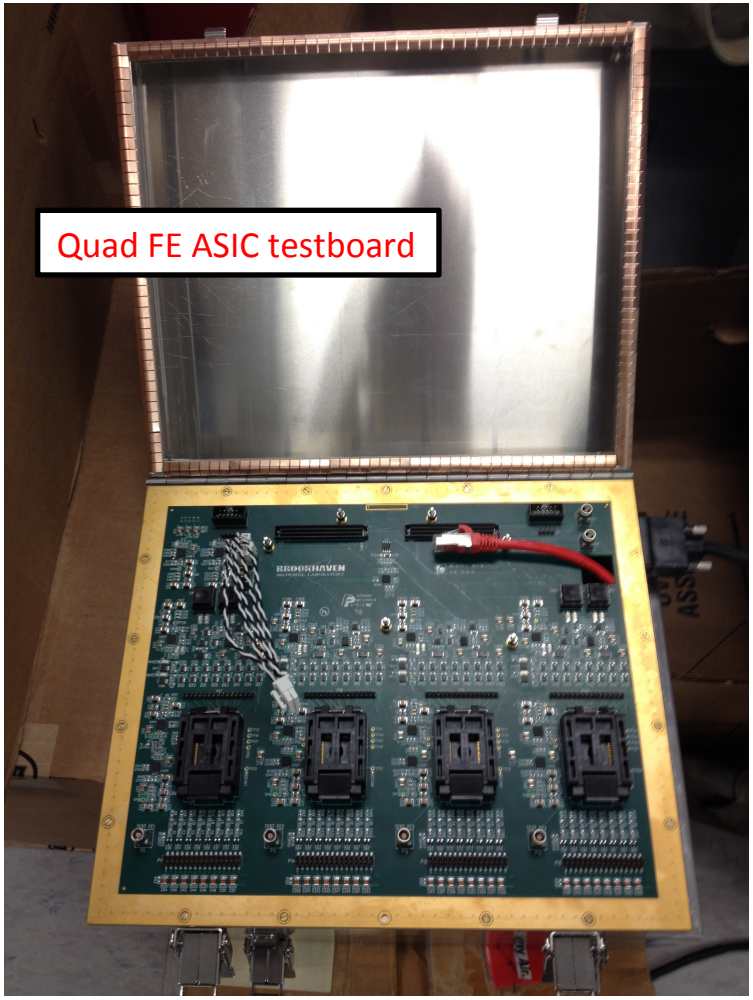
Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable to FEMB
LV and data cable (120+120) and APA wire-bias SHV cable (48)

Front End Motherboard
(FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

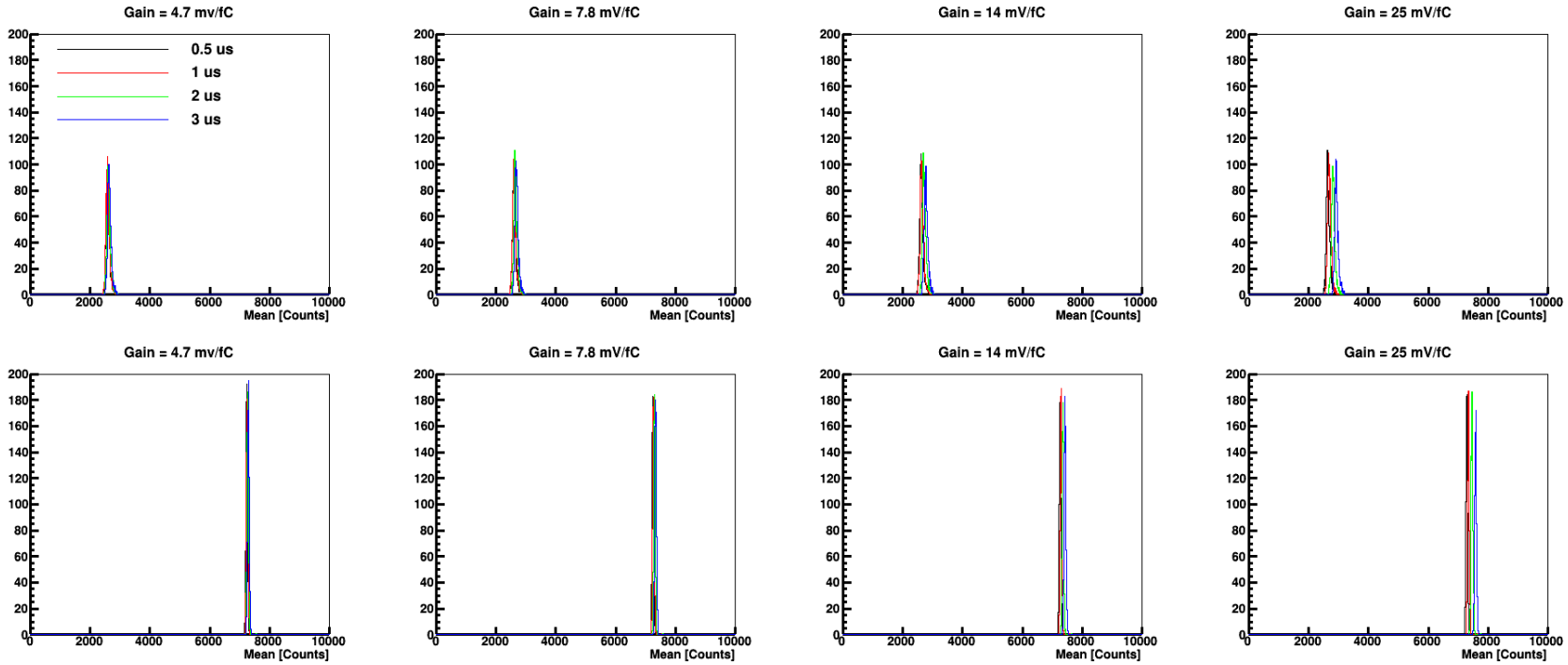
FE ASIC

- P2 FE ASIC
  - 268 P2 FE ASICs for APA1 tested warm and all pass with no dead channels
    - 2 quad socket P2 FE ASIC testboards running on QC teststands
    - Final testing code and selection cuts being optimized
  - Setting up to start cold FE ASIC testing this week
    - Cryo yield of ~10% will be tested
    - MSU dewars expected to arrive this week
- Production ASICs expected to be delivered by end of June



Baseline Summary: 6/8-9

Mean baseline, raw 14-bit ADC counts, all channels, top row: 200 mV; bottom 900 mV



All data taken with good test runs very uniform: baseline, gain, and ENC

QC Testing

- 4 QC teststands are running at BNL: 2 FE and 2 ADC ASIC
  - 2 shifters from University of Florida have been testing FE ASICs
  - New shifters from MSU, Houston this week
  - Justin (LSU) finalizing the ADC teststands
  - Brian Kirby (BNL) finalizing the FE teststands
  - Mailing list:

mailto:ce-teststands-l@lists.bnl.gov

  - Weekly shift meetings on Fridays, 2 pm ET:

https://fnal.zoom.us/j/766631510

- E. Worcester and M. Bishai shift coordinators
  - Guang Yang (SBU) and Jyoti Joshi (BNL) shift leaders
- Shift calendar to sign up:

https://docs.google.com/spreadsheets/d/15a-QsJhyJppWninh5XQquv_DmerxDRAn_NDW2tmgj4c/edit - gid=494612915

  - Shifters will be trained at BNL
  - CE expertise not required to shift
- Shifts expected to run from June-September 2017

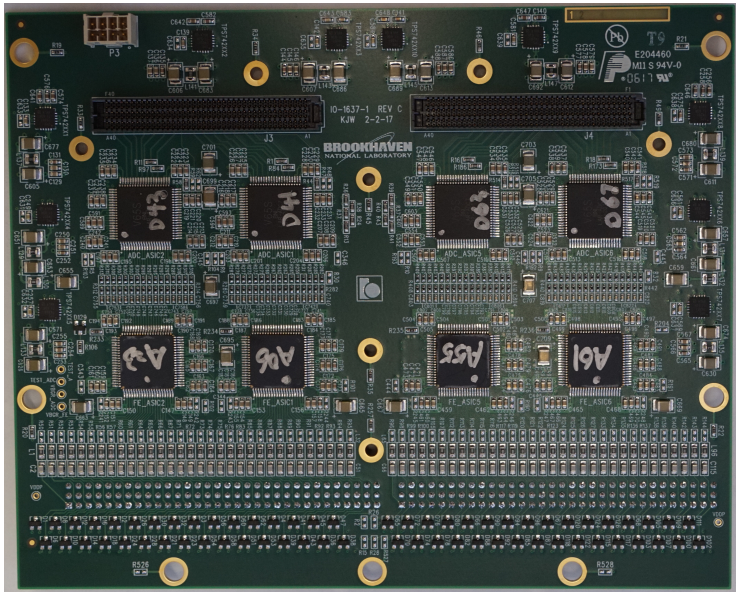
ADC ASIC

- P1 ADC ASIC
  - ~400 P1 ADC ASICs for APA1 expected this week
    - 2 single socket P1 ADC ASIC testboards running on QC teststands
    - Final testing code and selection cuts being optimized
  - After warm check, all ADCs will be tested in LN2
- Production ASICs expected to be delivered by end of June
  - Quad socket ADC testboards are having firmware developed and will be tested

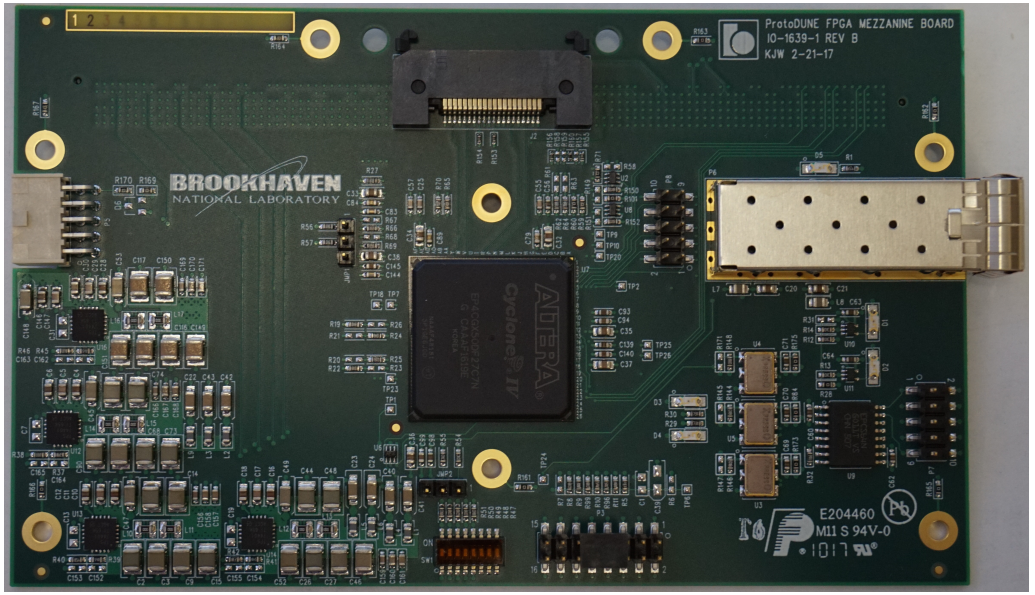
FEMB

- 6 total P2 analog motherboard (with P2 FE/P1 ADC) have been delivered
  - 1 Gohm resistors no longer required to bring up FE channels
  - External clock to P1 ADC
- 35 FPGA mezzanines have been delivered for APA1 and will be tested

P2 analog motherboard



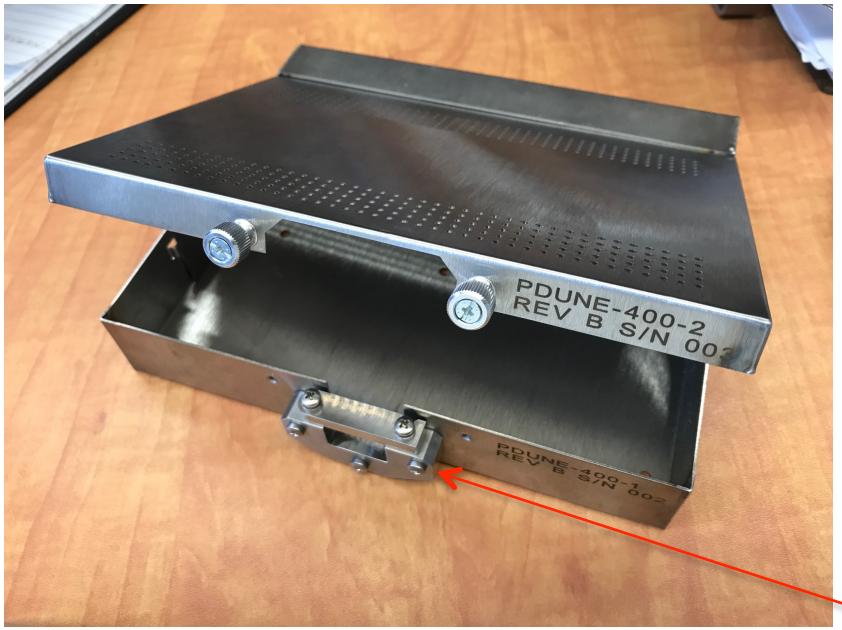
P2 FPGA mezzanine

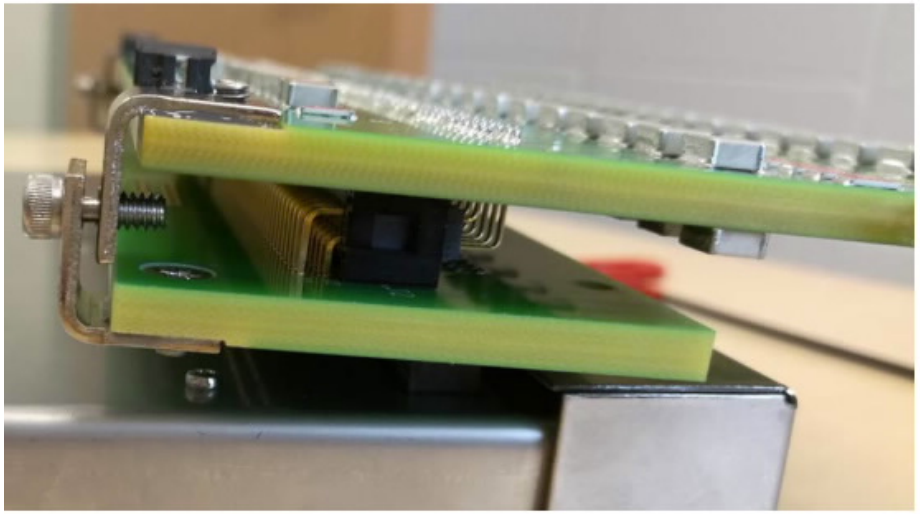


- 50 data/150 LV cold cable bundles have been delivered to BNL and will be tested cold (remaining data cable bundles have already been ordered)

CE Box

- CE Box drawings are complete and posted to DUNE DocDB 2611
  - 3 prototypes have been received
  - Bo will take 1 to PSL for mechanical checks with APA
  - Others will be tested under multiple thermal cycles for damage or loss of cable connectivity
- One prototype was machined at BNL and assembled with a CR board and PSL adapter





Top to bottom: CR board, PSL adapter, CE Box

Clamp for data and LV cable

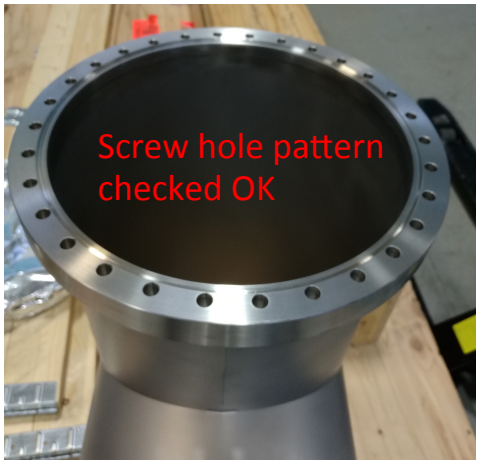
WIB/PTC

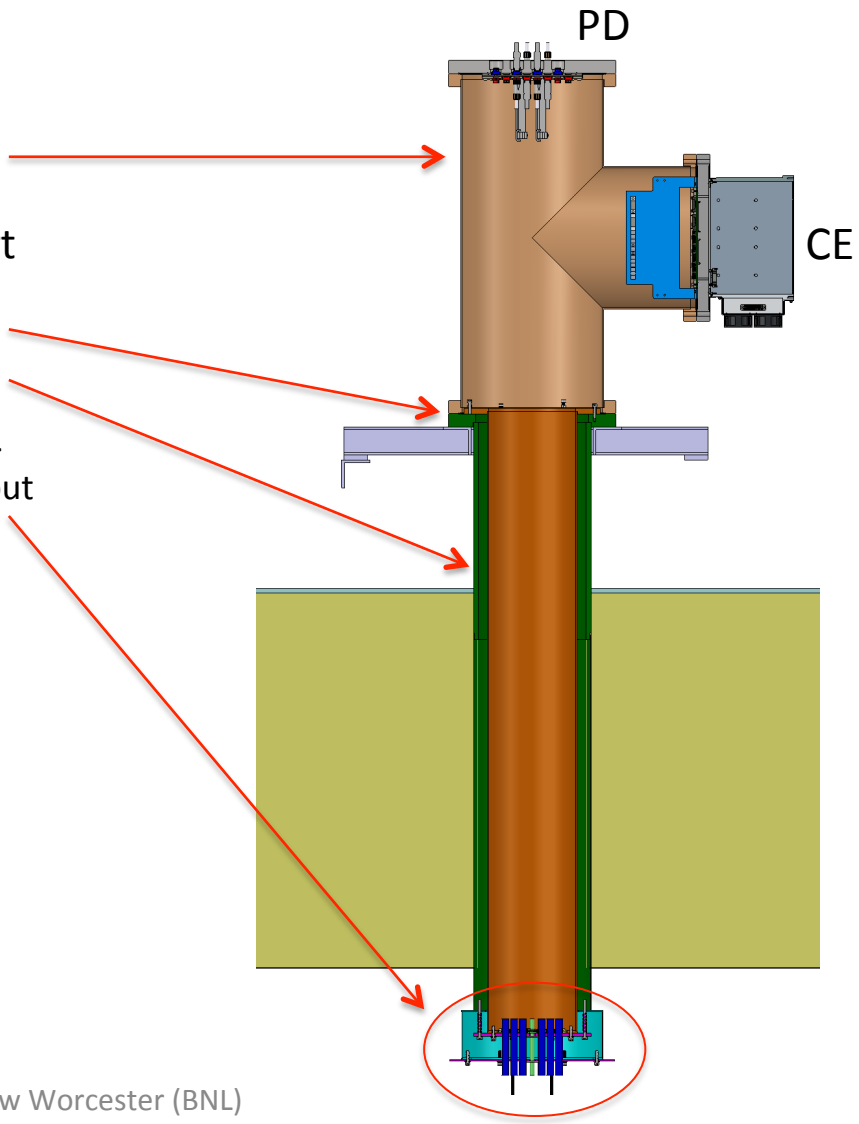
V1 ProtoDUNE WIB

- ProtoDUNE V1 WIB received
  - Arria V GT variant FPGA
  - ProtoDUNE clock/data separator
- Testing with V1 WIB
  - Boston
    - WIB-RCE links working via optical fiber
    - Firmware to work with Bristol timing system now the priority
  - BNL
    - Hardware and 10 Gbps link checks done
- SBND WIB + WIB-RCE optical fiber at CERN for several months
  - V1 WIB will be sent once timing system works on BU and BNL teststands
- P2 version PTC layout complete and posted to DUNE Doc 2988 (UC Davis)
  - 2 variants for 2 options for 48/12V DC converter
    - V2-A: with Vicor "Cool Power" Pi3546
    - V2-B: with Linear Tech. LTM8064
  - V2B fabrication complete and boards will ship to BNL

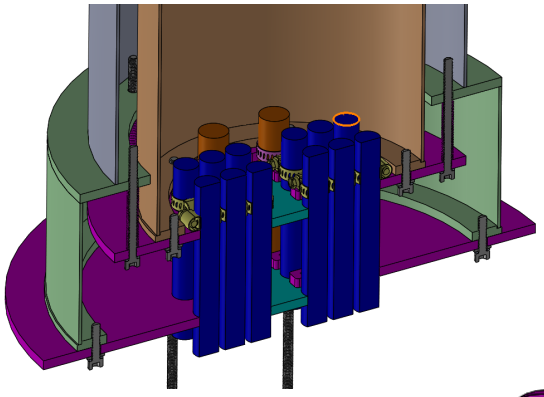
Signal Feed-through

- ProtoDUNE-SP signal feed-through has two major parts
  - Tee pipe with 14” Conflat flanges to attach CE and PD flanges
  - Crossing Tube Cable (CTC) support
    - Attaches the top of 14” Conflat flange of crossing tube from CERN
    - Thin inner tube also controls GAr flow in ullage
    - Provides cable strain relief at lower end of cryostat crossing tube without touching tube
- 10 final Tee pipes ordered





CTC Support



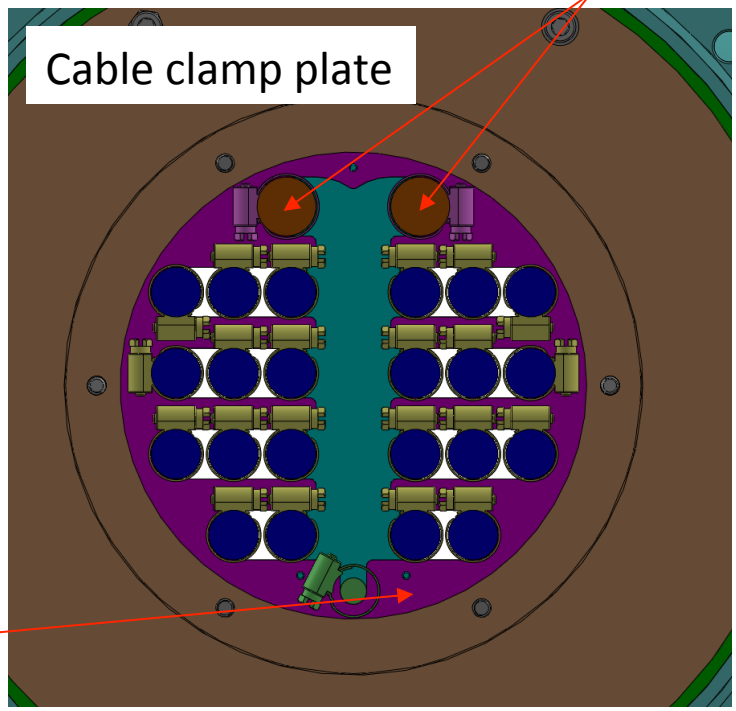
Assembled view

Exploded view of the lower end of the feed-through chimney

CTC drawings posted to [DUNE DocDB 2883](#)
2 prototypes ordered

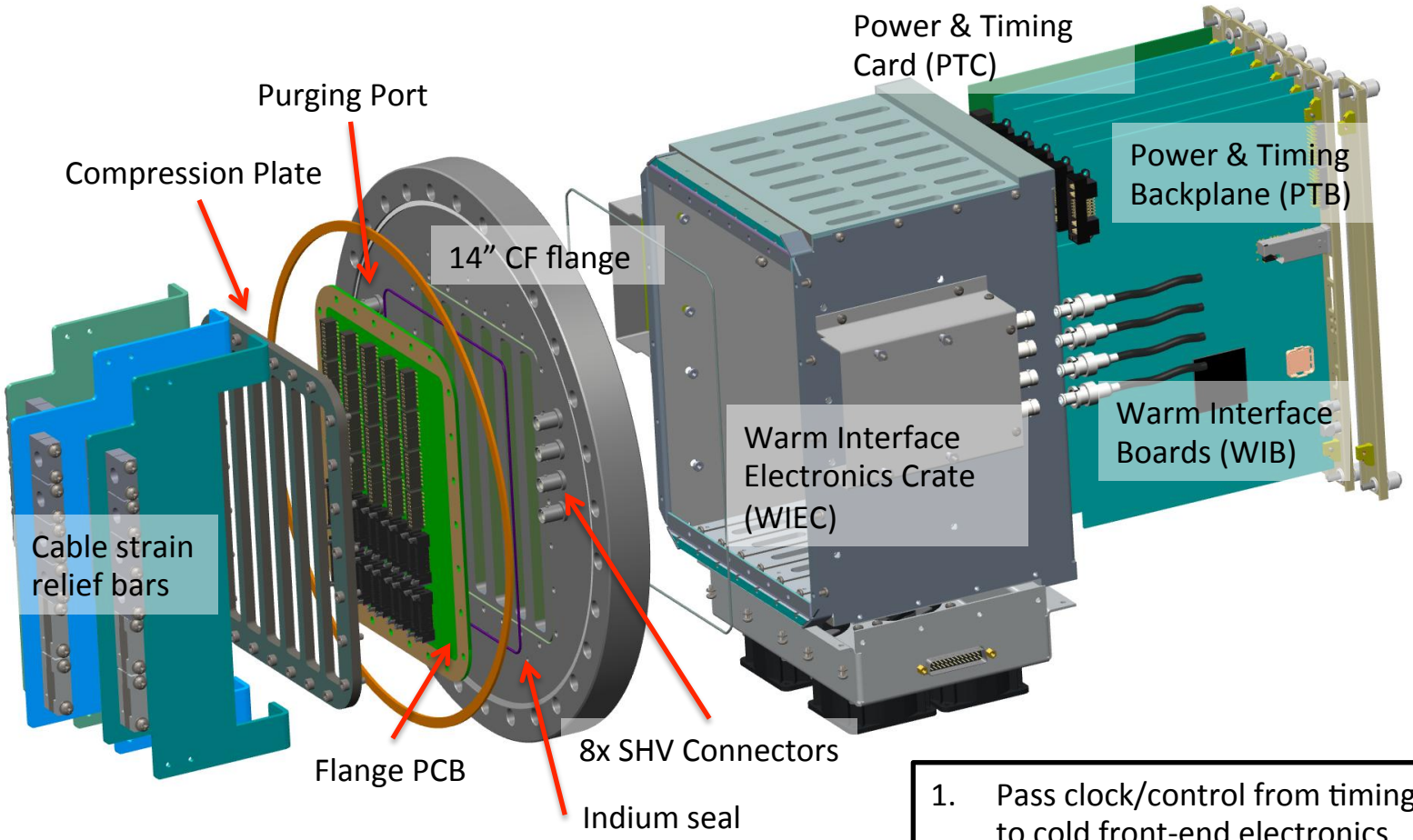
Looking down through inner tube at Clamping Plate:

PD cable bundles



HV cable bundle

CE Warm Components

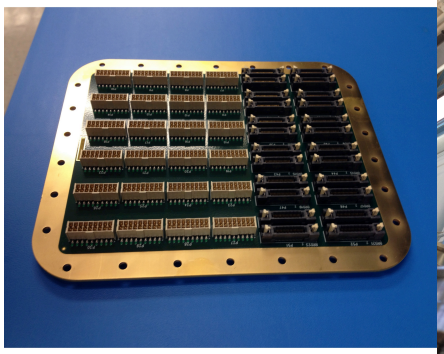


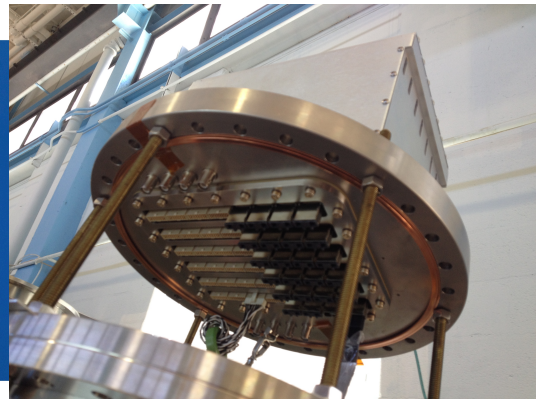
1. Pass clock/control from timing system to cold front-end electronics
2. Deliver high-speed TPC wire data from cryostat to DAQ

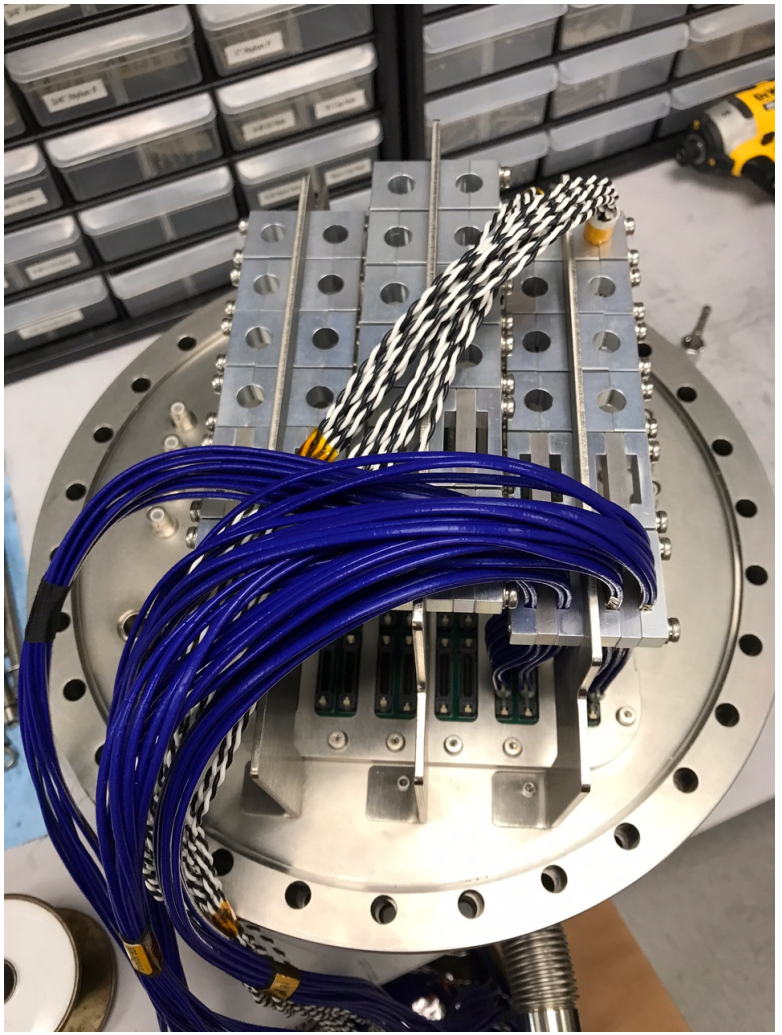
3. Connection to detector ground at CE flange
4. Pass wire-bias and FC HV to cryostat

CE Warm Flange

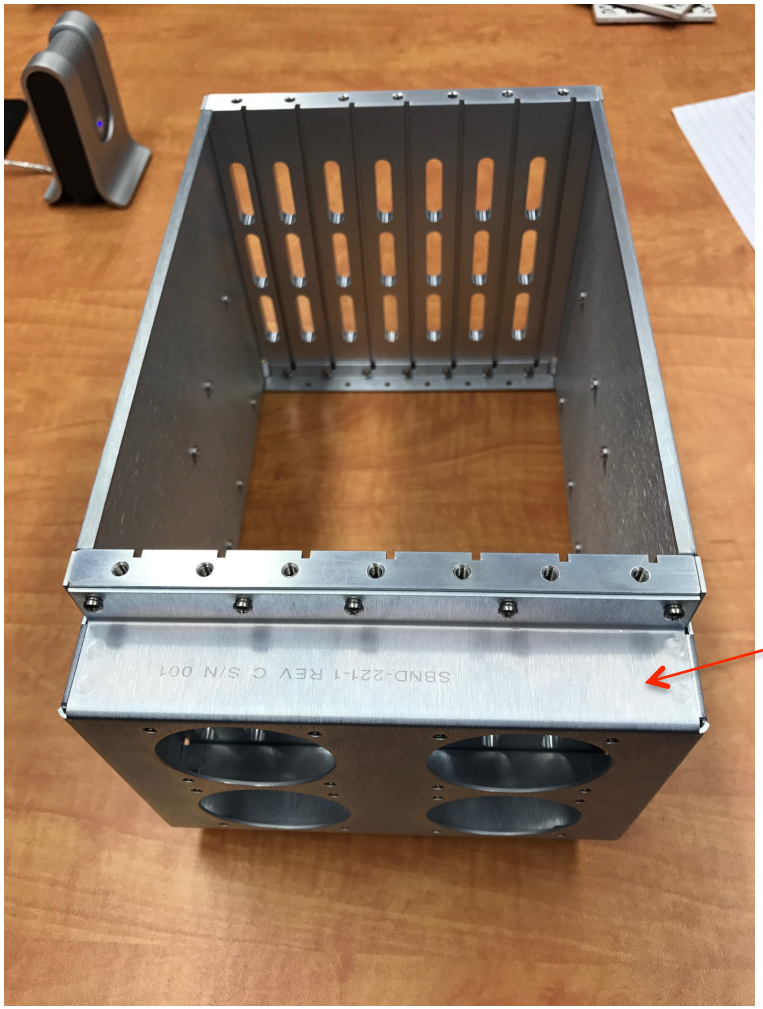
- Mechanical and assembly drawings in DUNE DocDB 2771
- Current status
  - 2 final prototypes have been received at BNL
  - Strain relief support hardware on the flange has been received
  - Will be assembled with flange PCB and have differential pressure tests done
- Flange PCB schematics posted to DUNE Doc 2777
  - PCB fabrication done
  - 3 have been assembled





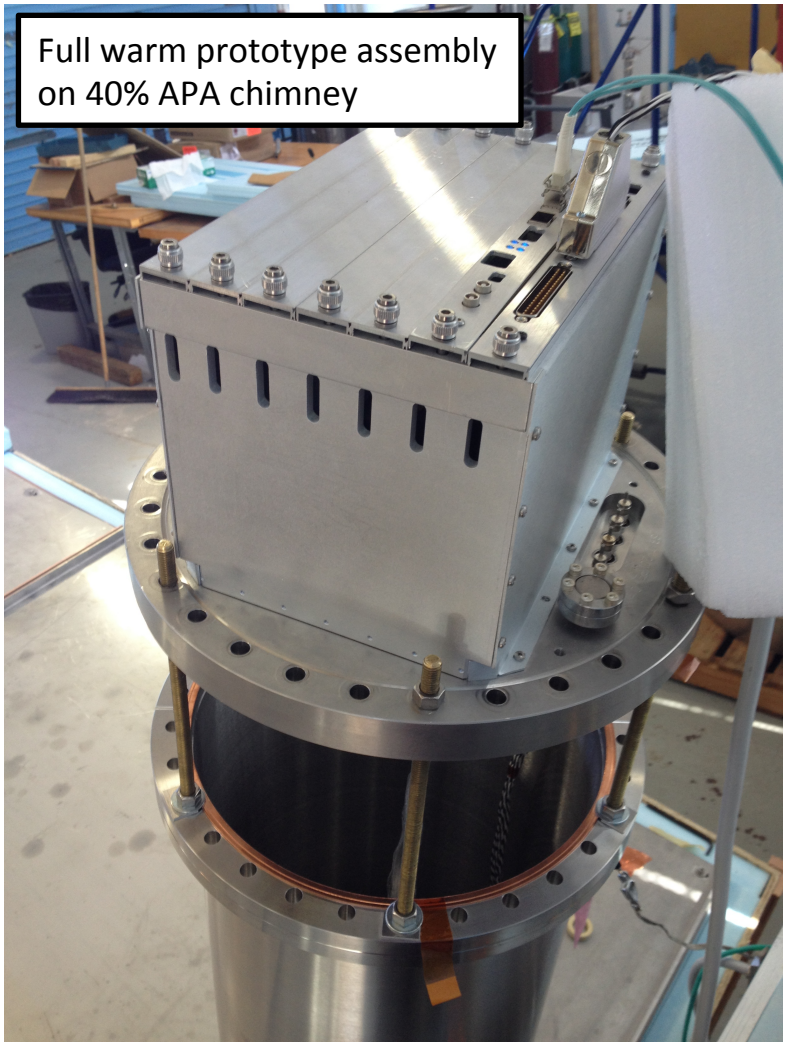


WIEC



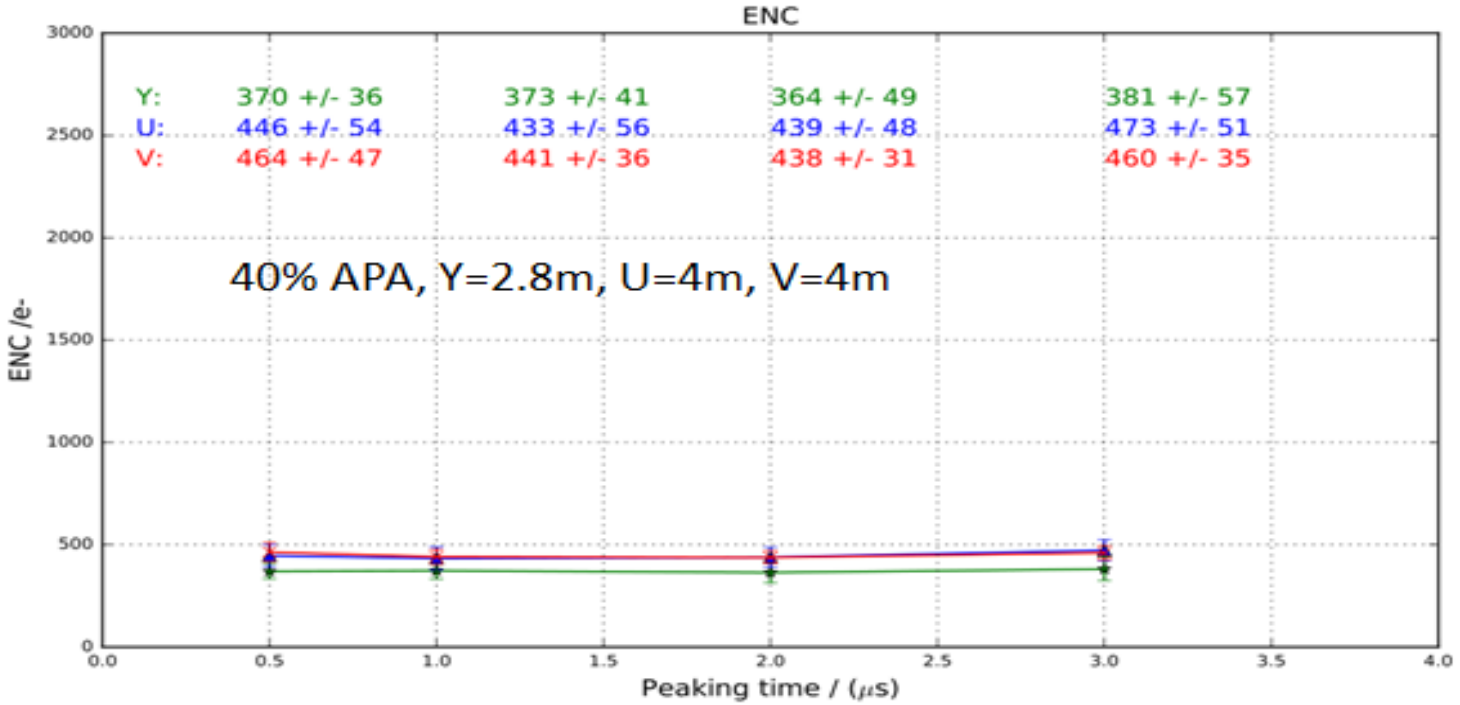
- Mechanical and assembly drawings in DUNE DocDB 2774
- Current status
  - 1 prototype machined by Zober Industries and assembled and tested at BNL
  - System tests ongoing with full CE flange assembly and FEMB on the PSL 40% APA
  - 2 final prototypes delivered
- Each WIEC is cooled by 4 brushless fans supplied by a variable power supply up to 24V
  - Aavid PEAD26025BH (data sheet)
  - Fans ordered
- Thermal measurements were made on a WIB reading out 4 FEMB (fully loaded)
  - Fan and temperature test results in DUNE DocDB 1809

40% APA Teststand



- 40% APA in cold box at BNL
- Full prototype CE system readout
  - WIB/PTC/PTB in WIEC
  - Wiener LV power supply delivering 12V to PTC
  - WIB readout via optical fiber to DAQ PC
    - Internal clock on WIB
  - Prototype CE flange
    - Purge port and SHV connectors on warm side
    - Flange PCB and squash plate on cold side
  - Cold LV and data cable bundles to FEMB on APA wires
    - Maximum 4m wire length
- Grounding scheme for low noise performance has been developed
  - LN2 cycle testing since late April
  - Improvement ongoing…

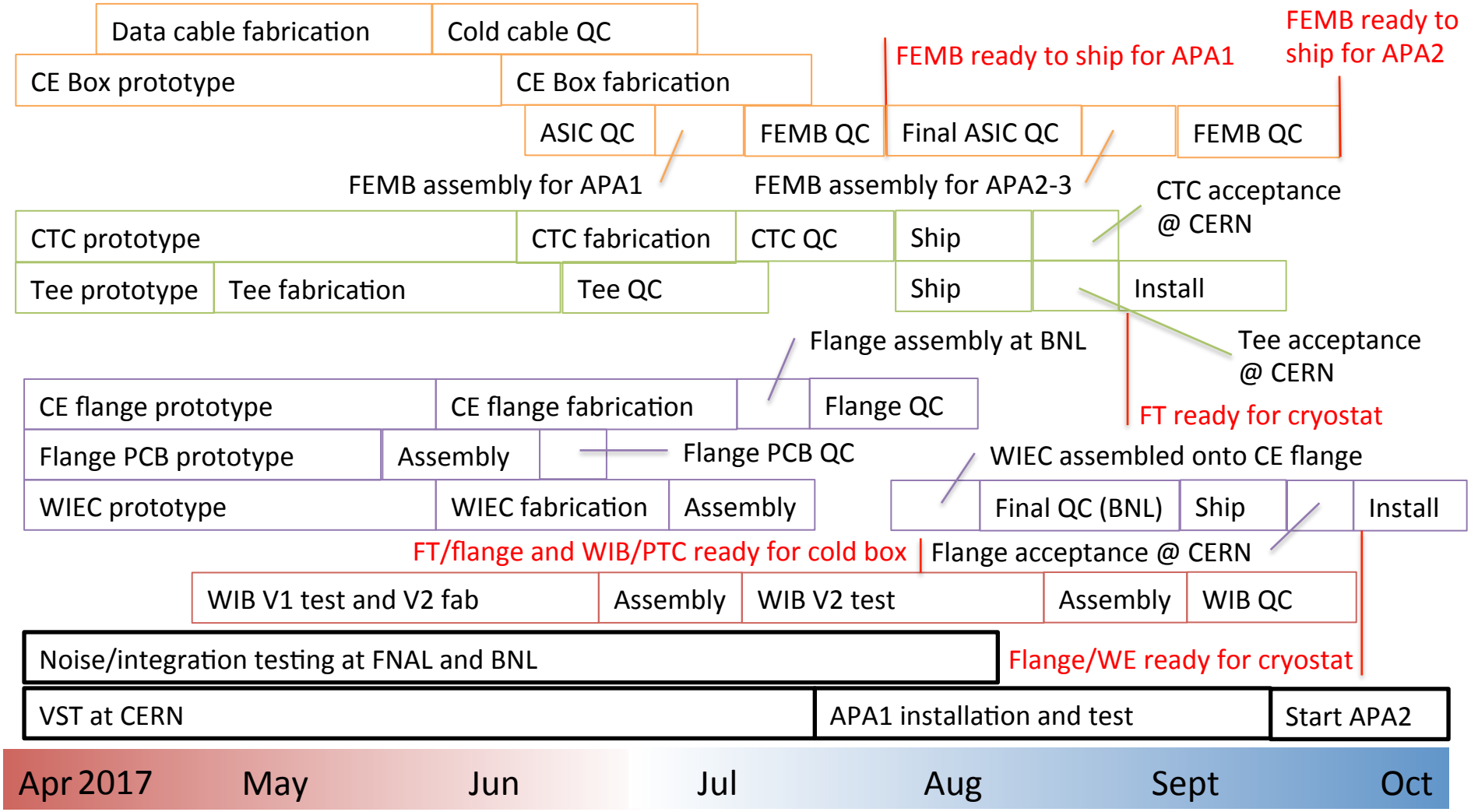
40% APA in LN2: Preliminary Test Results



- Integration test at BNL is ongoing, more tests will be carried out in coming weeks
- ENC at LN2 Temperature
  - Collection plane is ~370 e^- and induction plane ~440 e^- at 1us peaking time

CE installation (as of March 2017 RLS)
- APA1: 6/28
- APA2: 9/8
- APA3: 10/26

CE Schedule



Prototype Milestones

✔ = complete since last update

Prototype Development		Design	Fabrication	Test
Cold Electronics	FE ASIC	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ongoing
	ADC ASIC	P1 ✔	P1 ✔	P1 ongoing
	FEMB AM	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ongoing
	FEMB FM	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ongoing
Cold Cable	Data	✔	✔	ongoing
	Power	✔	✔	ongoing
Signal Feed-through	Flange	✔	✔	ongoing
	Flange PCB	✔	✔	ongoing
	WIEC	✔	✔	ongoing
Warm Electronics	WIB	P1 ✔ P2 ✔	P1 ✔ P2 ongoing	P1 ongoing P2 July
	PTB	✔	✔	ongoing
	PTC	P1 ✔ P1 ✔	P1 ✔ P1 ongoing	P1 ✔ P1 June