Progress toward Cold Electronics for Pixelated Readout of the DUNE Near LArTPC

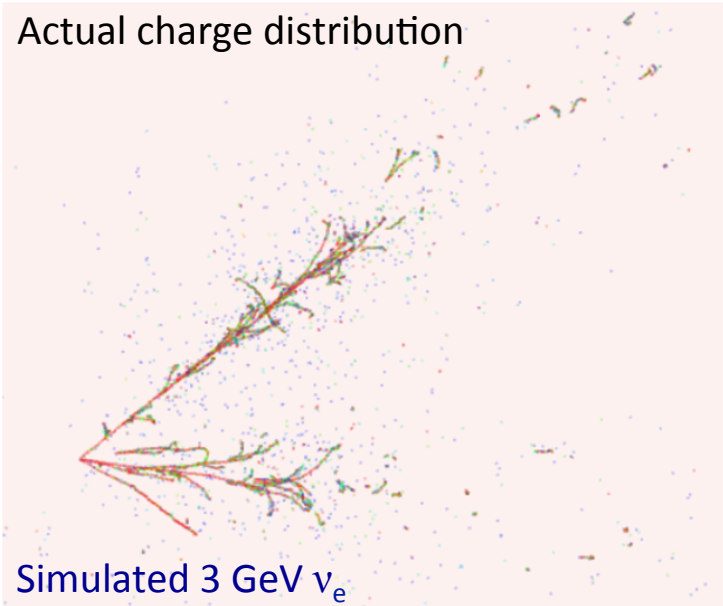
Dan Dwyer (LBNL)

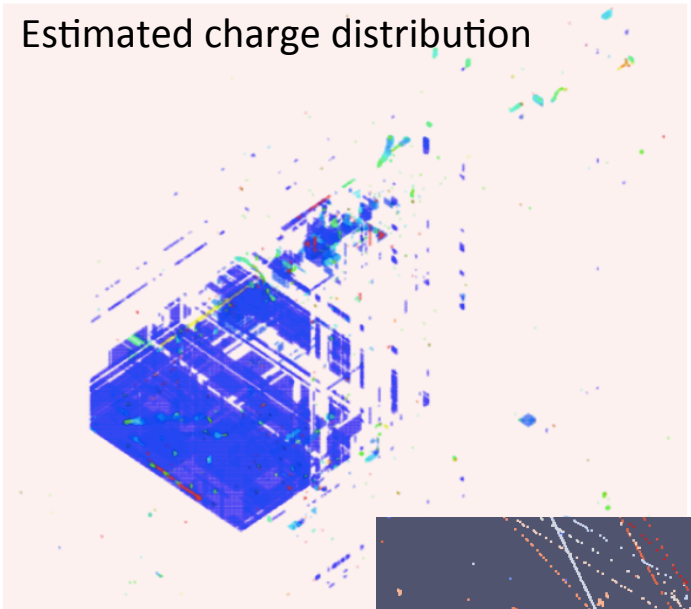
DUNE Near Detector Workshop / CERN

Nov. 6, 2017

3D LAr-TPC: Motivation

Ambiguities in projective wire readout:





When tracks/showers parallel to wire plane, signals arrive simultaneously.

→ Unable to resolve actual charge distribution.

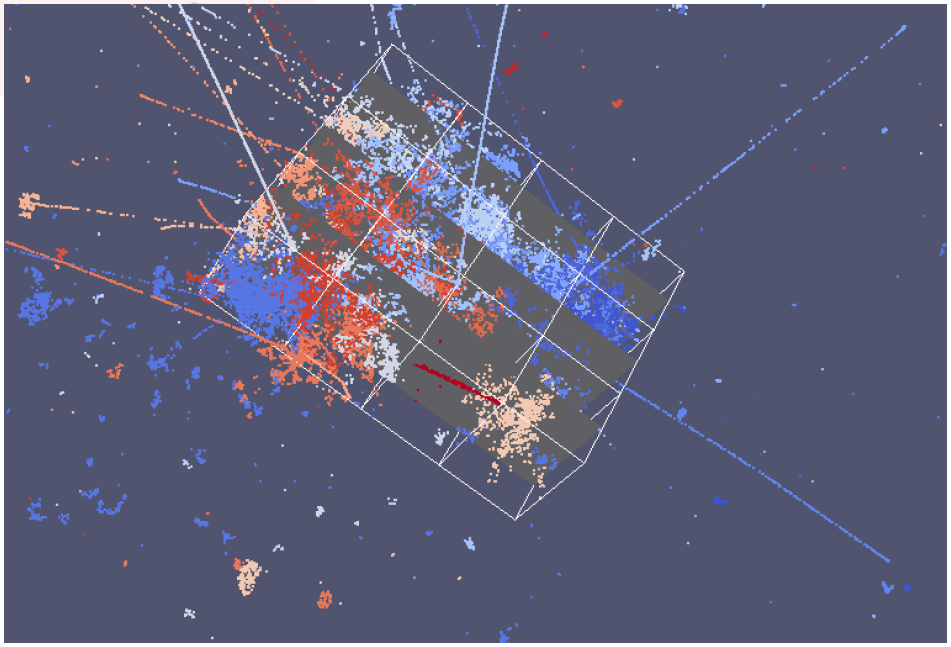
DUNE Near LAr-TPC:

High rate of neutrino interactions at near site exacerbates ambiguities and event reconstruction

→ *Develop true 3D readout.*

Building on experience from ArgonCUBE pixel demonstrator

ArgonCube



Example neutrino signals from one LBNF spill

LArPix Overview

Developing front-end ASIC for scalable LAr-TPC pixel readout

- True 3D readout: front-end channel for each 'pixel' (i.e. pad-based readout)
- Scalable: power use must be very low to avoid excess heat generation in LAr

Recent Progress:

- LArPix v1 ASIC: Chips diced and ready at LBNL
- Test PCBs: Produced and delivered to LBNL
- Control system: firmware and software written, completed basic testing.

Testing program has begun:

Electronics testing:

Initial tests on bench at room temp, in cold box, and at LN_2 temperature

In-situ testing:

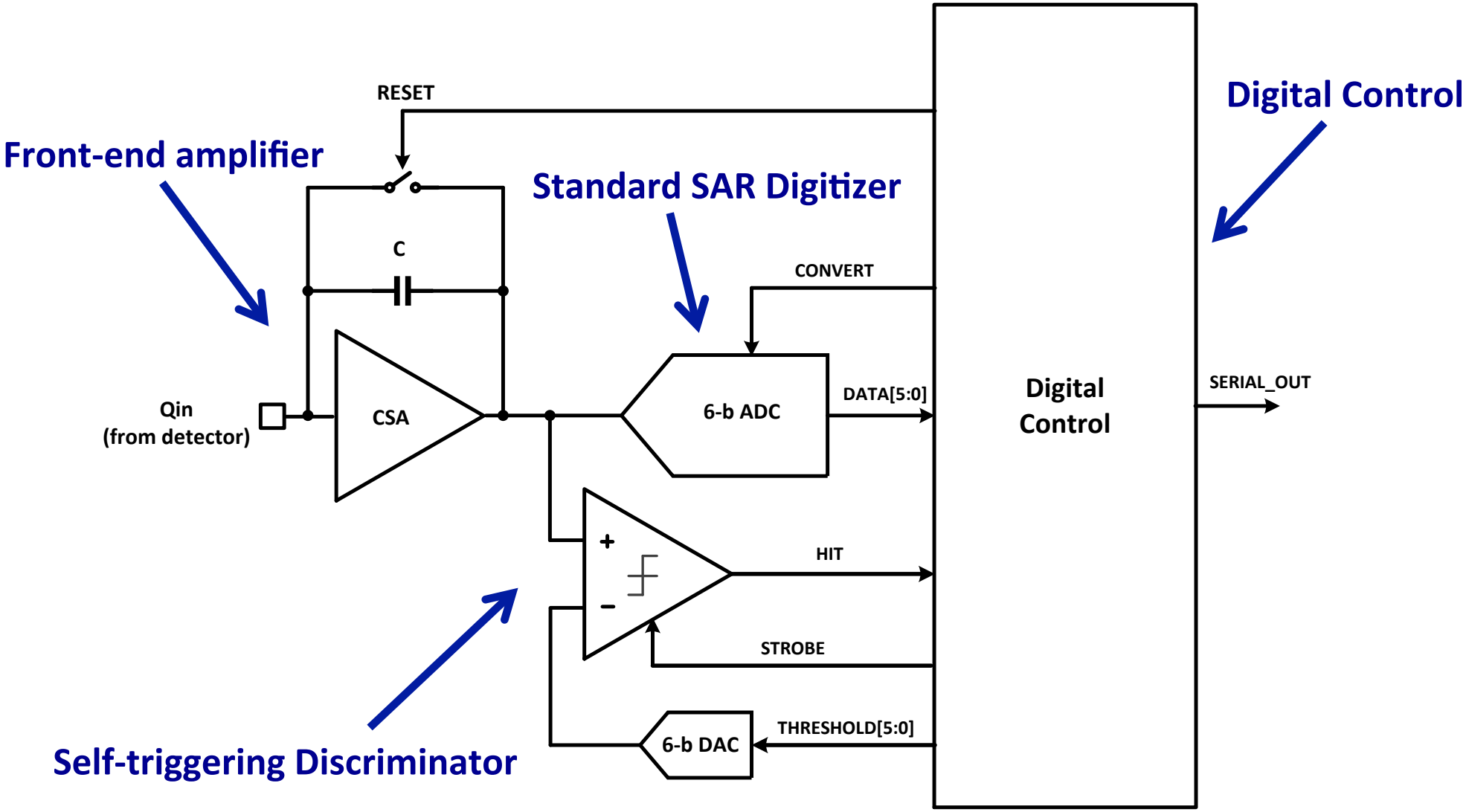
Actual particle detection in small pixel demonstrator TPC provided by Bern

Team:

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stezelberger, M. Kramer, S. Kohn, P. Madigan

LArPix v1: Design Concept

Amplifier with Self-triggered Digitization and Readout



Achieve low power: avoid digitization and readout of mostly quiescent data.

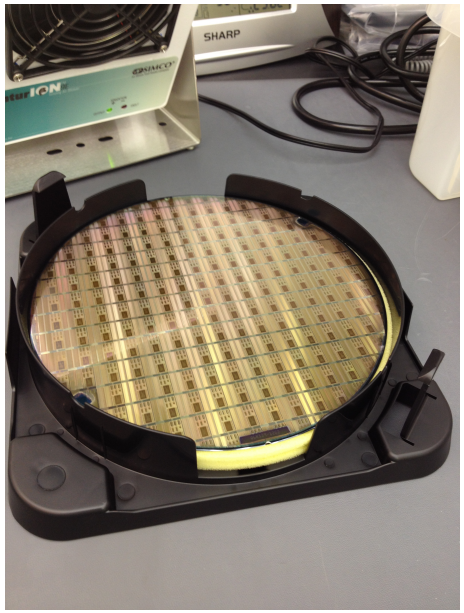
LArPix v1: Design Details

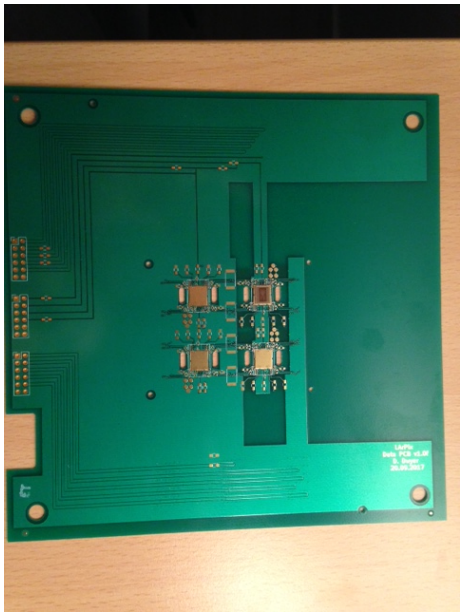
Specification	Value	Units	Note
Number of Analog Inputs (channels)	32 (single-ended)		160 µm effective pitch
Noise	300 @ 88K 500 @ 300K	ENC, e-	Stipulated charge deposition is 15 ke- per MIP for a track in LAr
Channel gain	4 or 45	µV/e-	Digitally programmable
Time resolution	2	µs	with 10 MHz master clock rate
Analog Dynamic Range	~1300	mV	max signal ~ 250 ke-, minimum detectable signal ~ 600 e-
ADC resolution	6	bits	programmable LSB, 4 mV nominal (1 ke-)
Threshold Range	0 – 1.8	V	
Threshold Resolution	< 1	mV	nominal
Channel Linearity	1	%	
Operating Temperature Range	88 - 300	°K	
Event Memory Depth	2048	memory locations	~8 ms without data loss in case of track normal to pixel plane
Output Signaling Level	3.3	V	
Digital data rate	10	Mb/s	with 20 MHz master clock
Event readout time	5	µs	

LArPix Prototype Progress

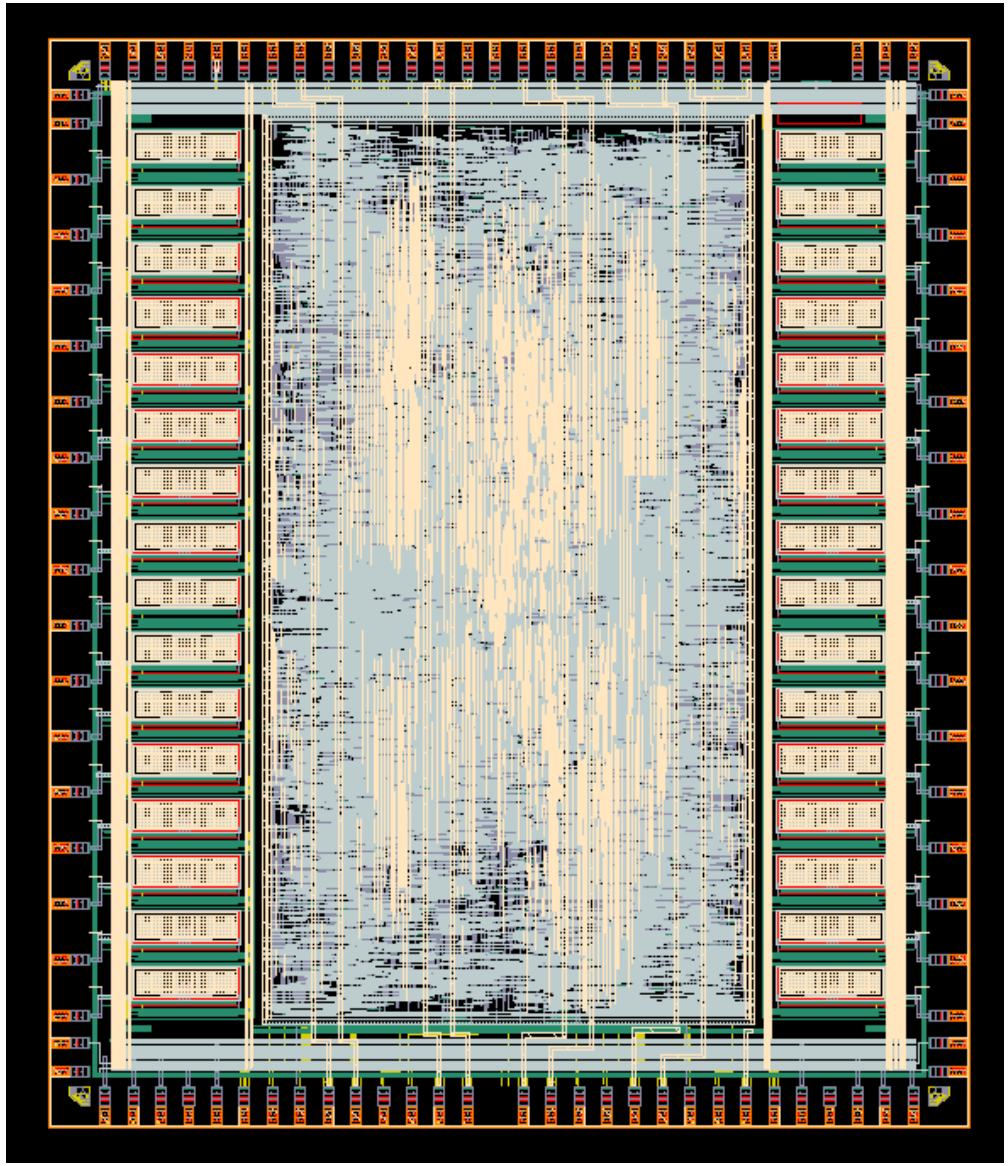
LArPix v1 ASIC:

- Dec. 2016: Design began
- May 2017: Design completed
- June 2017: Submitted for fabrication
- Sep. 2017: Test board designed
- Oct. 2017:
  Wafer delivered to LBNL, then diced
  Testing board manufactured



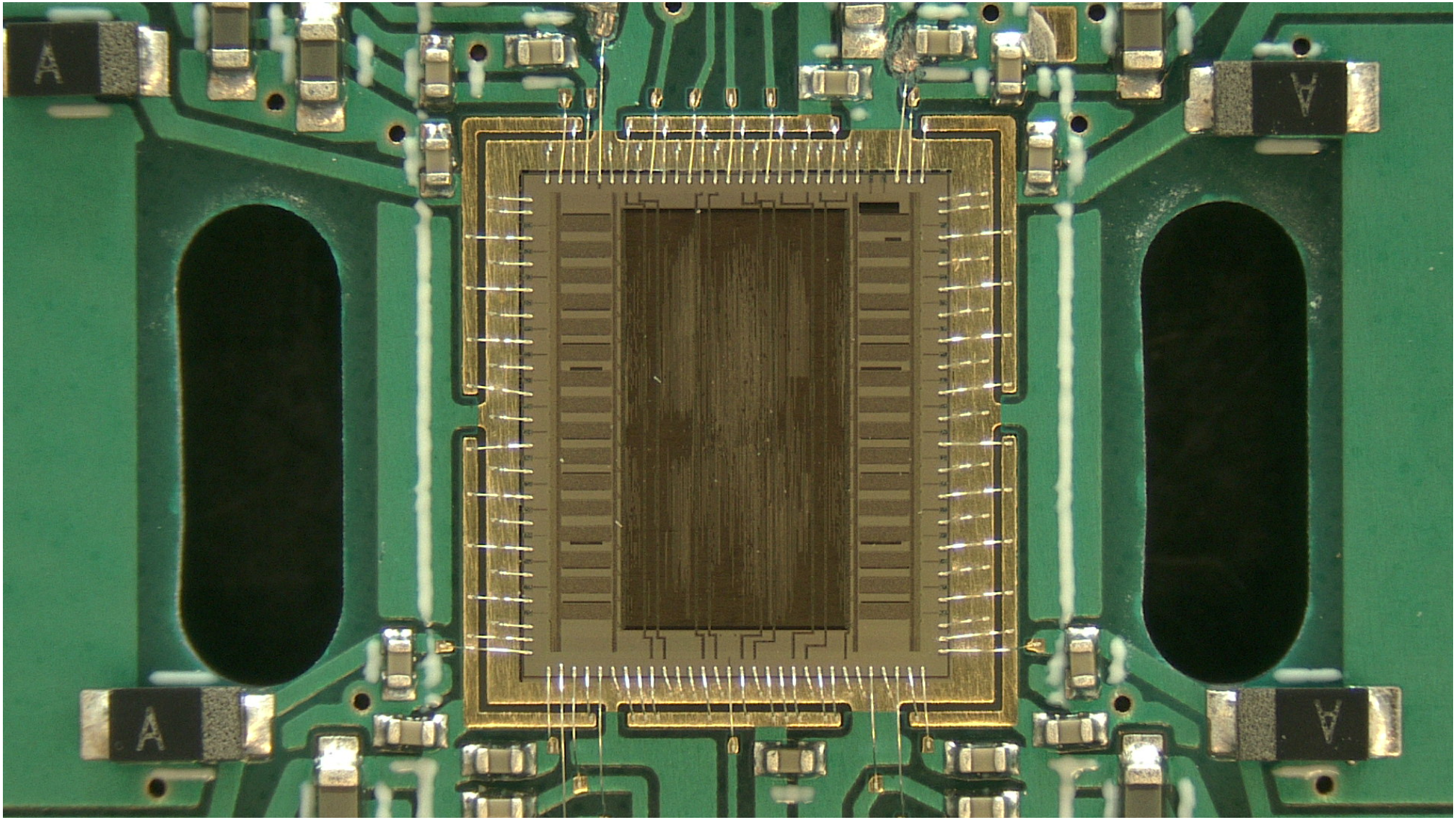


- Nov 2017: Testing has begun



Process: TSMC 180nm

LArPix IC on Test Board



First batch of ICs wire bonded onto test boards

Initial LArPix-v1 Test Results

Very quick progress in bringing chips up:

Nov. 2:

- ✓ Completed bonding of first chips to testing boards
- ✓ Verified power delivery to chips
- ✓ Established communication between chips and control computer
- ✓ Confirmed daisy-chain communication functions as designed
- ✓ Read out and verified all internal chip configuration registers
- ✓ Confirmed ability to write to internal configuration registers

Nov. 3:

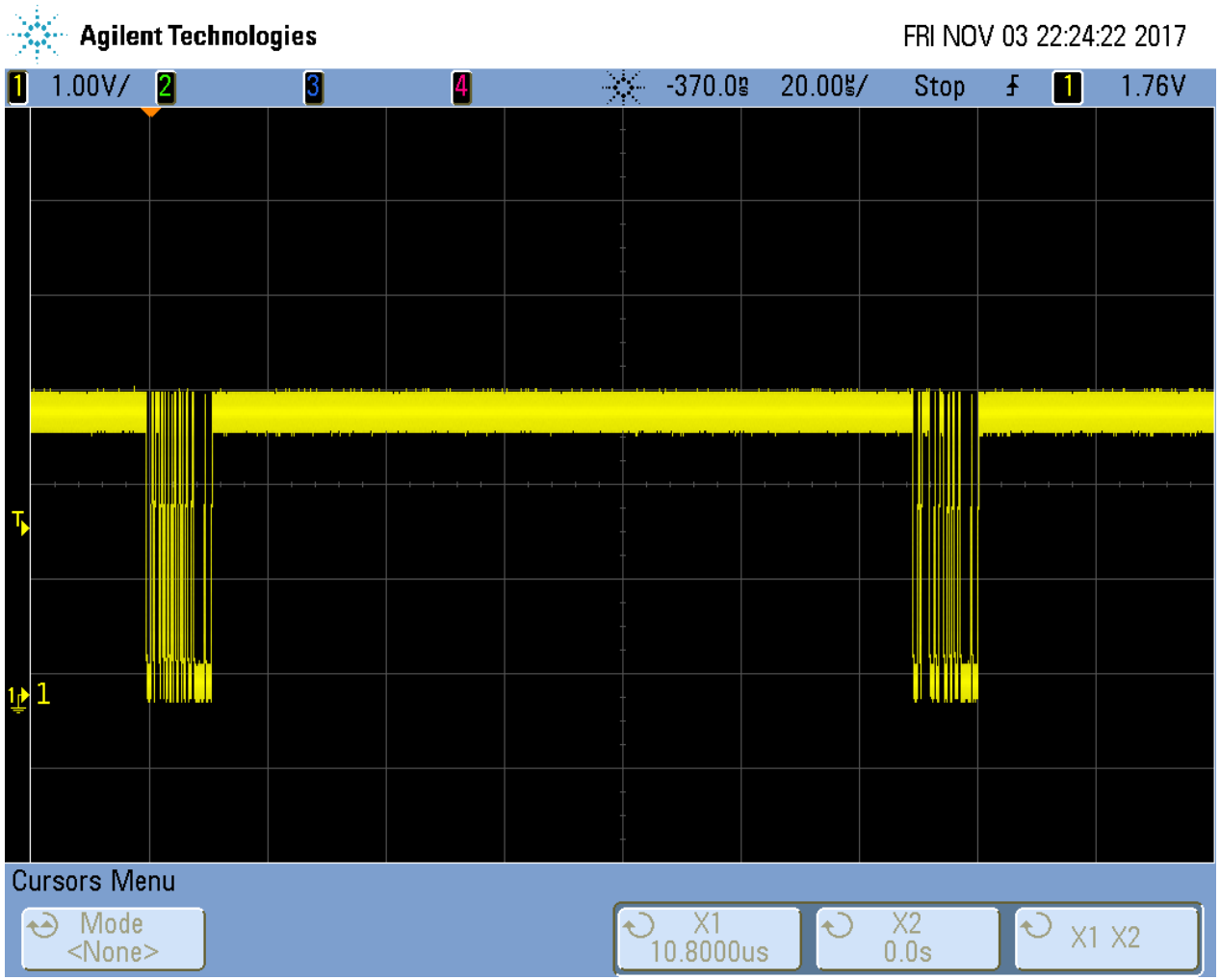
- ✓ Verified external reset of chip, restores default configuration
- ✓ Read out initial hit data (low-threshold noise)
- ✓ Measured channel hit rates versus internal channel threshold
- ✓ Exercised external triggering. Estimated initial noise level from ADC rms.
- ? Tested input of external reference voltage into ADC.

Found some quirks, but all-in-all ICs are working remarkably well.
Hope to report detailed performance measurements soon.

LArPix-v1: First Hit Data

Example: First self-triggered hit data

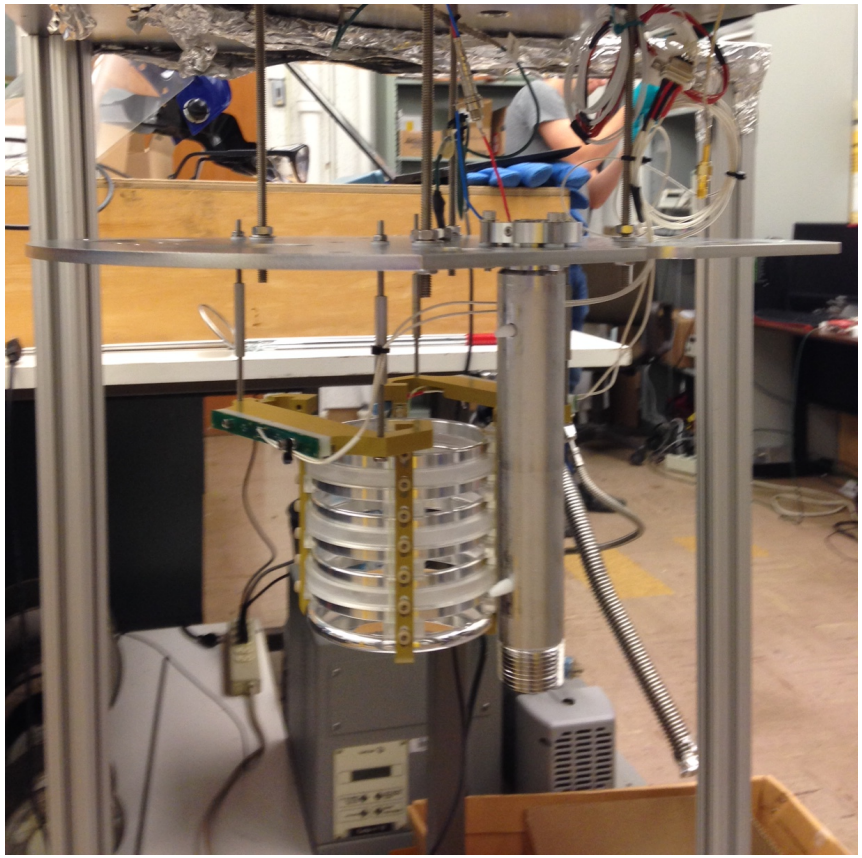
- Adjusted threshold just above noise floor, and captured data from hits on a single channel
- Each data packet 10 µs long. Two hits separated by 130 µs in this scope trace.
- Each data packet contains chip ID, channel ID, timestamp, and ADC value.

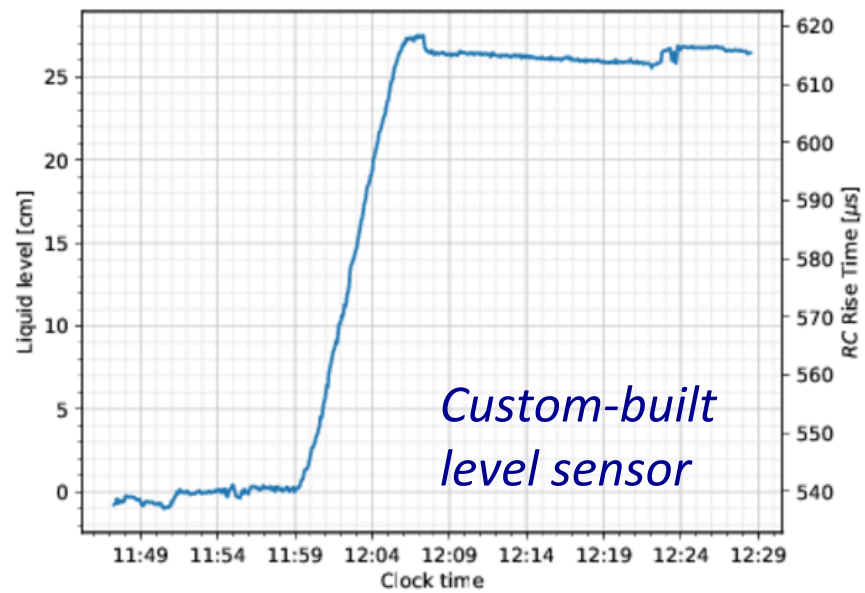


Preparation for TPC Testing

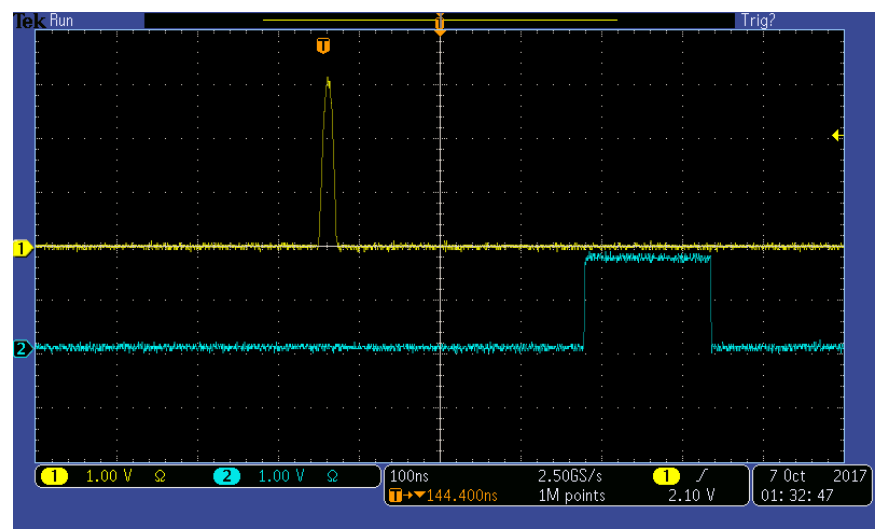
Initial test preparations using LUX/LZ high-purity LAr system:

- Single-pass LAr purification and cryostat
- Tested cool-down process, SiPM operation, LAr level monitoring
- Determined appropriate SiPM bias in LAr (-49 V)
- Refining system to reduce susceptibility to noise from lab environment.





UV LED pulse (yellow), SiPM coincidence trigger (blue)



Future Testing

Next Steps, assuming tests of LArPix v1 continue to go well:

1) LArPix Demonstrator Sensor

- Produce fully-instrumented (1024-channel) LArPix Demonstrator sensor
- Test one copy in Small Pixel Demonstrator at LBNL
- Test one copy in Full-sized Pixel Demonstrator at Bern

2) LArIAT

- Design, produce sensor board for LArIAT PixLAr tests
- Install in LArIAT TPC
- Characterize performance with well-known particle beam.

3) ArgonCube 2x2

- Design, produce sensor plane for ArgonCube 2x2 module

Summary

LAr-TPC Near Detector Module:

Hindered by signal pile-up from LBNF beam intensity.
ArgonCUBE prototype: demonstrated feasibility of 3D charge readout
Large-scale deployment requires low-power readout electronics

LArPix v1 IC:

Dedicated IC for low-power 3D charge readout.
Chip production completed, and ICs delivered to LBNL.
Initial test results are positive. Proceeding to measure performance.

Working closely with Univ. of Bern / ArgonCUBE / LArIAT.

→ *Glad to work with any others interested in 3D readout.*