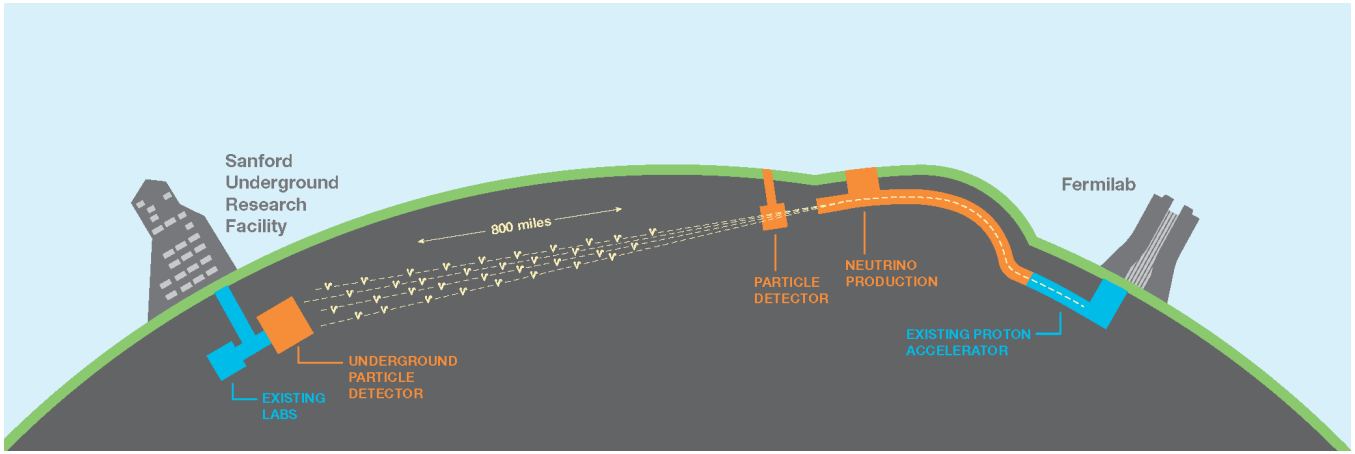

DUNE Cold Electronics Strategy

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Outline

- CE task force
- New Plan for ASIC development
- CE Consortium
- Milestones

CE Task Force

- Members from BNL, FNAL, SLAC, & LBNL
- Focused on ASICs (requirements and status)
  - Failed to concisely restate requirements (gained appreciation for complexity of this task).
  - Verified existing requirements/specifications for FE and ADC.
    - Low noise is essential (ALARA).
    - 12-bit linear ADC is desirable.
      - Linear because induction planes (bipolar) and collection plane (mostly unipolar) require different baselines.
      - 12-bit so ADC contributes very little to noise while ensuring that signals from tracks near the primary vertex don't saturate ADC "too frequently." (Allows for 4-5 protons at primary.)
- Full "answers to charge questions" are included with this talk on the Indico page.

Task Force Conclusions

- FE must be cold (to minimize noise) & current ASIC is likely to satisfy DUNE requirements after minor changes.
- For best performance, ADC conversion and multiplexing should also be done in the liquid argon. Because of the risk of accelerated aging, commercial circuits should be used only as a last resort.
- The current "domino" ADC is unlikely to meet DUNE requirements.
- The 65-nm communications/data concentrator ASIC (COLDATA) has not yet been tested (1st prototype was submitted in May & will be tested this summer), but is likely to work.
- We recommend that a new ADC ASIC be developed using a more conventional architecture.
- The SLAC group recommends to minimize risk by developing in parallel a fully integrated ASIC (FE+ADC+communications/control).

Executive Committee Response

- The EC agreed that the existing cold ADC ASIC design would no longer be pursued and that a new cold ADC solution would be developed;
- The EC agreed that the development of the new ADC should be a collaborative effort between more than one institution, to avoid a possible single point of failure;
- The EC agreed that, if resources were available, an alternative solution should be investigated. This could be a single-chip solution or an alternative to the new baseline cold ADC (once chosen). The Technical Coordinator would investigate possibilities and report back to the EC by the time of the August collaboration meeting.

New Plan for ASIC Development

- BNL will continue FE ASIC development.
- FNAL will continue COLDATA development.
- A new ADC will be developed.
  - Carl Grace (LBL) will lead a comparative study of architecture (now-Sept).
  - A design collaboration will be formed (Sept)
  - New ADC prototype submission expected Spring/Summer 2018.

ADC Architecture - ΔΣ

Delta-Sigma (AKA Sigma-Delta)

- Uses oversampling to reduce error by (weighted) averaging.
- Relaxed analog requirements, but complex digital logic:
  - ΔΣ modulator = differential amplifier + integrator(s)+1-bit ADC produces high frequency digital output; fraction of 1s is proportional to input amplitude.
  - Followed by a low-pass digital filter (sinc=sin(x)/x or $sinc^3$) and digital decimation (weighted average) to produce high resolution output at desired sampling rate.
- PRO: No calibration required (all signals pass through the same analog circuitry).
- CON: Sampling rate of 128-256 MHz required for 12-bit 2-MSPS
  - Only 1-2 channels/ADC; power consumption may be problematic.

ADC Architecture - SAR

Successive Approximation Register (SAR)

- Uses a sample-and-hold, a DAC, a single comparator, and a binary search to find setting of DAC such that DAC output = ADC input.
- Number of cycles required for conversion = number of bits in output+1.
- DAC precision depends on capacitor matching
  - But can't use simple DAC with binary-weighted capacitors for a 12-bit ADC
    - Smallest capacitor size is determined by how well capacitors match.
    - Dynamic range of 4096 would make largest capacitor too large.
  - More complex DAC geometry requires complex built-in calibration (every code uses a different combination of capacitors).
- PRO: Low power, tolerant of constant comparator offset.
- CON: Sampling rate of 2 MHz x (12 + 1) = 26 MHz limits multiplexing, complex calibration required.

ADC Architecture - Pipelined

Pipelined ADC

- Uses a series of pipelined FADC stages.
  - Most likely to be implemented using a series of “1.5-bit” FADCs
  - at each stage with output=1, a fixed voltage is subtracted from the input.
  - Built-in calibration is required, but is fairly simple.
- Operates at the output sample rate; pipeline delay increases with the number of bits.
- PRO: Pipelined architecture makes multiplexing input channels natural, 2-MSPS ADC operates at 2 MHz, tolerant of comparator offset (redundant codes w/3 comparators/stage).
- CON: Higher power than SAR (Op amps used in each stage), calibration required.

Cold Electronics Consortium

- Significant interest from US members of DUNE, many of whom are not working on ProtoDUNE CE.
- Continued interest from US members working on ProtoDUNE CE.
- Eric James expects “structure” to be in place by the end of July.

Response to LBNC Recommendations

"Given the development timeline and longevity requirements for DUNE cold electronics, planning should commence for a large scale cold electronics test facility that can permit large-scale testing, evaluation and burn-in." (Due Date: 26-Oct-17)

The deliverables of the CE Consortium include "System Engineering." This will include validation of components and a variety of test facilities. A number of groups have already expressed interest in this activity. The planning for these facilities is expected to begin in earnest early this fall.

Milestones – Calendar Years

Q2/2017: CE task force report✅ (DUNE-doc-2374 “Response…”)
Q3/2017: Formation of CE consortium
Q3/2017: ADC design study
Q4/2017-Q2/2018: ADC design
Q2-Q3/2018: ADC submission