Identifying Opportunities for R&D and Collaboration

Roundtable Discussion

ANL

Marcel Demarteau, Robert Wagner

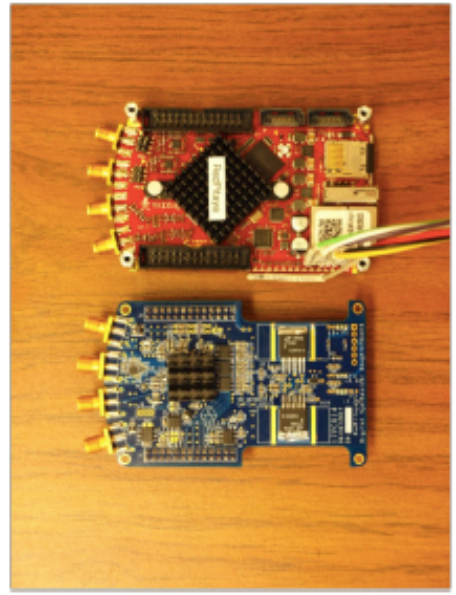
ANL Recently completed and ongoing projects

1. ATLAS experiment at CERN → ongoing and completed
   - FTK to Level-2 Interface Card (ATCA hardware and firmware)
   - FELIX (firmware)
   - Hardware Track trigger interface (firmware and software)
   - FELIX for the HL-LHC upgrade of ATLAS (hardware and firmware)
   - Concluded work on Tile Cal upgrade (LVPS, HV_OPTO, QIE FEB, QIE MB, project engineering)
2. LBNE (proto DUNE) → ongoing
   - Front-end electronics for Photon detectors (boards + firmware)
3. CTA → all completed
   - L2 trigger (boards + firmware)
4. g-2 → all completed
   - Trolley motor control
   - Field measurement electronics
5. Generic R&D → development of wireless techniques in data and power transmission application for particle-physics detectors
6. Electronics for quantum computers at the University of Chicago → ongoing
   - Digital synthesizer daughter board
7. GRETINA TDAQ System. → Development is ongoing

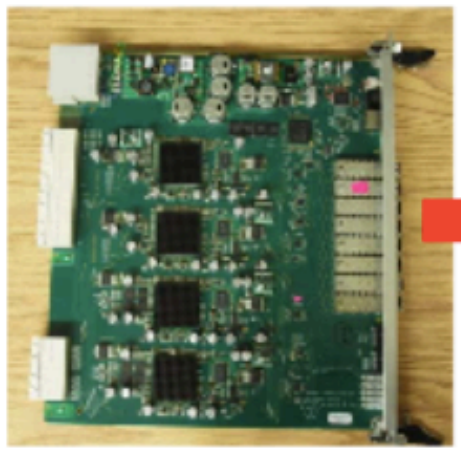
Some Current projects

ATLAS TileCAL @ CERN
– Low Voltage Power Supplies for Phase 2 Upgrade

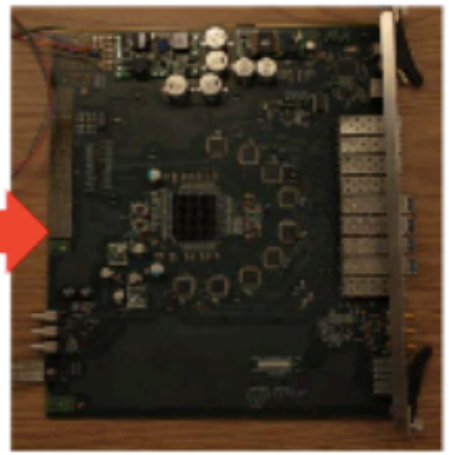
LBNE (DUNE) @ FNAL (35-ton prototype)
– Front End Electronics for Photon Detectors
Now: 35-ton prototype; Next: CERN TB



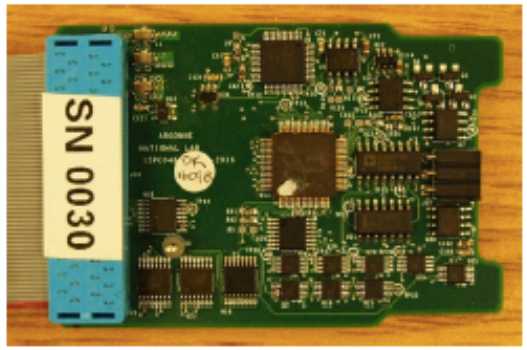
Synthesizer for a quantum computer



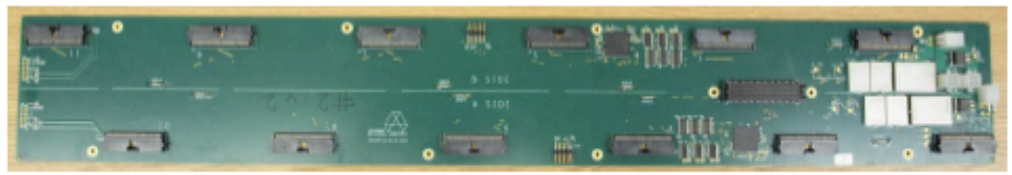
ATLAS TDAQ @ CERN
– FTK Readout Driver



CTA
– L2 Array Trigger



QIE front-end electronics for ATLAS Tile Calorimeter



BNL

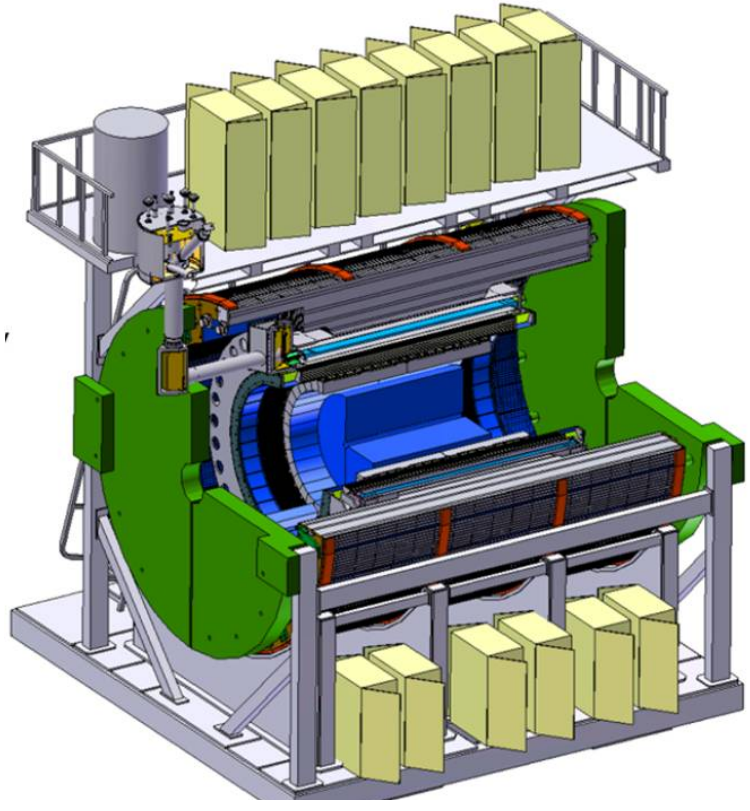
Michael Begel, Kai Chen, Paul O’Connor, Martin Purschke

DAQ Activities Overview

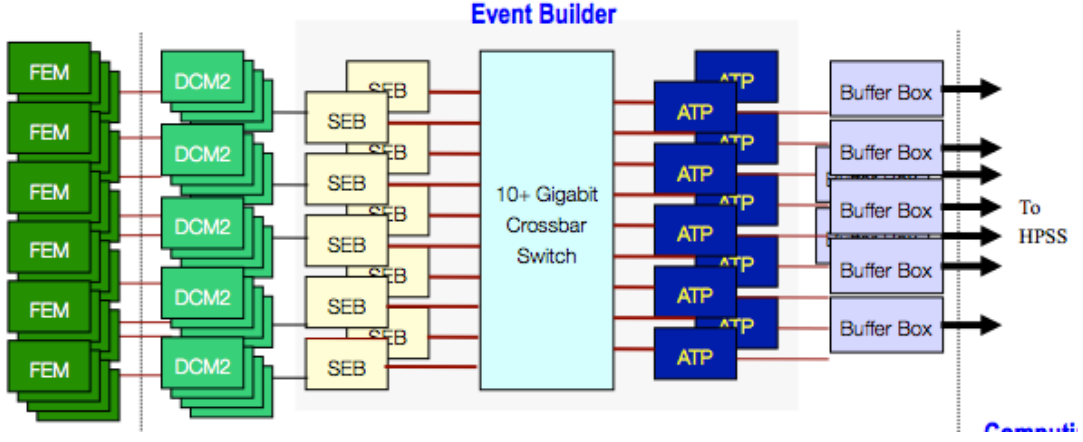
- sPHENIX
  - Time Projection Chamber Electronics
    - Front End Electronics (FEE)
      - 154k readout channels. 600 FEE cards, each handling 256 channels
      - Total estimated data rate is 940Gbits/s
    - Data Aggregator Module (DAM)
      - Collects data from 600 FEE cards
      - Reduces data via triggering, clustering and compression to reduce data rate to 80Gbits/s
      - Hardware will utilize 24 FELIX PCIe cards, developed for ATLAS by BNL Physics Omega Group

- NSLS II
  - Germanium 384 Element Strip Detector
    - 1st system installed at Powder Diffraction (XPD) beamline at NSLS II, future systems at APS and CHESS planned
    - Custom BNL developed ASIC (MARS), provides peak detection and timing circuitry for spectroscopy and time of arrival.
    - The data is collected photon-by-photon and processed in an embedded computer based on the Xilinx Zynq system-on chip, can readout and process > 20M photon events per second
  - VIPIC (Vertically Integrated Photon Imaging Chip)
    - 1Mpixel camera custom-designed for x-ray photon correlation spectroscopy (XCS), an application in which occupancy per pixel is low but high time resolution is needed
    - Takes advantage of 3D integration technology
    - Collaboration between BNL, FermiLab and Argonne
    - Detector Head output provides 36 fibers running at 5Gbps each. DAQ will utilize FELIX PCIe card, developed by BNL Omega Group for ATLAS

sPHENIX Experiment at the Relativistic Heavy Ion Collider



- Inner tracking system (MAPS, TPC)
- Electromagnetic and Hadronic Calorimeters
- Streaming readout of the TPC
- High data rates (~100Gbit/s sustained) – maybe more
- Proven DAQ architecture



- Predecessor experiment “PHENIX” was the trailblazer for “Petascale” data volumes in the early 2000’s
- 15KHz event rate (remember these are heavy-ion collisions)

Technologies

- Streaming readout of the TPC using the ALICE SAMPA chip
- ATLAS FELIX card adapted for SAMPA readout
- New front-ends for calorimeter electronics
- R&D-themed DAQ system “RCDAQ” has become a real hit worldwide
- sPHENIX uses RDAQ for virtually all R&D data taking needs
- First-rate data format and assorted analysis framework might spill over to the EIC era

ATLAS Phase-I Upgrade (Near term projects)

- ***Front-End LInk eXchange (FELIX) in readout and DAQ***
  - factorize front-end electronics from data handling with **compact, high-density, scalable, low maintenance, easily upgradeable, commodity-based solution**
    - 48 pairs of optical links up to 14 Gb/s, PCIe Gen3 x16 lanes
    - Supports to interface TTC, TTC-PON, White Rabbit timing systems
  - BNL co-leads ATLAS readout architecture development
    - Contribute to **hardware**, **link firmware** and **system integration**
  - FELIX adopted by ATLAS for Phase-I readout
    - LAr, Muon, Level-1 Calorimeter Trigger
  - **paradigm shift adopted by ALICE, ATLAS, LHCb, sPHENIX, and proto-DUNE**
    - ***proto-DUNE***: readout one TPC Anode Plane Array
    - ***sPHENIX***: TPC & MVTX readout
    - evaluating use at ***DUNE***, BNL & ANL Light Sources ***NSLS II***
    - Proposed 2017 LDRD: to use FELIX in ***eRHIC***
- ***Global Feature Extractor (gFEX) in Level 1 Calorimeter Trigger***
  - Conceived, designed, developed, prototyped, and produced at BNL
    - collaboration of BNL, Chicago, Indiana, Lund, Oregon, Pittsburgh, Stockholm
  - trigger hardware using FPGA with many transceivers satisfies the high-bandwidth, fixed-latency, & processing requirements
    - 3 Virtex Ultrascale and 1 ZYNQ Ultrascale+ FPGAs
    - 16GB DDR4 DIMM
    - 30 Layers Stack up
    - 12.8 Gb/s optical links, and onboard electronical 25.6 Gb/s GTY links
    - 312 RX links, 96 TX links
    - 1.12 Gb/s parallel data bus between processor FPGA
  - ***LHCb group at Milan purchased a gFEX board for evaluation***

ATLAS HL-LHC Upgrade

- ***FELIX in the Data Acquisition***
  - Used by all subsystems
  - **based on the Phase-I FELIX card designed, developed at BNL**
    - PCIe Gen4 x16 lanes
    - FPGA: Kintex Ultrascale+ or ZYNQ Ultrascale+
  - BNL will reprise Phase-I role with additional production responsibilities

- ***Features Global Common Module (GCM) in the Global Trigger System***

  - different functions implemented in firmware rather than in hardware

  - **based on Global Feature Extractor Module (gFEX) that was conceived, designed, developed, prototyped & produced at BNL**

  - kernel components: FPGAs
    - 2x Virtex Ultrascale+
    - 1x ZYNQ Ultrascale+
  - firmware for frame and serial-to-time multiplexing & transmission to Global Event Processor

Fermilab

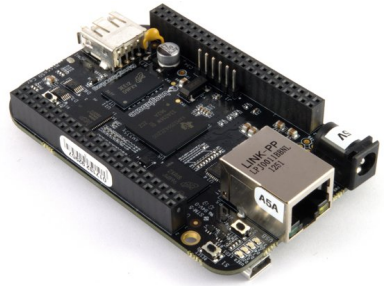
Kurt Biery, Alan Prosser, Ryan Rivera, Lorenzo Uplegger

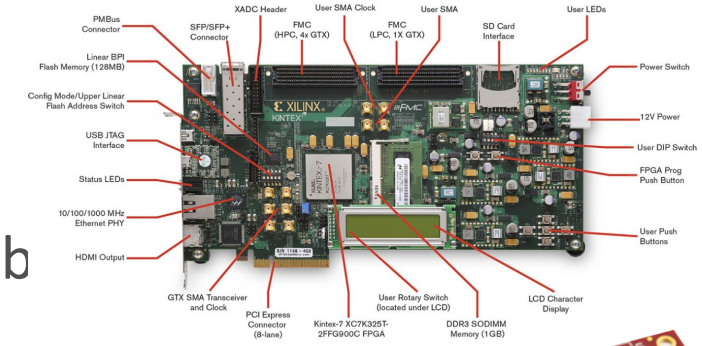
Test Beam and Test Stand DAQ Technologies

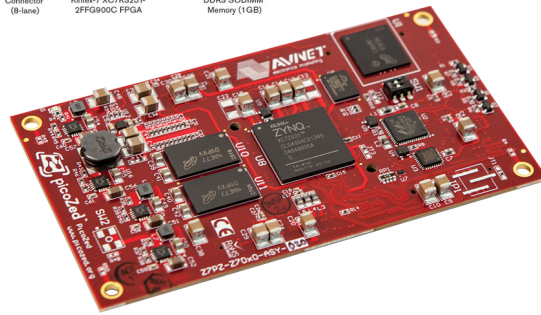
- This is a brief **survey** of DAQ technologies for **test beams** and **test stands** currently available at U.S. institutions.
  - Based on input from SLAC, BNL, and FNAL.
- The goal is to raise awareness of existing solutions and to spark discussion toward future collaborations and new developments.
- SLAC (Contact: Carsten Hast, hast@slac.stanford.edu)
  - No standard test beam facility DAQ. Users generally provide their own DAQ. Available tracking telescope, ADCs, flash ADCs, scalars.
- BNL (Contact: Martin Purschke, purschke@bnl.gov)
  - RCDAQ was developed as a general purpose DAQ – used by experiments, test beams, and test stands. Light weight and configured via Linux script.
- Fermilab (Contact: Mandy Rominsky, rominsky@fnal.gov)
  - Test beam facility DAQ based on *otsdaq/artdaq* (general purpose DAQ with web-based configuration and control) commissioning. Available tracking telescopes, wire chambers, Cerenkov, scalars, PREP equipment, CAPTAN FPGA-based test stand hardware.

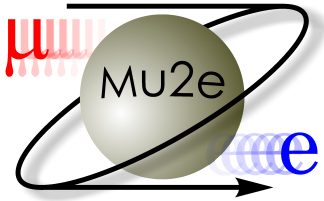
otsdaq and *artdaq* Data Acquisition Toolkits

- *otsdaq* is a Ready-to-Use DAQ solution aimed at test-beam, detector development, and other rapid-deployment scenarios
  - *otsdaq* uses the *artdaq* framework under-the-hood, providing flexibility and scalability to meet evolving DAQ needs
  - Library of supported front-end boards and firmware modules implementing custom protocol
  - Provides Run Control and readout software that works with *otsdaq* firmware
- *artdaq* is a plugin-based DAQ framework, used by several Fermilab experiments such as DUNE and mu2e
  - Flexible design allows for different detector technologies and event selection
  - Allows for data to be analyzed mid-stream for software triggers
  - Configurable asynchronous readout
  - *artdaq* filtering modules are compatible with the *art* analysis suite



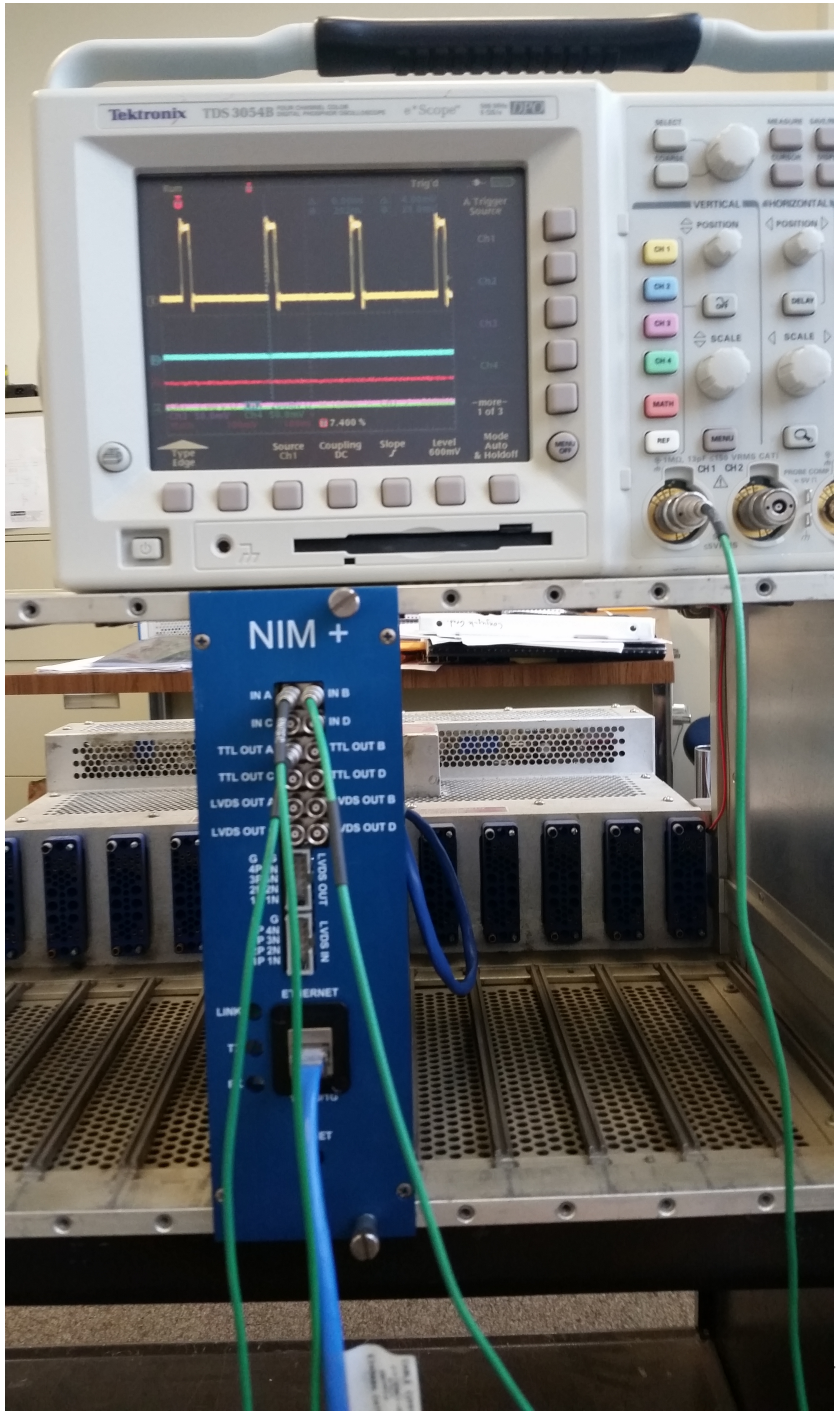






Test Stand Hardware - NIM+

- FPGA-based coincidence module.
  - Custom daughter card (FNAL/PPD) to digitize NIM signals for processing on CAPTAN+ FPGA board (FNAL/SCD).
- Firmware developed for signal processing (delay and stretch).
- Remote setting of parameters via *otsdaq* and data readout event-by-event supported
- Successfully used in 4+ efforts at FTBF in May.
- Goal is 2 modules available from PREP in next month.



LBNL

Carl Grace, John Joseph, Sergio Zimmermann

- High Reliability, Cold Electronics
  - e.g. ICECUBE
    - ATWD, waveform digitizing ASIC
    - Electronics designed to operate from 0C to -60C
  - DUNE – Deep Underground Neutrino Experiment
    - Cold ADC ASIC - 30+ years immersed in Lar
    - LArPIX, pixelated low power readout ASIC
    - ASICs operate from 88K to room temperature
  - SNAP
    - CCD Readout processing ASIC with pipelined ADC
    - DC/DC Converter and Clock Driver ASIC
    - Designed to operate at -140C
- On Detector Processing with custom instructions
  - Designer HPC ASIC based on RISC-V open source Instruction Set
  - Currently in design targeting 28nm
- Digital-on-Top physical design methodology for Hybrid Pixels

- FPGA
  - Real Time Signal processing
  - Embedded networking
    - High speed serial links (electrical & optical)
    - Ethernet, JESD204B
  - Hard & Soft Core CPUs and embedded software
  - VHDL, Verilog, & high level synthesis
  - High speed controls & synchronization
- Network based data streaming to NERSC
- Switched network based event builder and processor farm
- ATCA/uTCA
  - Si Detector DAQ platforms
- System design, integration, and deployment

PNNL

Eric Church, Jim Fast, Lynn Wood

DAQ Development for National Security

Generally use COTS DAQ solutions

- Development effort/cost not feasible in 3-year programs
- Size, weight and power are often design drivers
- FPGA-based real-time analysis often employed
- Scaling COTs solutions to 1-10k channel systems is ineffective – technology gap for this application space

Some recent PNNL development systems

High-Rate HPGe Detector

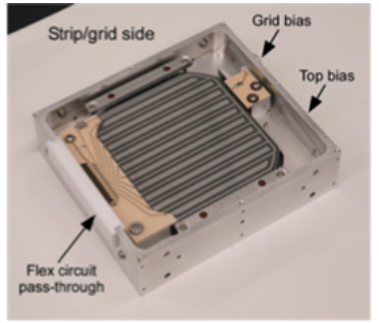
- Assay of spent fuel with gammas with segmented HPGe detector; extreme pileup and deadtime
- Real-time FPGA processing in 250MS/sec streaming data for trigger and energy

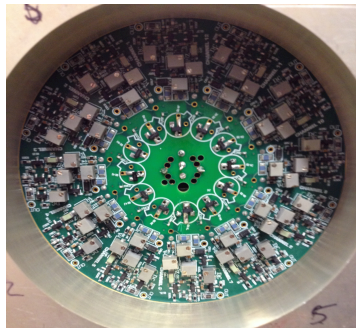
Analog Electronics for Ultra-Low Background Detectors

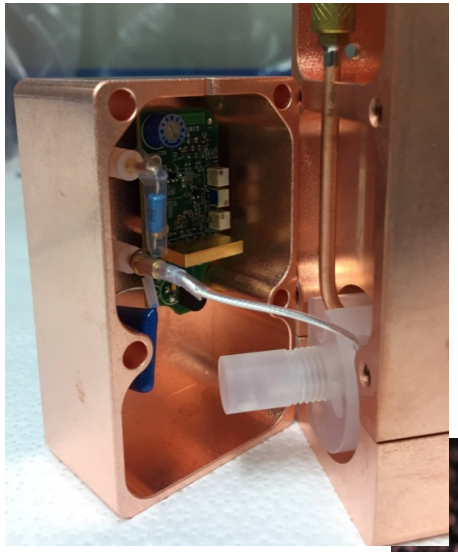
- Preamplifier front-end electronics design
- Ultra-clean material selection, assay, and assembly
- Custom cleanroom integration with detectors

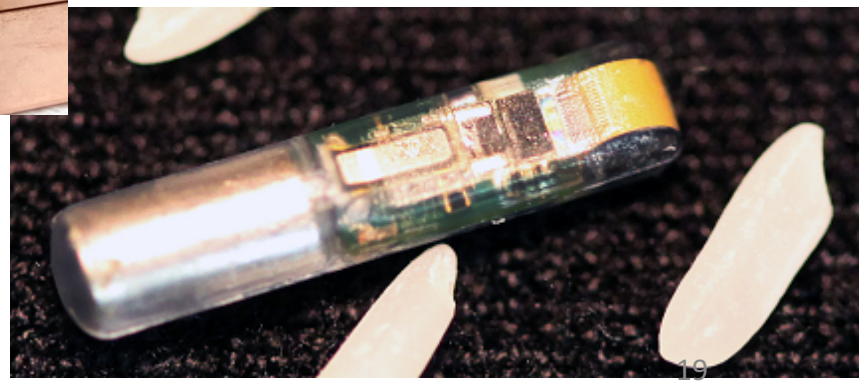
Low-Power, Miniaturized Circuitry

- Injectable fish tags for salmon dam survivability assay
- Custom battery and low-power electronics design





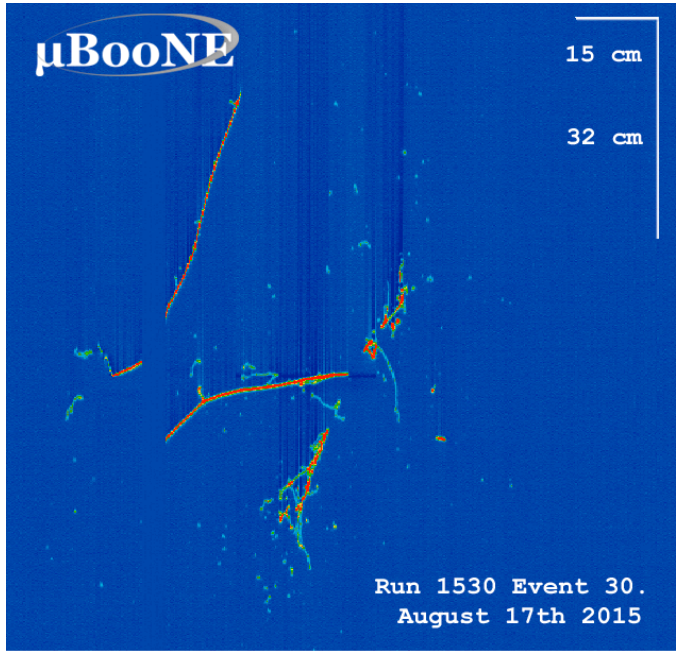


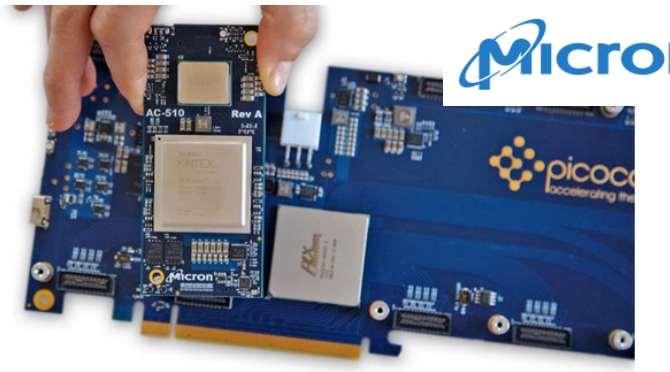


Deep Learning – micro-BooNE

- PNNL has expertise in deep learning for Science and National Security efforts
- As members of the DUNE DAQ consortium, we have performed early work in our partnership with Micron/Pico Electronics in Seattle to put Deep Learning inference on FPGAs for triggering purposes
- Leveraging national security investments, we are looking at ways to identify beam-off physics such as proton decay

This event can fake proton decay:





A board like this one could be a DUNE DAQ FELIX replacement for the BNL711.

Rice University

Paul Padley

4 Faculty

- Karl Ecklund (Particle Physics, CMS)
  - Pixel/Tracker front end daq electronics/software
  - US CMS manager Phase 2 Pixels
- Paul Padley (Particle Physics,)
  - US CMS Detector operations manager
  - Long history of DAQ and Trigger projects
    - Currently trigger elements of CMS muon trigger
    - http://padley.rice.edu/cms
- Frank Geurts (Heavy Ion, STAR, CMS)
  - On CMS, endcap muon system online systems
- Wei Li (Heavy Ion, CMS)
  - DAQ software

4 Engineers

- M. Matveev, Ph.D. Research Electronics
  - FPGA Programming, board design, optical links
  - Involved in various components of CMS endcap muon trigger electronics
- Ted Nussbaum, EE
  - Analogue electronics, board design, FPGA programing
- Jinghua Liu
  - CMS Endcap muon system online software
- Andrea Petrucci
  - CMS DAQ software.

SLAC

Mathew Graham, Günther Haller, Ryan Herbst

- RCE Platform
  - Flexible modular platform for DAQ and trigger applications
    - Low latency network inter-connected platform of FPGAs
    - Deployed for ATLAS, HPS, ProtoDune
    - Development for LSST, KOTO, LDMX
  - Collaborating with Oxford on upgraded version of DPM for deep data buffering
  - Interested in working with other collaborators for additional version of the DPM and COB
    - Alternative FPGA families
    - Additional interconnects such as Hybrid Memory Cube(HMC)
- LCLS-2 DAQ & Fast Detector Development
  - Front end triggering and data reduction at the camera
  - Back end data processing with hardware acceleration in the server farm, machine learning, image processing, etc.
- LCLS-2 Accelerator Controls and Beam Line Data Acquisition in ATCA
  - 1Mhz beamline data acquisition
- RF based DAQ system in ATCA
  - High frequency multiplex RF readout of Transition Edge Sensors (TES)

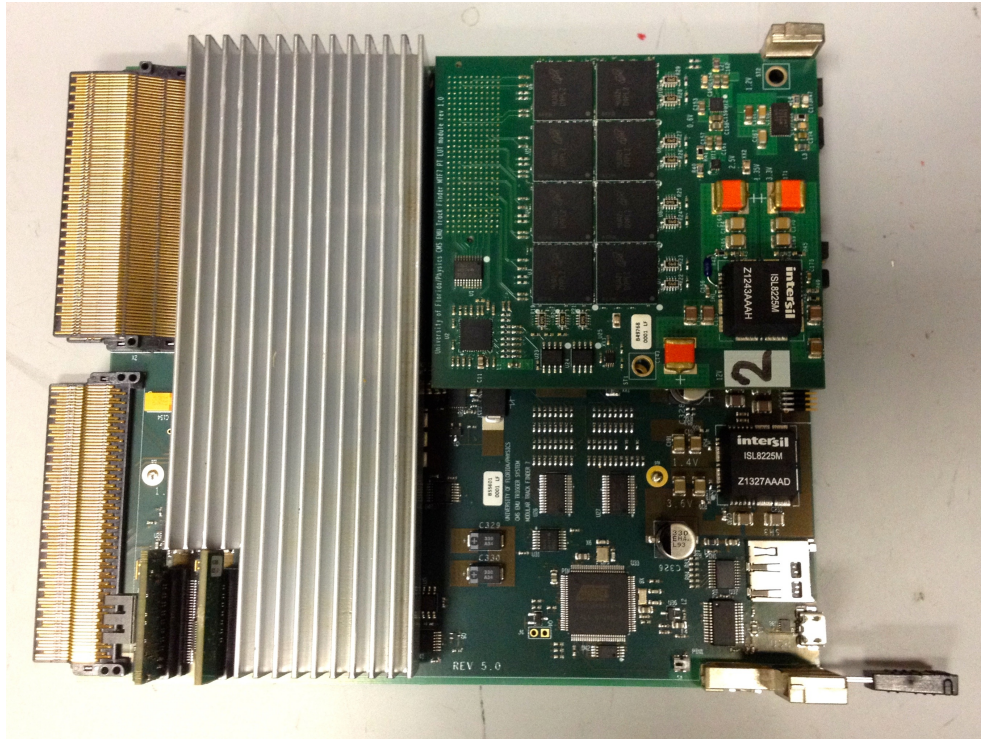
- FPGA design expertise
  - Modular design approach to accelerate application development
  - Extensive open source library of protocol and interface libraries
    - Ethernet: ARP, DHCP, ICMP, IPV4, UDP, RDUP
    - JESD204b
    - AMBA based protocol cores
      - AXI-Lite for register access
      - AXI-Stream for high speed streaming interfaces
      - AXI for DMA and bulk memory access
    - RF libraries for detector and controls applications
      - LLRF for accelerators
      - Laser locker and precision timing
      - TES readout
      - Beam Position Monitors (BPM)
- Interested in multi-lab collaboration in shared libraries
  - Use, test and extend existing libraries
  - Add new modules to existing libraries
  - Collaborative development on future interface and common modules

University of Florida

Darin Acosta, Ivan Furič, Jaco Konigsberg

U Florida Trigger-DAQ Activities

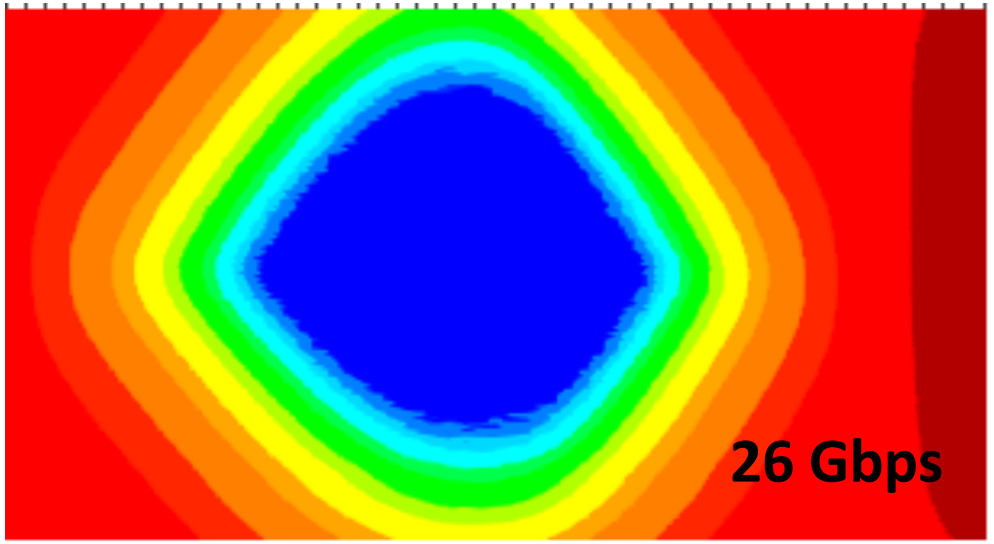
Phase-1 “MTF7” board, uTCA format with mezz.



- Level-1 Endcap Muon Triggers for CMS
  - CSC Track-Finder, 2008-2015
  - Phase-1 Endcap Muon Track-Finder, 2016–
  - HL LHC Endcap Muon Trigger, ~2026--
- Salient Features:
  - Optical link I/O (1.6Gbps→10Gbps→26Gbps)
  - Large FPGA for standalone muon track-finding (Xilinx V5→V7→US+)
  - Large on-board RAM for PT Look-up Table (4MB→1GB→64GB)
- Algorithms:
  - Track building: Extrapolations → Patterns
  - Measurement: Likelihood fit → Machine Learning (BDTs, DNNs)
  - Achieving same rates in endcap as for barrel region
- Firmware:
  - Early adopter of high-level synthesis: single source code for synthesis and software emulation (custom macros → Vivado HLS)
  - Good collaboration with NSF CHREC center at UF (ECE Department) for firmware projects

U Florida Trigger-DAQ Activities

- HL LHC Level-1 AM-based Track-Trigger for CMS
  - Track reconstruction using stubs from double-sided outer tracker modules
    - 4 μsec latency w/ high-efficiency and offline level p_T resolution (@ <200> pileup)
  - One of 3 approaches considered
  - In collaboration with Fermilab et al. [NW, TAMU, Italy, France, Brasil]
  - Associative Memory + FPGA and Pulsar board projects
    - Simulation framework development
    - Study and optimization of patterns & data flow
    - Implementation in vertical slice demo [w/ AM instanced in FPGA] => meeting specs
- R&D
  - Development of an ATCA "Advanced Processor" in collaboration with U Wisconsin
  - Samtec Firefly optical link tests from 14G→28G
  - DD4 RAM tests

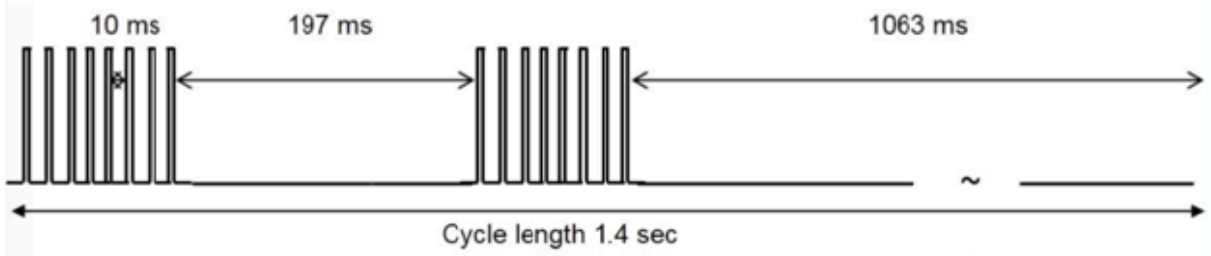


University of Kentucky

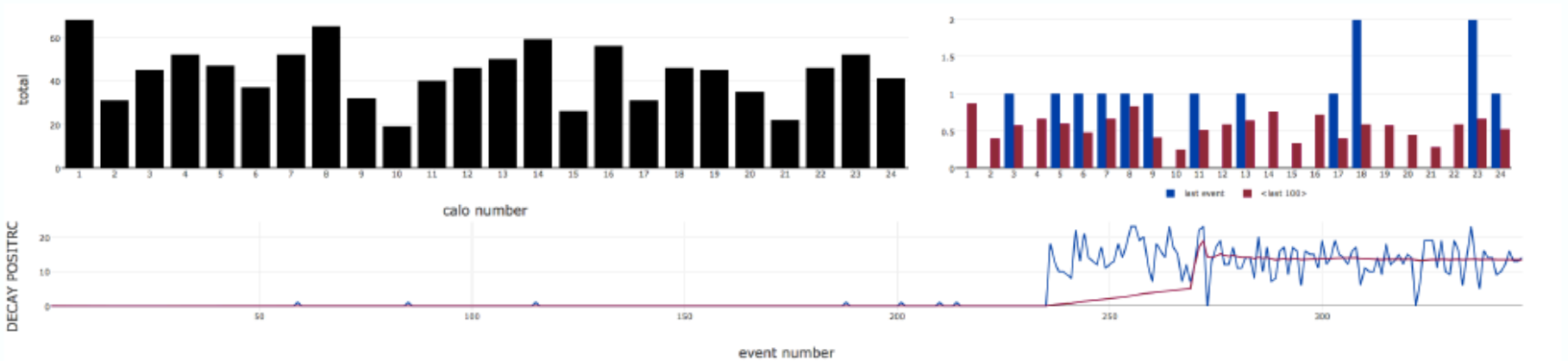
Wes Gohn

g-2 DAQ Design

- Must accommodate 12 Hz average rate of muon fills that consist of sequences of eight successive 700 μs fills with 10 ms fill-separations.

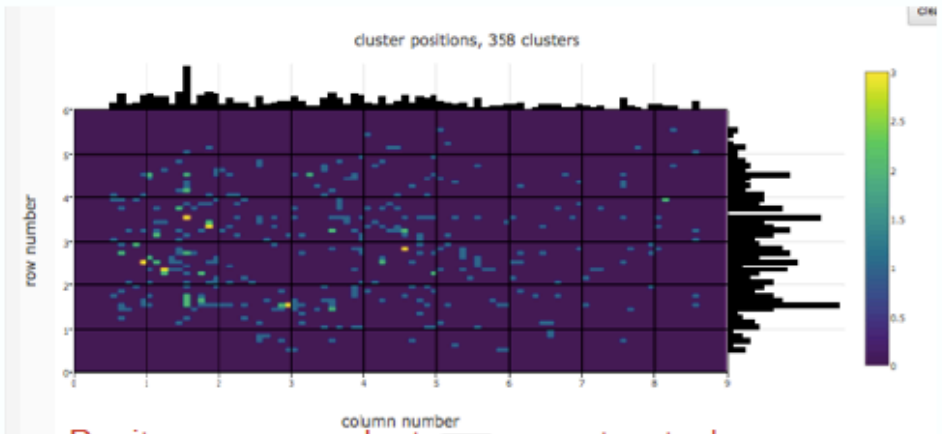


- Data is processed from 1296 channels of 12 bit 800 MSPS waveform digitizers.
- Time-averaged rate of raw ADC samples is 20 GB/s, which must be reduced by a factor of 100.
- Data is processed in GPUs to accomplish this task.
- We use the MIDAS data acquisition software for our DAQ.
- Total data on tape after 2 years of running will be 7 PB.
- An online data quality monitor uses *art* with ZeroMQ, node.js, and plotly to display data.

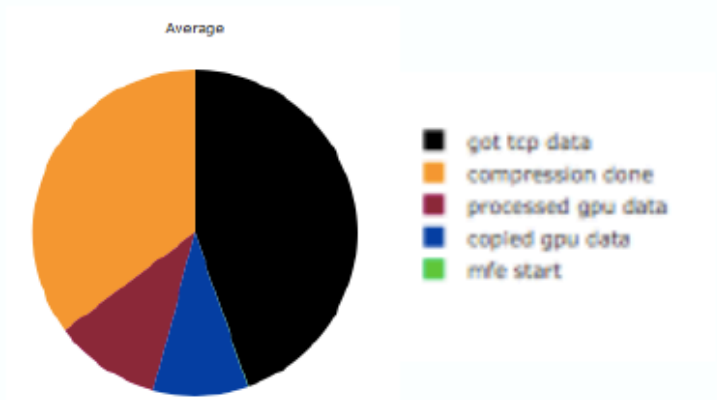


DAQ with GPUs

- The Muon g-2 DAQ uses 28 Nvidia Tesla K40 GPUs to process data.
- Each K40 has 2880 CUDA cores and 288 GB/s memory bandwidth and ECC memory protection.
- MIDAS frontends are written in C++ with CUDA and multithreaded with mutex locks.
- Must process each event in < 83 ms to keep up with fill rate.
- Most time is taken by copying data from TCP socket to GPU memory. Data processing in GPU is very fast.



Positron energy clusters reconstructed from template fits in GPU.



Breakdown of processing time for each event.

University of Wisconsin - Madison

Wesley Smith

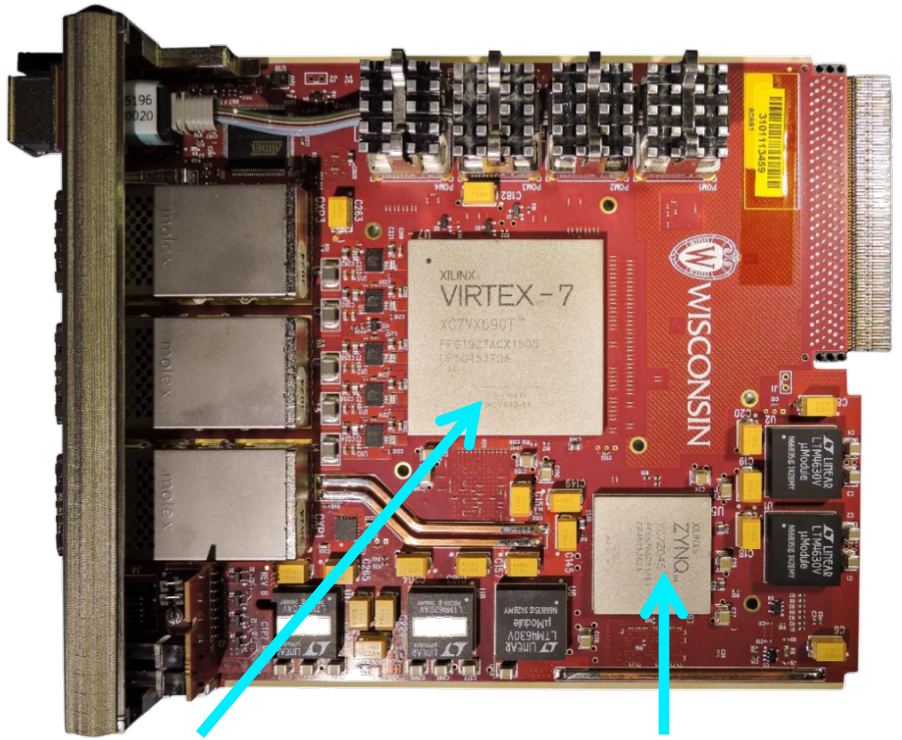
Collaboration: UW CTP7: CMS Phase 1 & HL-LHC

- Operation in CMS since 2015:
  - CMS Phase 1 Level 1 Trigger
  - Layer-1 Calorimeter Trigger
    - 22 CTP7s
  - Integrated Eye Scan capability: non-invasively capture eye diagrams on live operational data
  - Automatic Error Handling
- HL-LHC R&D: Cornell Track Trigger demonstrator test setups
  - 4 CTP7s @ CERN
  - 2nd setup at Cornell: 4 CTP7s
- HL-LHC CMS Endcap Muon and H/ECAL readout, Calorimeter and Correlator Trigger prototype setups: platforms for FW development and testing:
  - CERN (3 setups), Texas A&M, Fermilab, Notre Dame, Princeton, Rutgers, UCLA, Wisconsin

U. Wisconsin CTP7 MicroTCA Card for Phase 1 Cal. Trig.

12 MGT MicroTCA backplane links

67 Rx and 48 Tx 10G optical links



Virtex-7 690T FPGA (Data Processor)

ZYNQ `045 System-on-Chip (SoC) Device (embedded Linux control platform)

UW TDAQ R&D Activities

- Explore hardware technologies targeted for the Phase 2 upgrade
  - ATCA Form Factor including Rear Transition Module
  - MGT Link design beyond 10G line rates (16G, 25+G)
  - Efficient cooling of next-gen FPGAs
  - Next generation IPMI and embedded Linux solutions
  - First ATCA Prototype in 2018, Demonstrators in 2019
    - APd1 Block Diagram available on next slide
  - US CMS “Consortium” collaborating on various aspects
    - US CMS Trigger and Calorimeter and Muon Readouts
    - U. Florida, UIC, Fermilab, Notre Dame, UCLA, Texas A&M
      - e.g. U. Florida on advanced RAM/FPGA interconnections, links
- Firmware R&D
  - High Level Synthesis (HLS) of Trigger Algorithms
  - Firmware demonstrator using CTP7, Xilinx Vivado HLS in a dedicated framework environment
    - Design trigger algorithms and test derived FW to determine resources, latency, etc.