Front-End Electronics DP Consortium Deliverables

**Introduction:**

The Front-End Electronics DP consortium deals with the analog front-end cryogenic electronics for the charge readout (based on dedicated large dynamics dual-slope ASIC chips) and the FE digitization system (for both charge and light readout) which is hosted in uTCA crates located close to the signal feedthrough chimneys, for the charge readout, and near the PMTs signal feedthroughs of the light readout.

The charge readout system is designed for continuous, non-zero-suppressed, zero-loss-compressed readout of 3m long charge readout strips, arranged in two collection views of 3 mm pitch on the anode PCBs of the Charge Readout Planes (CRPs). Dedicated signal feedthrough chimneys allow operating the analog charge readout FE electronics at a temperature around 100K, while keeping the possibility of replacing the FE cards without contaminating the pure liquid argon volume. The analog FE cards, hosting the cryogenic ASIC chips, are plugged on a cold flange at the bottom of each chimney. The cold flange ensures the UHV tightness with respect to the pure liquid argon volume. The other side of the flange, inside the cryostat, is connected to the CRPs with flat cables. The FE cards are mounted on 2m long blades which support the connection cables for signals and LV and allow for the insertion or extraction of the FE cards in/from the cold flange connectors. The SFT chimneys are closed at the top by a warm flange which dispatches differential analog signals to the AMC cards in the uTCA crates and allows for the connections of the low voltage lines, calibration and control signals. The AMC cards include also a last stage of shaping at the input of the ADCs. The AMC cards host dual port memories and an FGA with a virtual processor (NIOS) which takes care of the readout and of the data transmission over the network. Digitized data are collected by the MCH switch in the each crate and transmitted from the uTCA crates to the DAQ back-end via optical fiber links at 10 or 40 Gb/s. The uTCA crates host the digitization AMC cards for the charge and light readout with a high channel density (with a minimal target figure corresponding to the present channel density already achieved in ProtoDUNE-DP of 640 channels per crate, 64 channels/card, 10 AMCs per crate). A White Rabbit slave node card is also inserted in each uTCA crate for timing/trigger distribution on the backplane of the crate to the AMCs.

The detection of the direct scintillation light is the main purpose of the light readout electronics in order to provide the absolute time. The system will also be capable to detect the so-called proportional scintillation light produced by the electrons extracted and amplified in the gaseous phase. The actual photon detectors are assumed to be coated PMTs located under the cathode. The system will group up to 16 PMTs to be read by a single AMC card in uTCA standard. The different cards are inserted in uTCA crates and the events are time stamped using the White Rabbit system of the charge readout by including in each uTCA crate a White Rabbit slave node card. The use of the uTCA standard allows a cost-effective integration of the light read-out electronics together with the charge readout electronics into the global DAQ system. As for the charge readout each crate is connected to the back-end via an optical fiber links for the data and White Rabbit.

**DP Front-End Electronics Consortium Deliverables:**

1. Hardware Deliverables
	1. Front-end cryogenic ASIC
		1. Design
		2. Production
		3. Testing
	2. Front-end cryogenic cards
		1. Design
		2. Production
		3. Testing
	3. Cold flanges, cables and insertion blades of Signal Feedthroughs (SFT) chimneys
		1. Design
		2. Production/assembly
		3. Testing
	4. Warm flanges of SFT chimneys
		1. Design
		2. Production
		3. Testing
	5. SFT chimneys
		1. Design
		2. Fabrication
		3. Assembly with cold and warm flanges
		4. Testing
		5. Installation (SURF)
	6. Signal cables from SFT chimneys to uTCA crates
		1. Selection/Validation
		2. Fabrication/Procurement
		3. Testing
	7. Analog FE Low-voltage, pulsing and control Cables
		1. Selection/Validation
		2. Fabrication/Procurement
		3. Testing
	8. uTCA crates and MCH
		1. Selection/Validation
		2. Fabrication/Procurement
		3. Testing
	9. uTCA AMC digitization cards
		1. Design
		2. Firmware development
		3. Production
		4. Testing
	10. uTCA White Rabbit slave nodes
		1. Design
		2. Production
		3. Testing
	11. Low-Voltage Power Supplies
		1. Selection/Validation
		2. Procurement
		3. Testing
	12. Light Readout FE electronics
		1. Design and production of interface between PMTs and FE
		2. Development of the analog section
		3. Development of the digital section
		4. Integration into micro-TCA backplane
		5. Component selection and procurement
		6. Cards production and testing
		7. Programming of FPGA to provide trigger and fast signal treatment
		8. Programming interface to micro-TCA back plane and DAQ
		9. Synchronization with White Rabbit
	13. FE Electronics Infrastructure
		1. Develop Cables Routing Plan (optical fibers for White Rabbit and data, LV, calibration and controls)
		2. Design LV filtering/distribution boxes and cable support structures
		3. Fabricate LV filtering/distribution boxes and cable support structures
		4. Develop Installation Plan
		5. Integration of LV power supplies
		6. Install FE electronics + blades in the chimneys (SURF)
		7. Installation of light readout FE electronics
		8. Installation of uTCA crates + MCHs + AMCs + WR slaves (SURF)
		9. Cabling of uTCA crates to SFT chimneys (SURF)
		10. Cabling of LV, calibration and controls to chimneys (SURF)
		11. Cabling of fibers (data and White Rabbit) to backend (SURF)
		12. Test electronics/cables (SURF)
2. Software Deliverables
	1. Simulation Code
		1. Analog Signal Processing
		2. Digital Readout
	2. Calibration
		1. Run Control Software
		2. Analysis Software
		3. Calibration Database
	3. Hardware Database
		1. QC Documentation
		2. Component Tracking
	4. Data Collection
		1. Hardware Initialization/Configuration Code
		2. Hardware Monitoring Code
	5. Data Monitoring Code
3. Physics Deliverables
	1. Validation of Cold Electronics Requirements with respect to Physics Performance
	2. Cold Electronics Performance Validation via ProtoDUNE Data Analysis
	3. Editing of TDR chapter
4. Integration Deliverables
	1. Detector Grounding & Shielding Plan
	2. Integration Test Facility
		1. Design
		2. Fabrication
		3. Operation