3D-IC technology trends and current development status for the stacked pixel detectors

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Outline

1. Introduction
   - Advantages of 3D-LSI
   - Road Map/Potential Application
2. Technology Approach
   - TSV process
   - Bond/Stack approaches
   - Examples of 3D integration
3. Pixel detectors
   - Background
   - Au cone bump using NpD method
   - Cylinder Bump for fragile semiconductor material
4. 3D Cost reduction approach
5. Summary

LSI Technology ≠ 3D-IC Technology

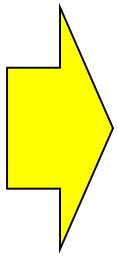
- Predictable
- Precisive but inflexible

- unpredictable
  Application driven technology
- Need flexibility
  System technology
  Many integration methods

3DIC Supply chain

Base devices

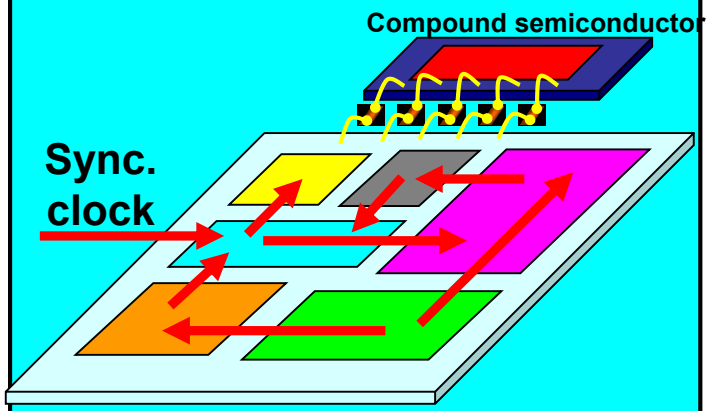
4 inch Si wafer
6 inch Si wafer
8 inch Si wafer
12 inch Si wafer
Shuttle service (LSI Chip)
Compound Semiconductor (Chip/Wafer)



3D integration

Unique Points of 3D-LSI

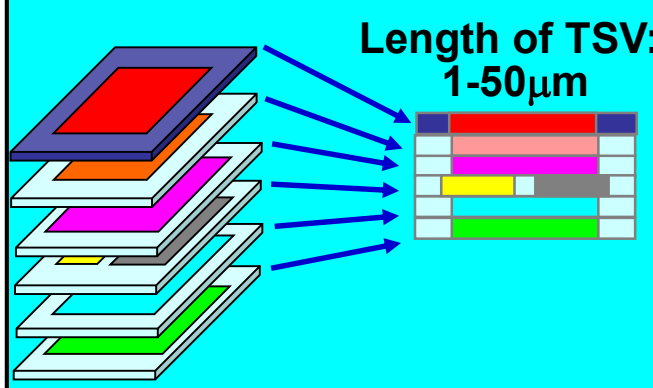
Conventional SoC



Long Global interconnect
→large RC delay, large C_P

Repartitioning Die

3D-SoC

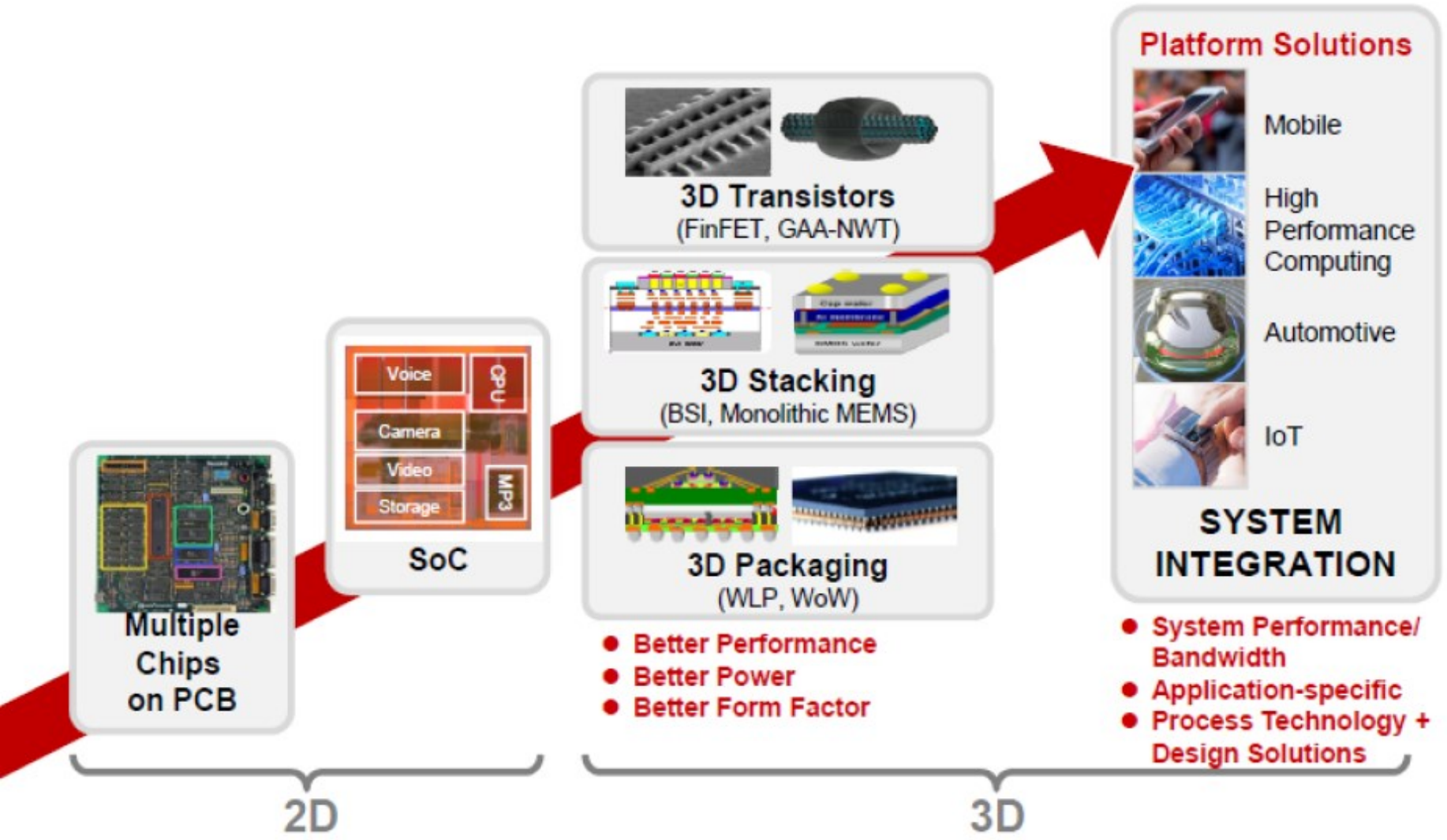


-Short global interconnect
→small RC delay, small C_P
-High band width
-Small form factor

1. Increase of electrical performances
2. Increase of circuit density
3. New Architecture (Hyper-parallel processing, Multifunction, etc)
4. Heterogeneous integration
5. Better yield

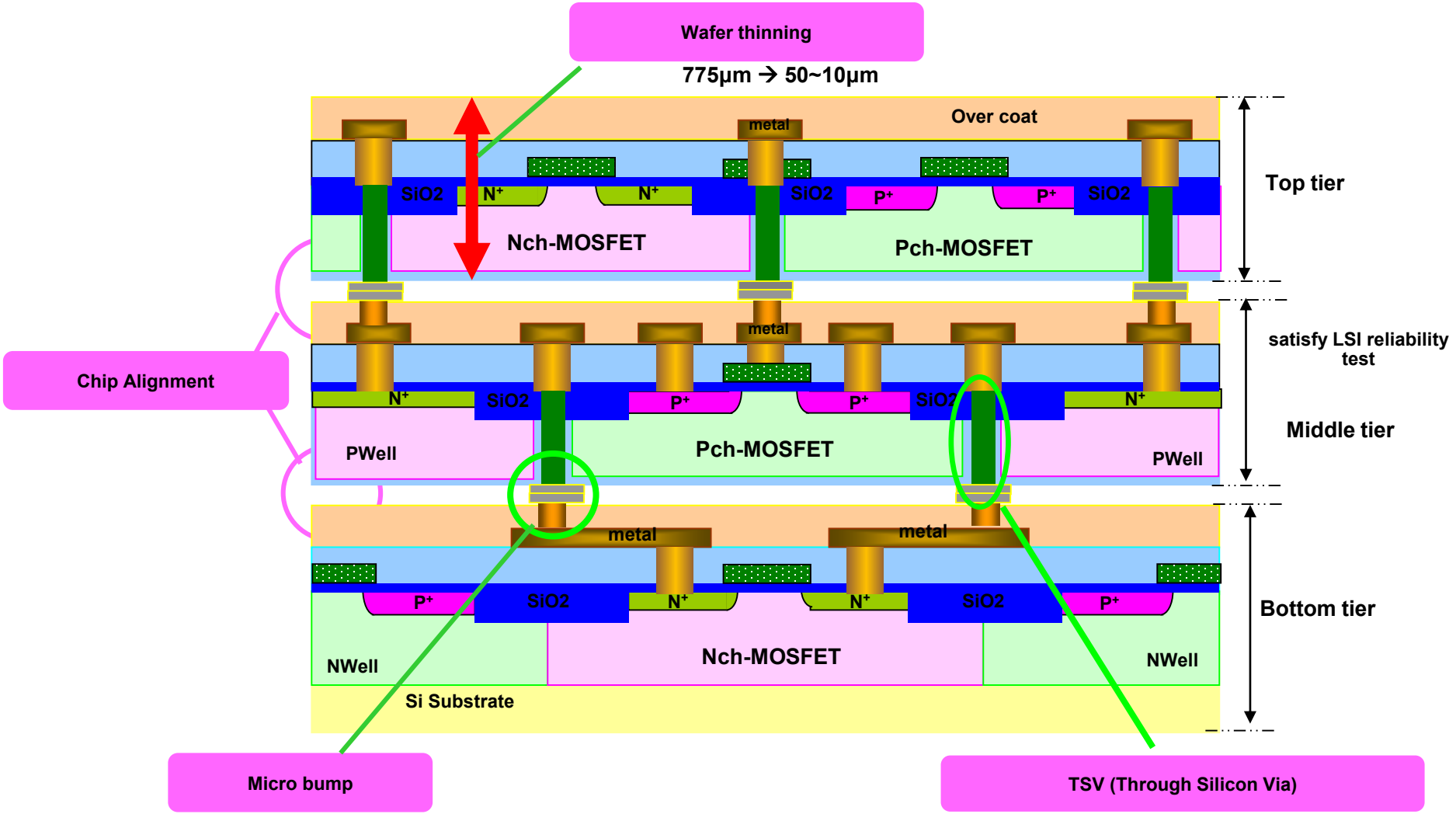
TSV : Through Silicon Via

Chip & System Integration Trends for better PPA & System Performance

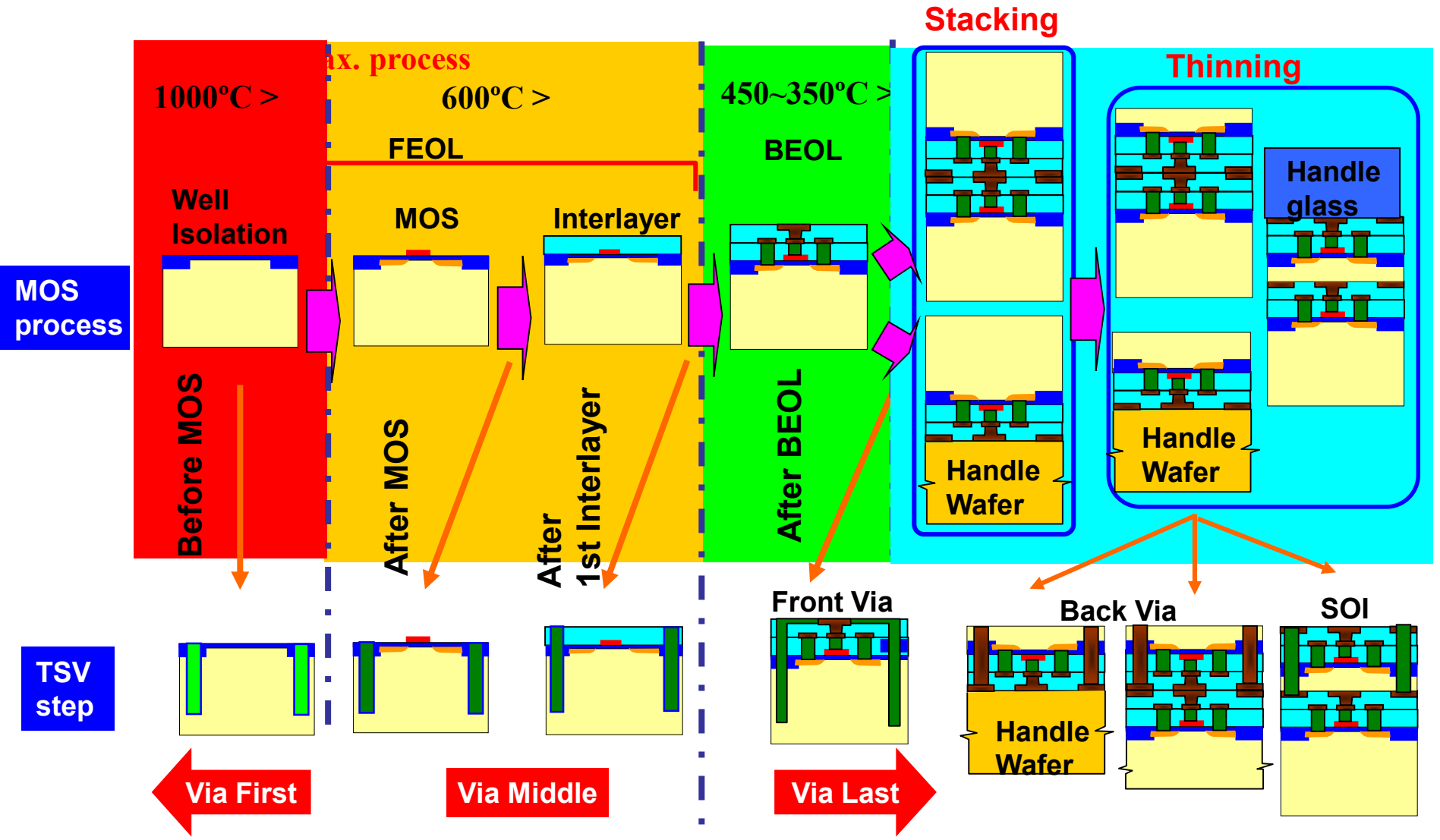


Source: Cliff Hou (TSMC), ISSCC 2017 (Plenary)

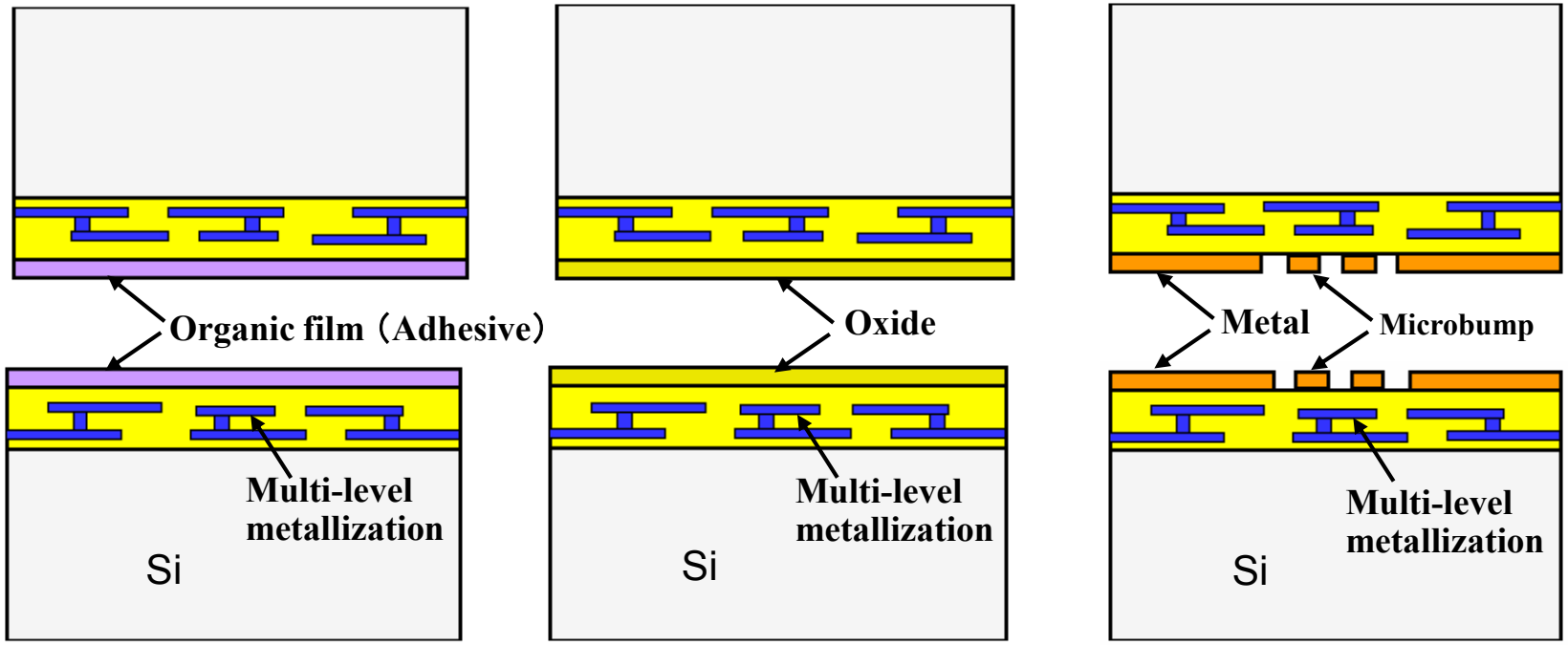
Key technologies of 3D-IC Integration



TSV process classification



Wafer Bonding Methods -1



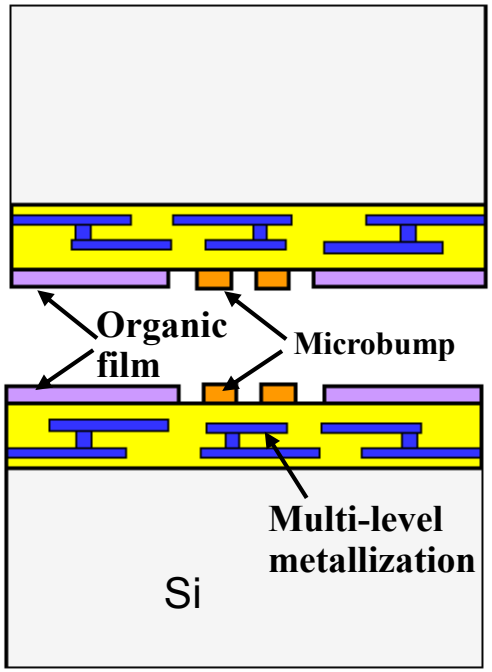
Adhesive Bonding

Oxide Fusion Bonding

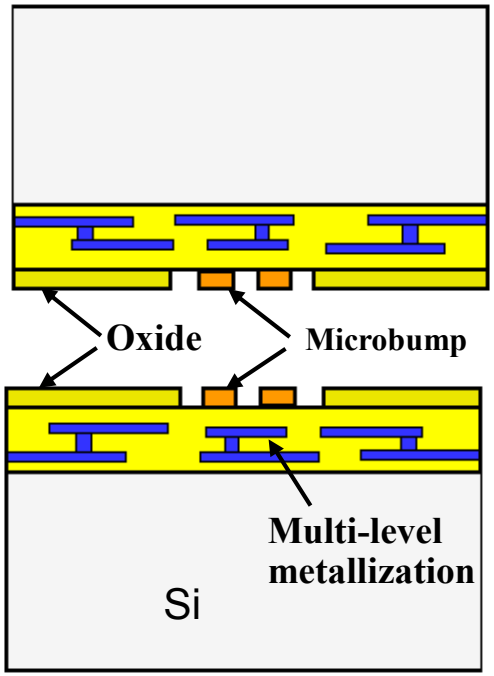
Metal (Cu) Fusion Bonding

Metal (Cu/SnAg) Eutetic Bonding

Wafer Bonding Methods -2



Adhesive/ Metal Bonding



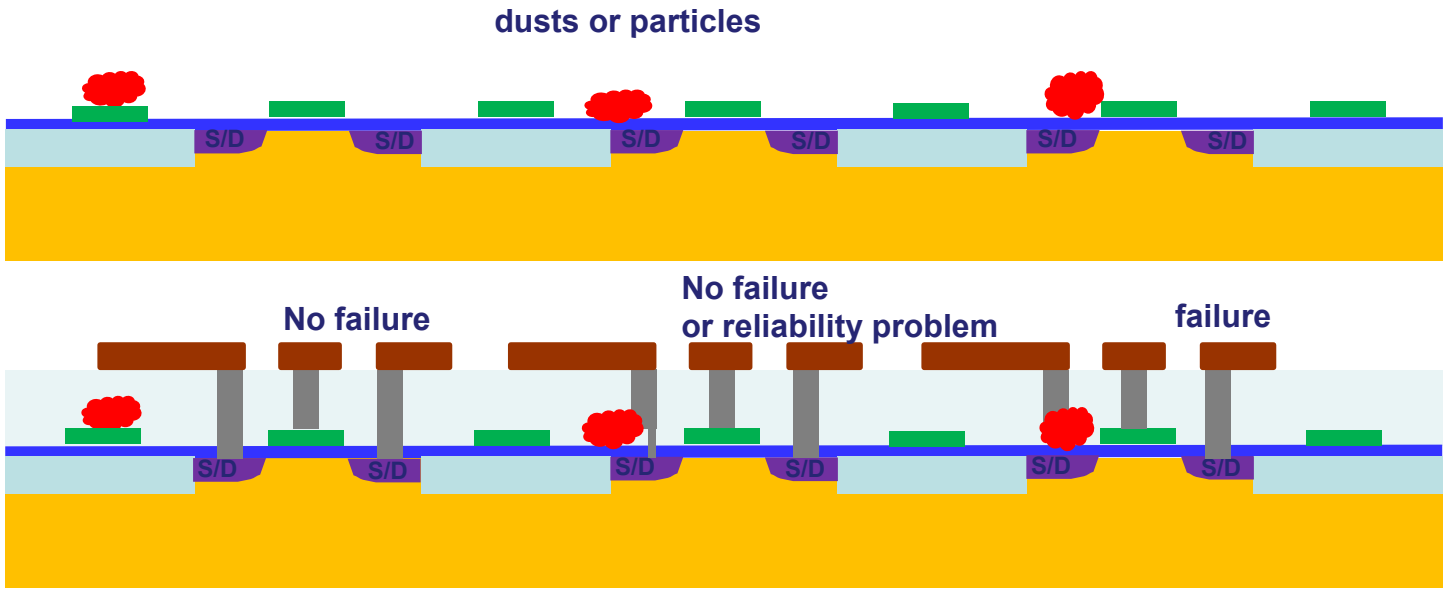
Oxide/ Metal Bonding

(Hybrid bonding)

Various types of 3D-IC Integration

Stack Approach / TSV process Conductor Mat.		Via first	Via middle	Via last		Process cost	Heterogeneous Integration
		before MOS	before Metal interconnect	after BEOL before Stack	after Stack		
		Poly-Si	W, Cu	W, Cu, etc	W, Cu, etc		
WoW	Bulk	MEMS	3D DRAM **3D Flash**	Image Sensor	Ziptronix IMEC Samsung •••••••••• IBM	Low	Impossible
	SOI			T-Micro etc.	MIT(Lincoln Lab.) RPI		
CoW		**MEMS**		-Heterogeneous Integration -Pixel detector		Low~ Middle	possible
CoC		**MEMS**	3D DRAM **3D Flash**		**T-Micro etc.**	High	possible

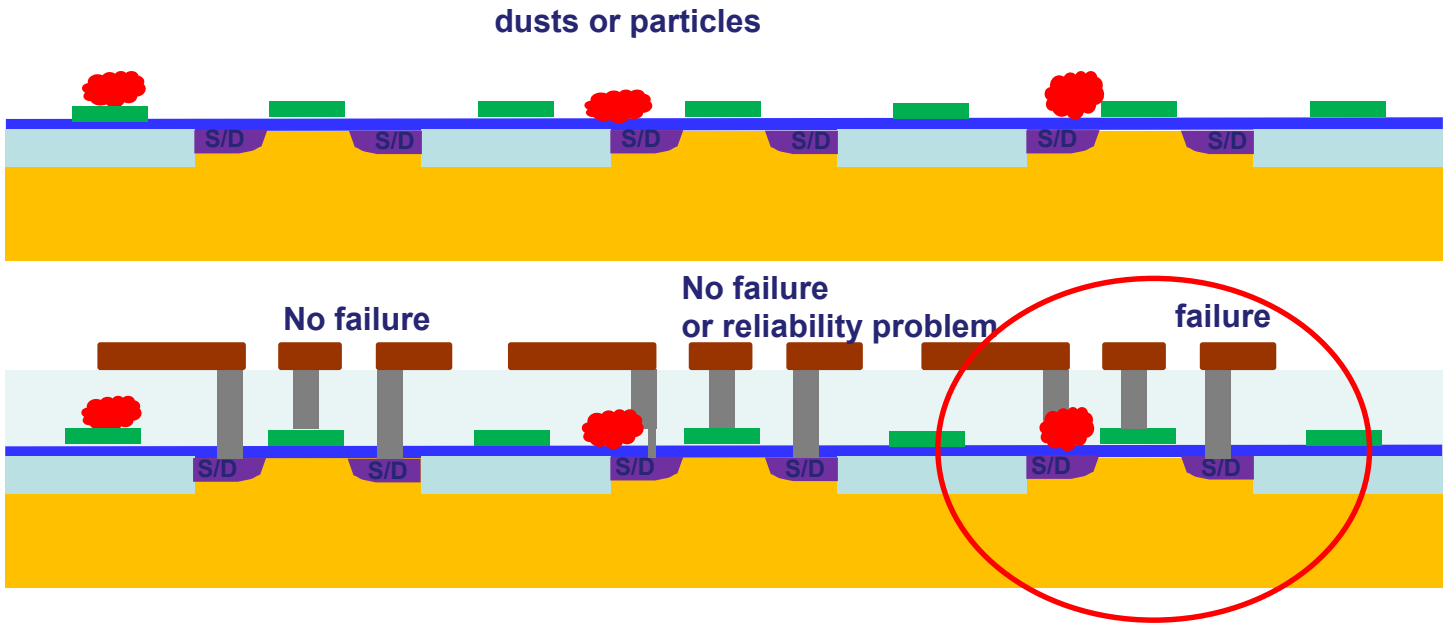
Yield loss by particles



Oxide CVD
CMP
Via patterning
Form metal interconnect

Yield loss by particles

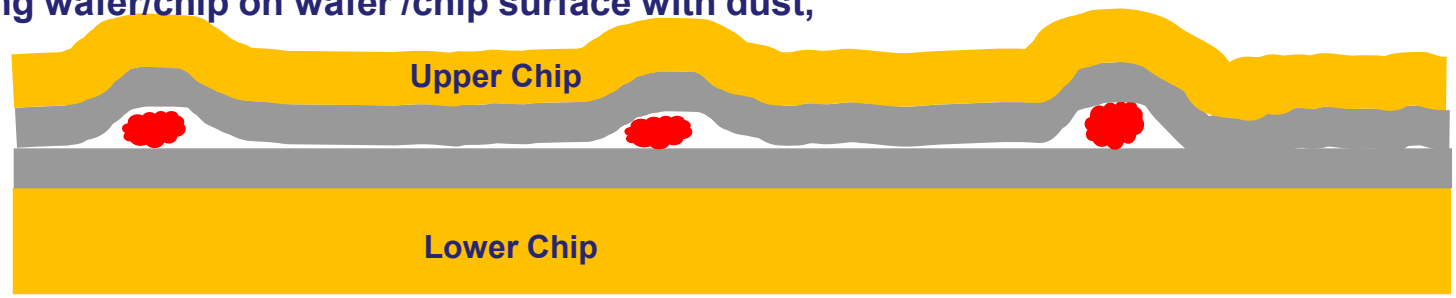
Oxide CVD
CMP
Via patterning
Form metal interconnect



We can only detect this failure from electrical testing.

Yield loss by particles

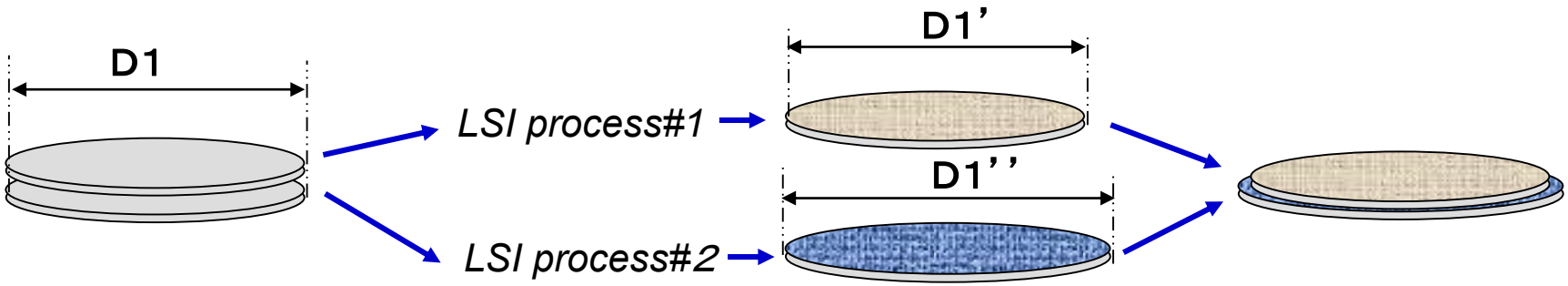
In case of bonding wafer/chip on wafer /chip surface with dust,



If the bonding method which needs microscopic smoothness and cleanliness, bonding yield will be affected by defect density of dusts and particles.
So we have chosen the bump bonding with adhesive injection.

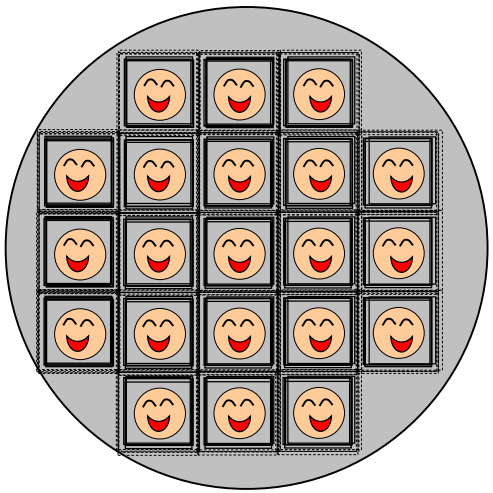
Issue of wafer to wafer bonding

(1) Shift of wafer size after wafer process

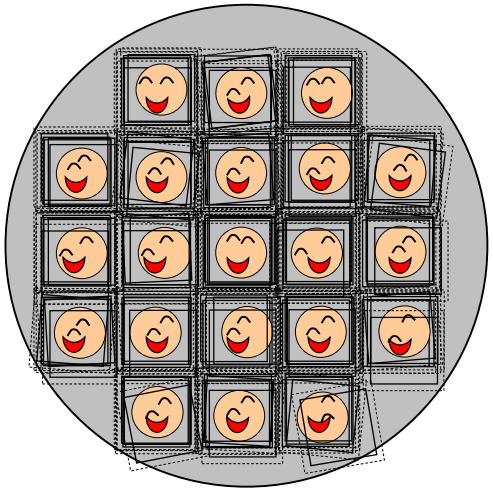


D1≠D1'≠D1"

(2) Alignment error of wafer process



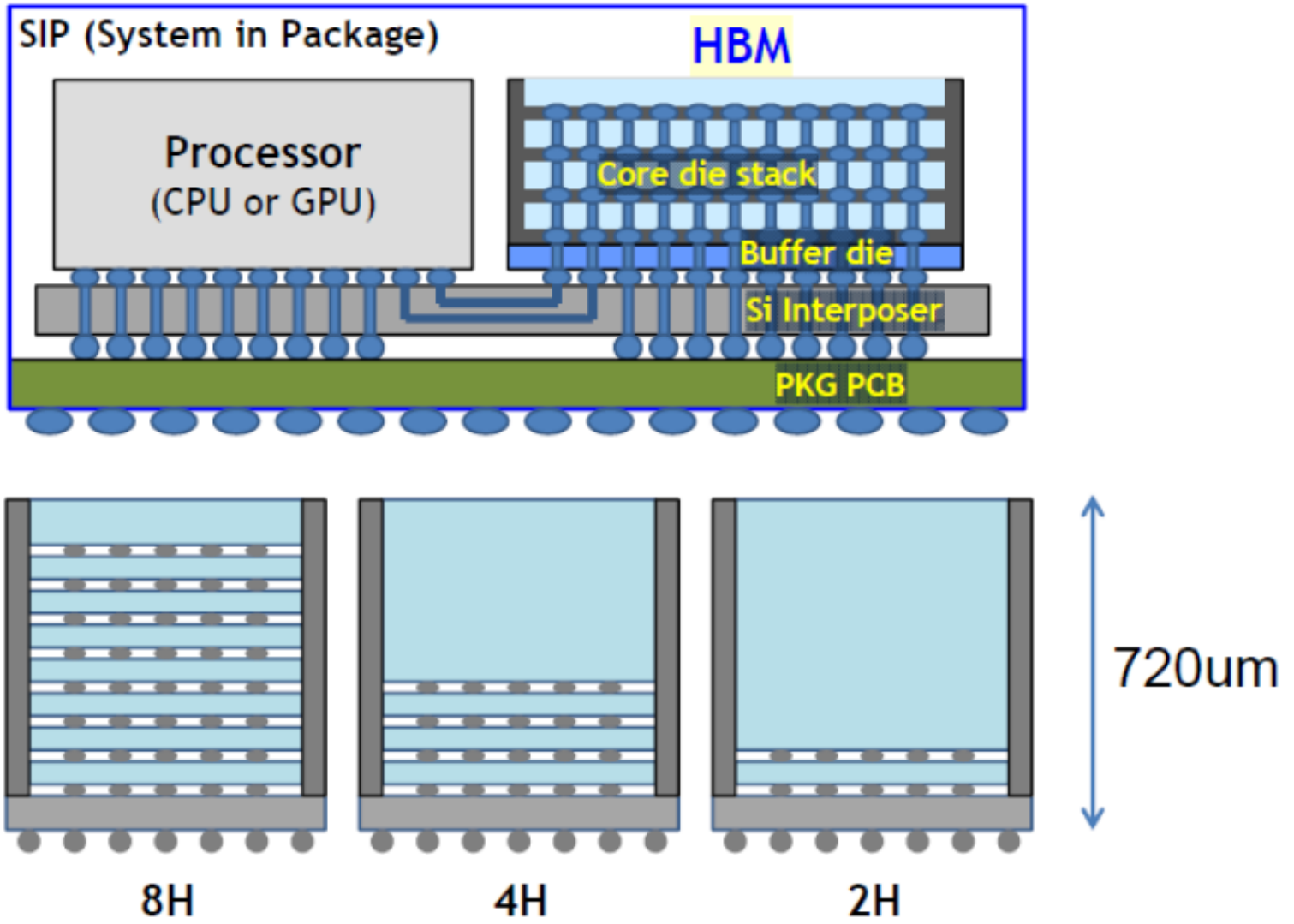
Ideal



Actual

HBM (High Band Width Memory)

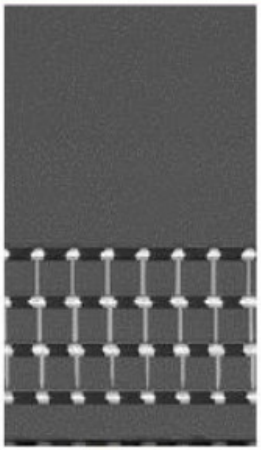
Commercialized 3D DRAM



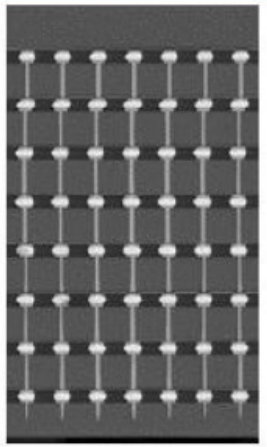
Source: Kyomin Sohn (Samsung), ISSCC2016

Cross-sectional View and Chip Photo of HBM

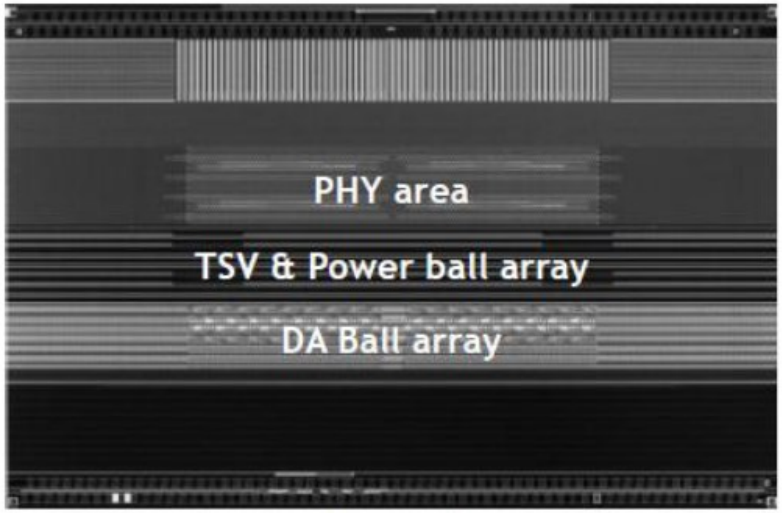
- Process: 20nm DRAM
- Capacity: 9Gb/core die
- Supply voltage: 1.2V/1.2V/2.5V
- Chip size: 12mm x 8mm (buffer die)



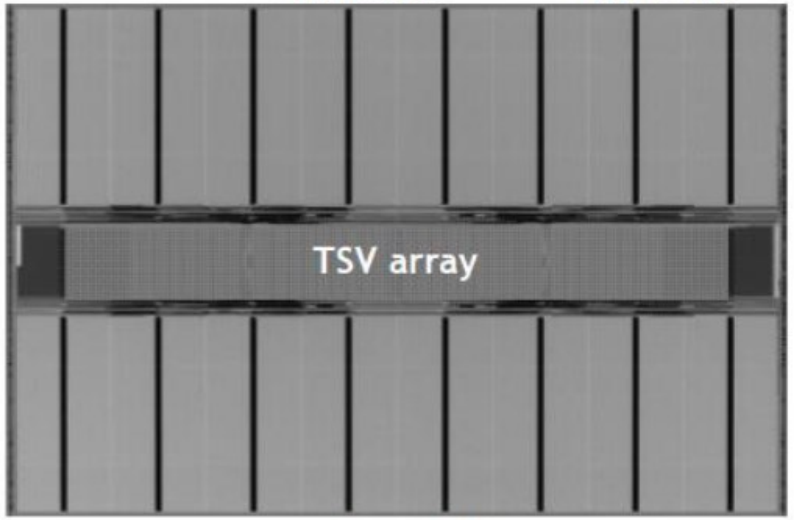
4H Case



8H Case



Buffer die



Core die

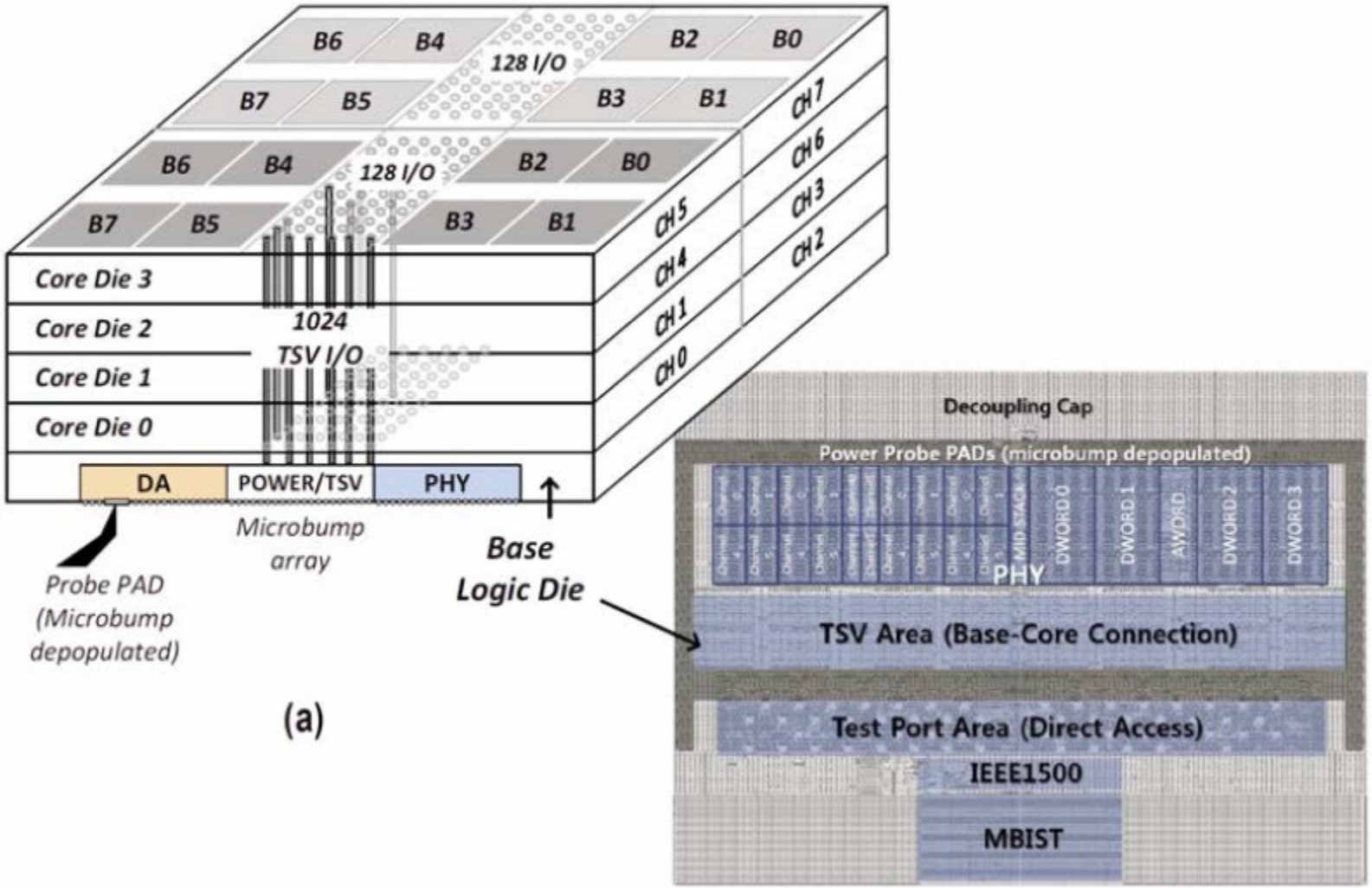
Source: Kyomin Sohn (Samsung), ISSCC2016

• Comparison table of GDDR5 and HBM Gen1.2

Items	GDDR5	HBM Gen1	HBM Gen2
Pin Data Rate	4~8Gbps	1Gbps	2Gbps
# of IO and CH	1CH, 32 IO	8CH, 128IO/CH	16pCH, 64IO/pCH
Bandwidth	16~32GB/s	128GB/s	**256GB/s**
Voltage (VDDC/VDDQ/VPPE)	1.35V~1.5V	1.2V/1.2V/2.5V	←
Interface	POD (VDDQ Term.)	CMOS (Un-term)	←
Banks	4banks/BG, 4BGs	←	←
Implemented new functions in this work			Pseudo channel, 2H/4H/8H, ECC storage, Implicit pre-charge, Lane remapping, …

Source: Kyomin Sohn (Samsung), ISSCC2016

SK Hinix/ 3D DRAM (High Bandwidth Memory: HBM)

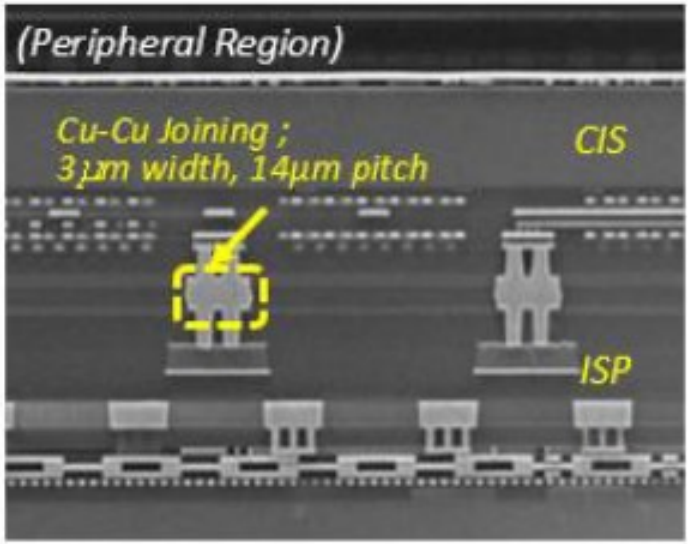


Sony / 3D-Stacked Image Sensor

Sony's first CIS module(IMX260) product with Cu-Cu Hybrid bonding

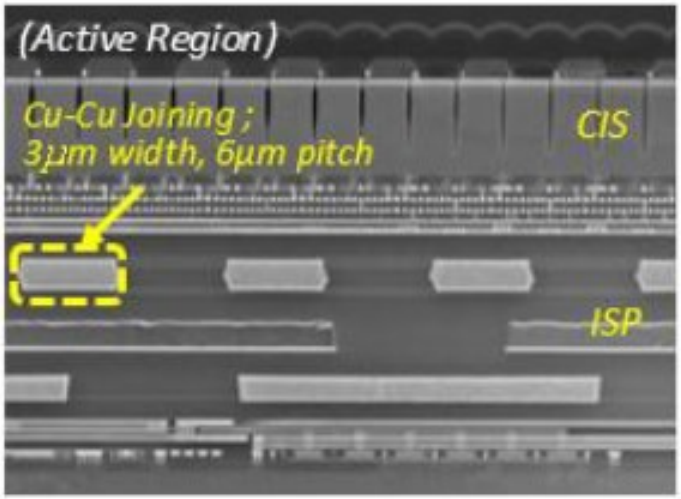
Cu-Cu Via

3um wide
14um pitch

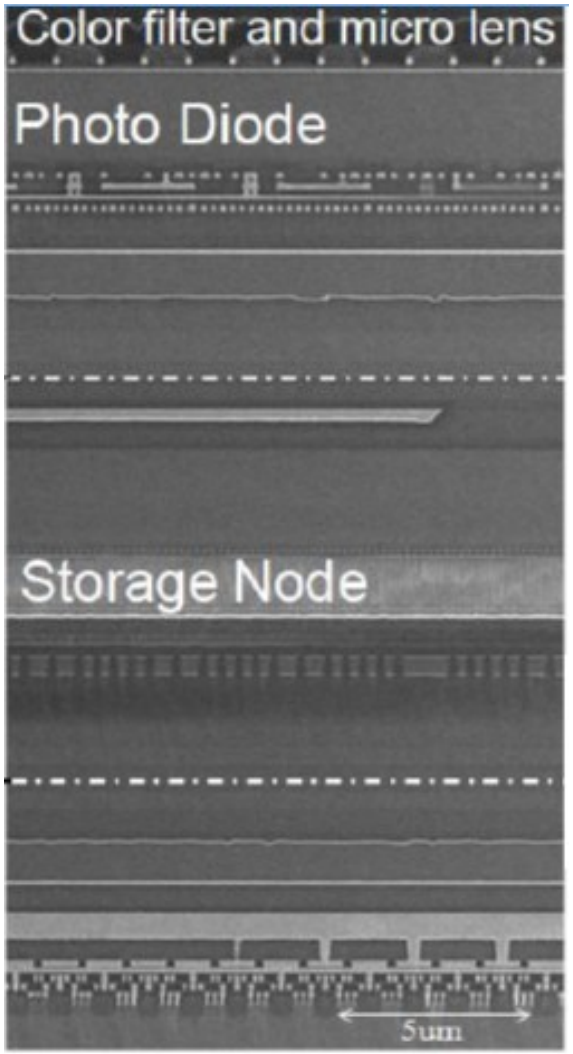


Cu-Cu Via

3um wide
6um pitch



Source: Chipworks, April, 2016



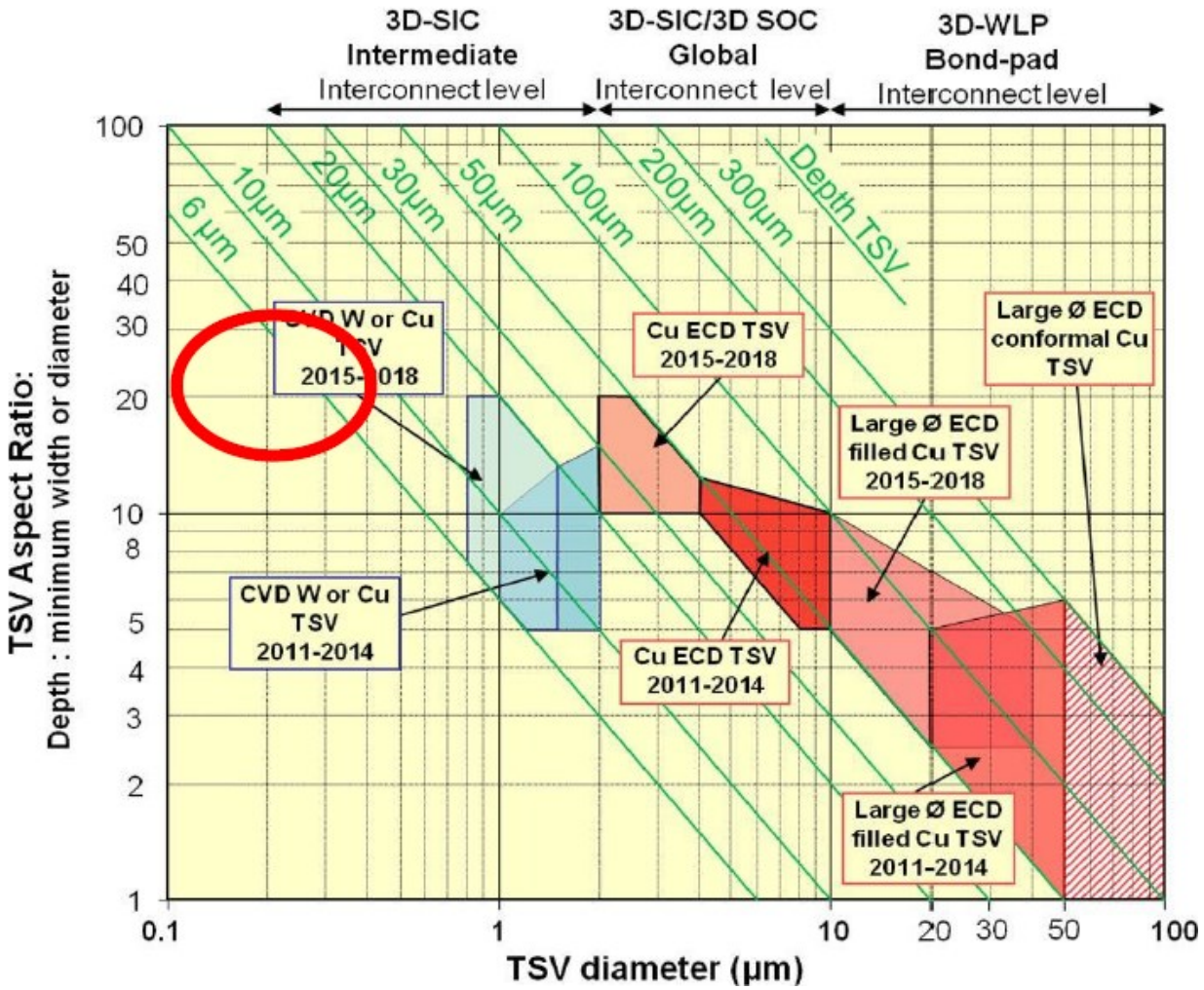
Top part
BI-CIS

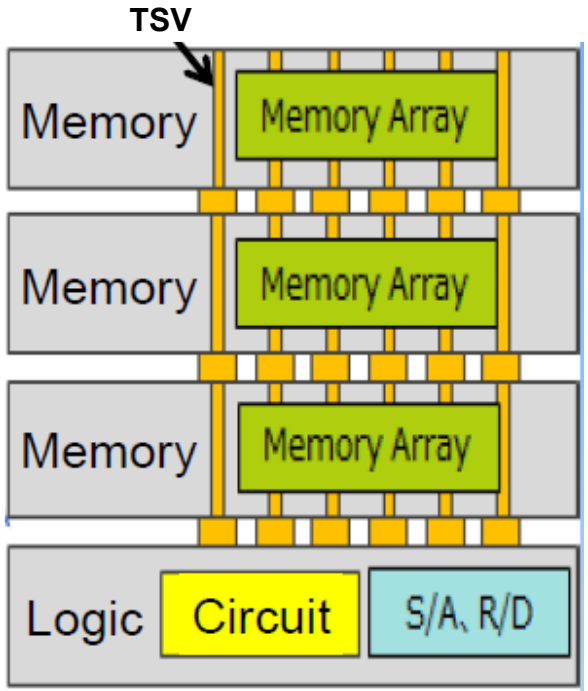
Middle part
DRAM

Bottom part
Logic

Source: T. Haruta (Sony) ISSCC2017

ITRS Road Map of TSV





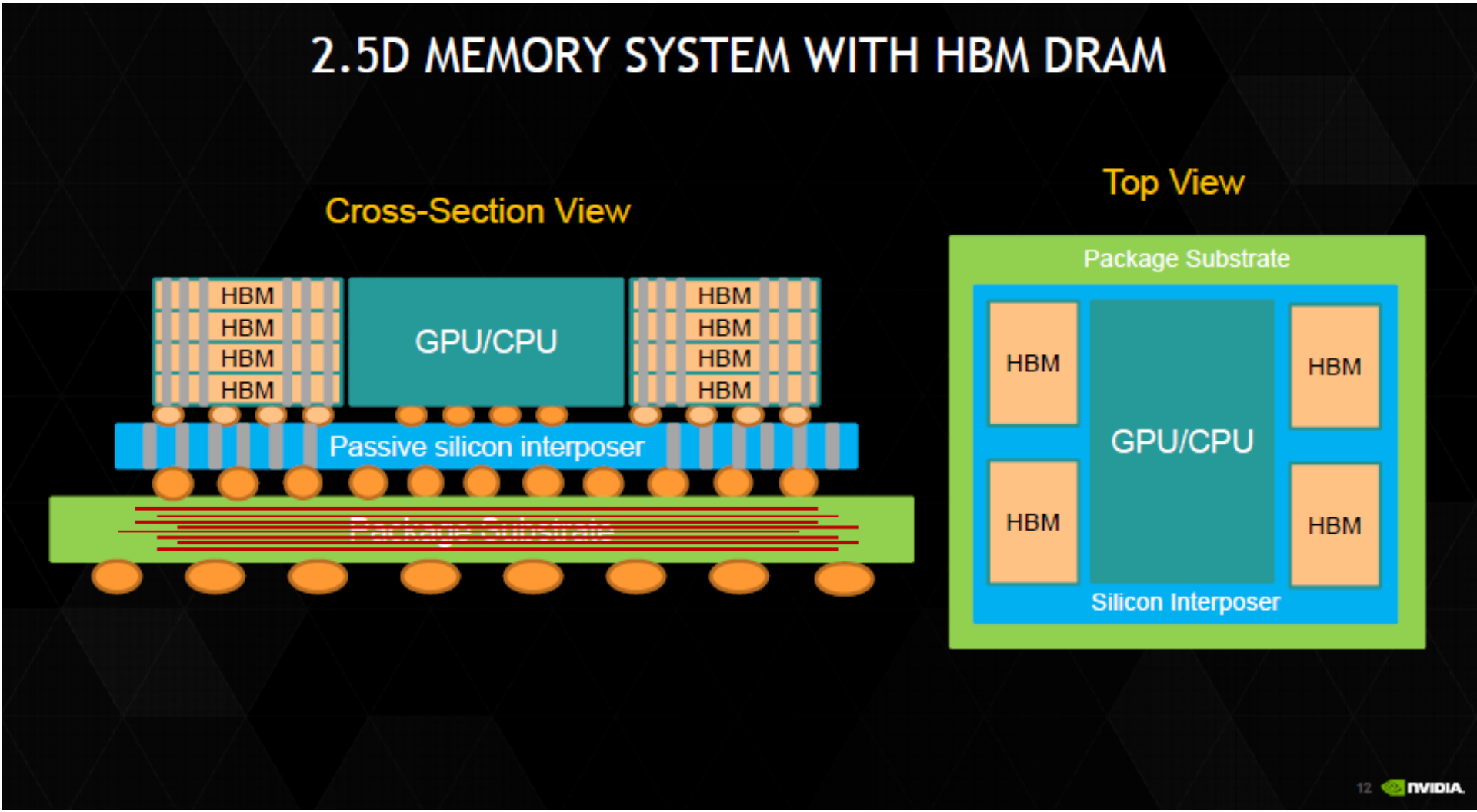
Low-power & high-bandwidth 3D Memory &Logic

Memory Density: >10TB
TSV length: <10um
TSV diameter: 0.5um

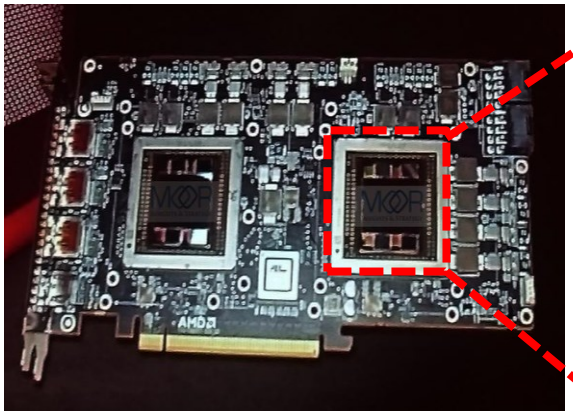
TSV is a leading-edge technology for new generation memory.

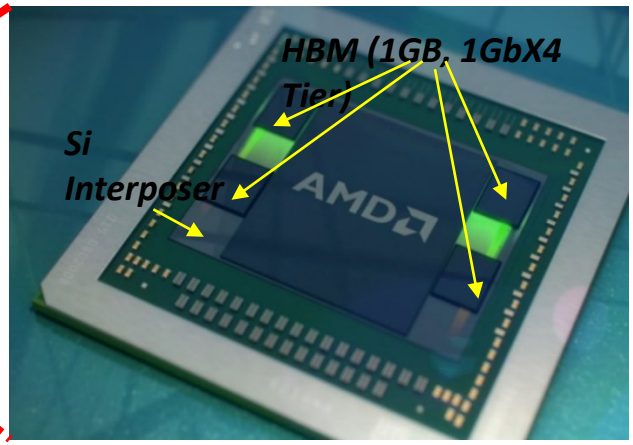
TSV scaling and increase I/O density are required for future 3D-ICs

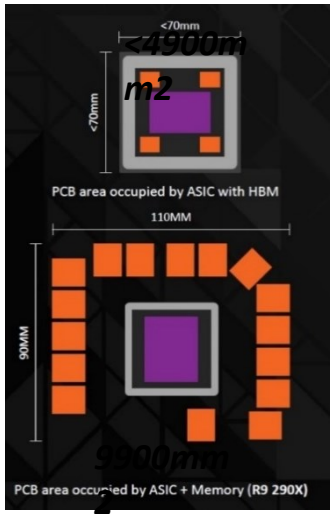
High Density Memory Systens using Si Interposer

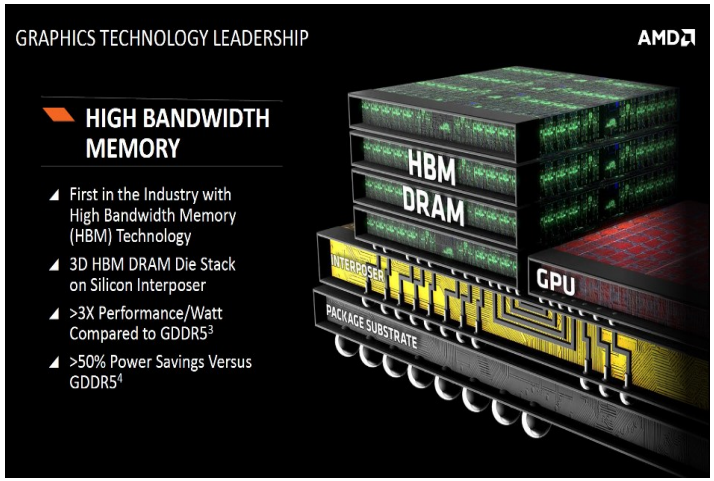


AMD reveals HBM-powered Radeon Fury graphics cards, new R300-series GPUs





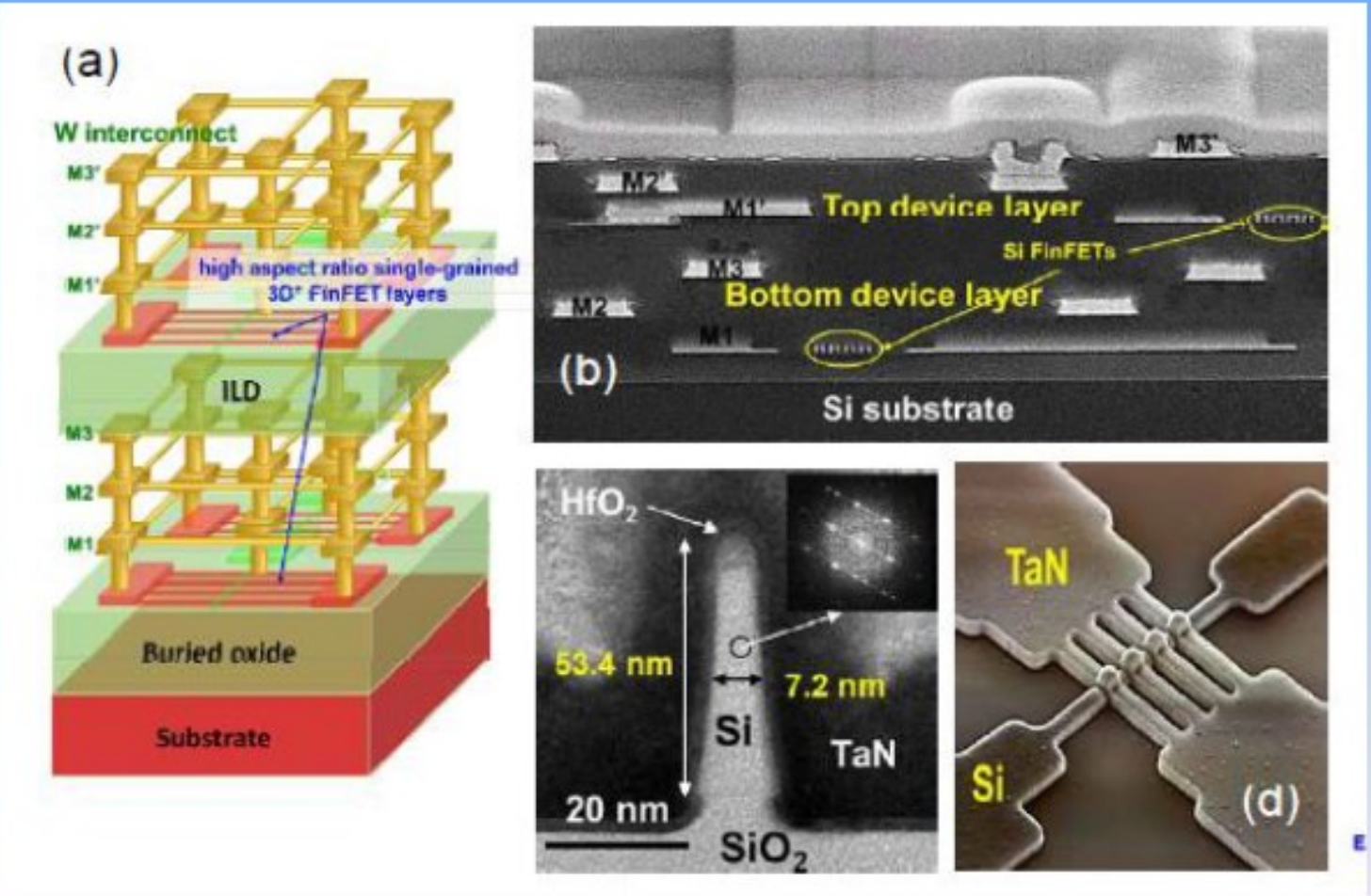




Fury graphics card : $649, June, 2015

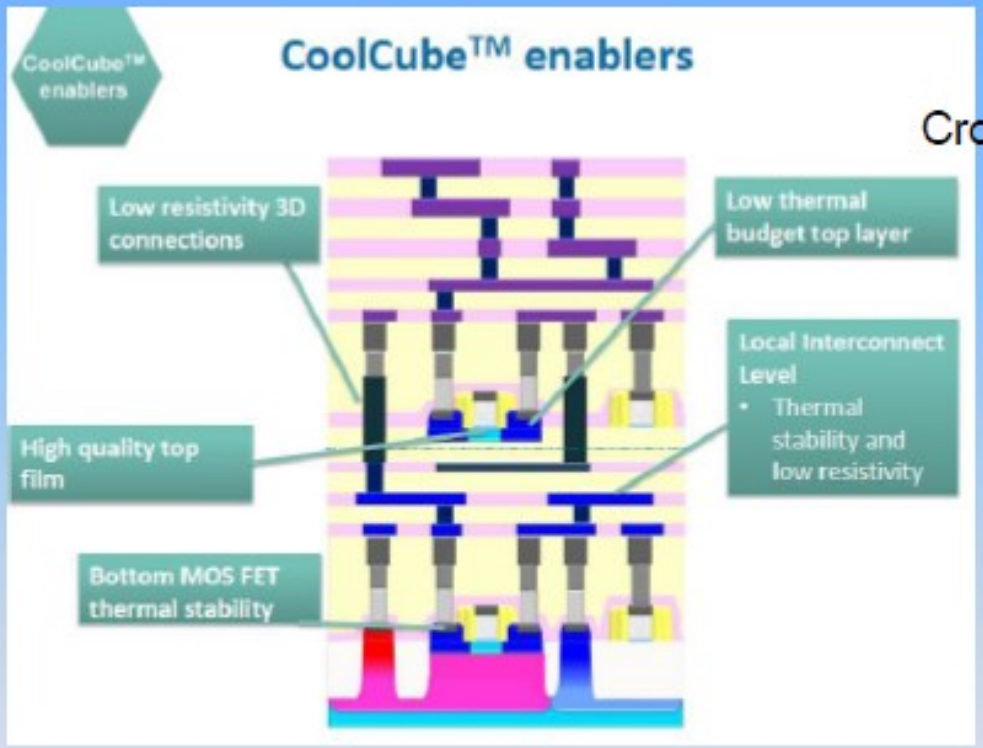
- ✓ *Memory Interface ; 4096bit*
- ✓ *Memory Bandwidth ; 512GB/s*

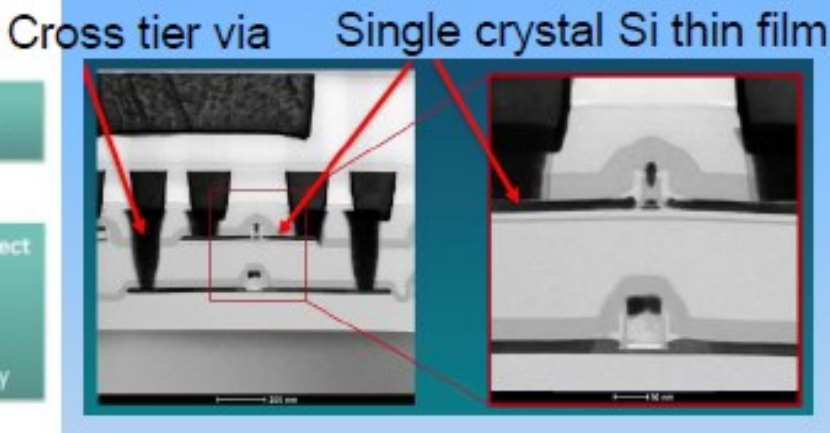
Monolithic 3D IC with FinFET Fabricated by Laser Anneal



Source: Chih-Chao Yang (NDL, Taiwan), IEDM2016

Monolithic 3D IC by Wafer Level Sequential Integration

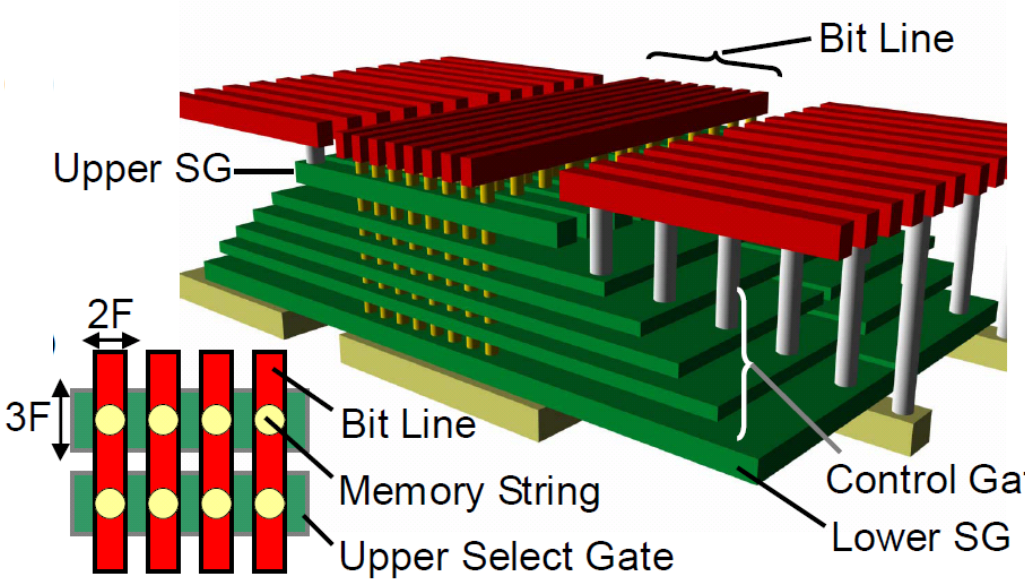


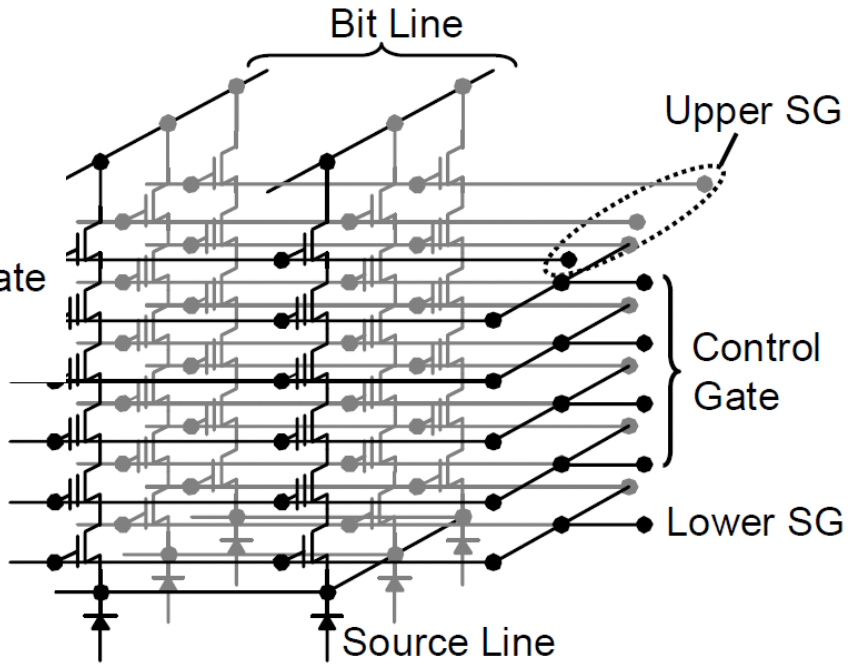


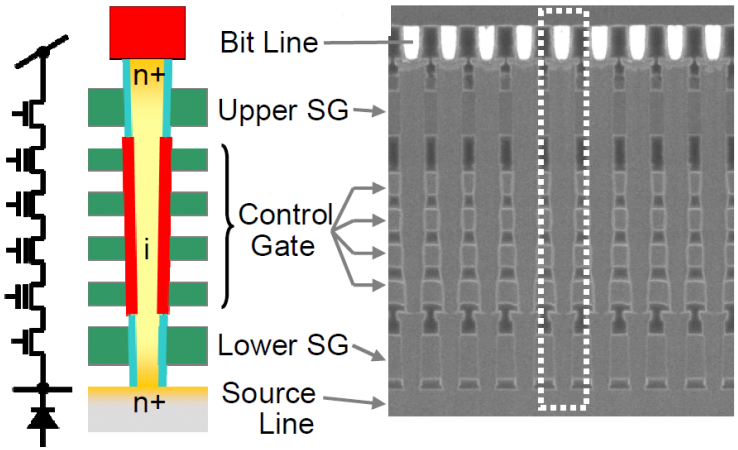
Source: H. Metras (Leti), 3D-ASIP2014

Monolithic 3D-IC with vertical TFT

Toshiba : Flash Memory

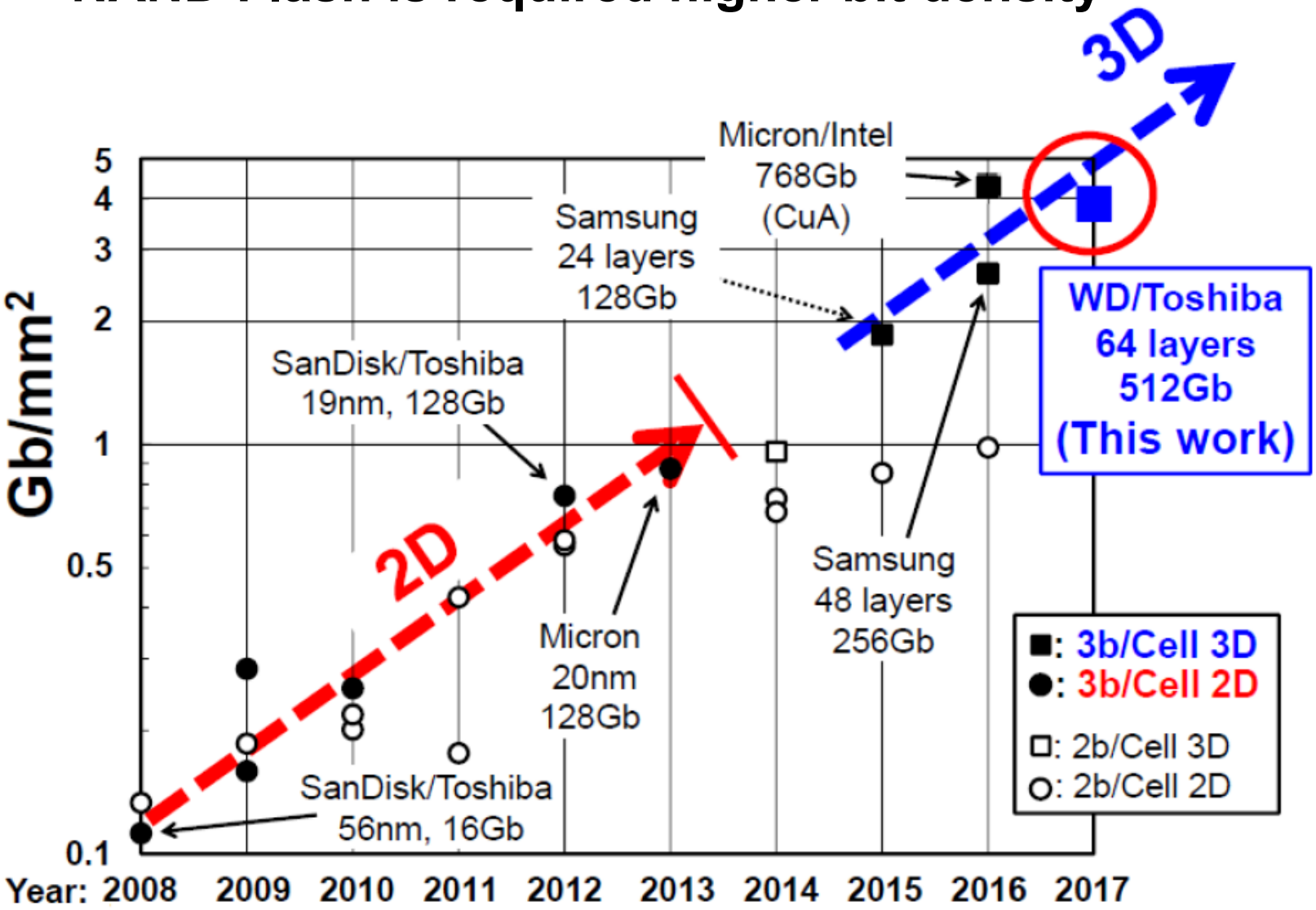






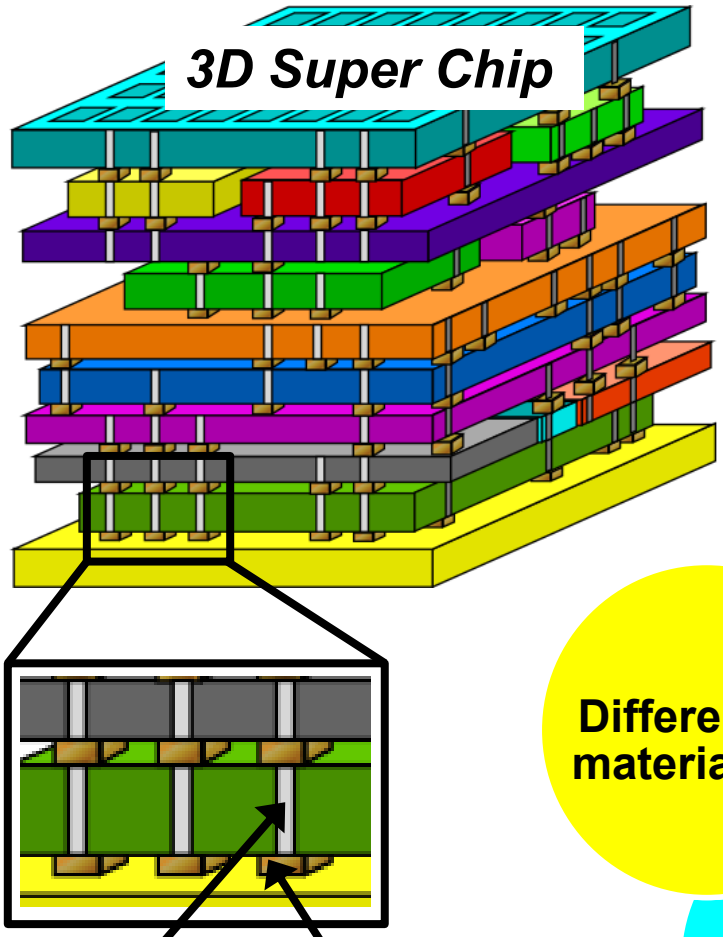
IEDM2007

NAND Flash is required higher bit density



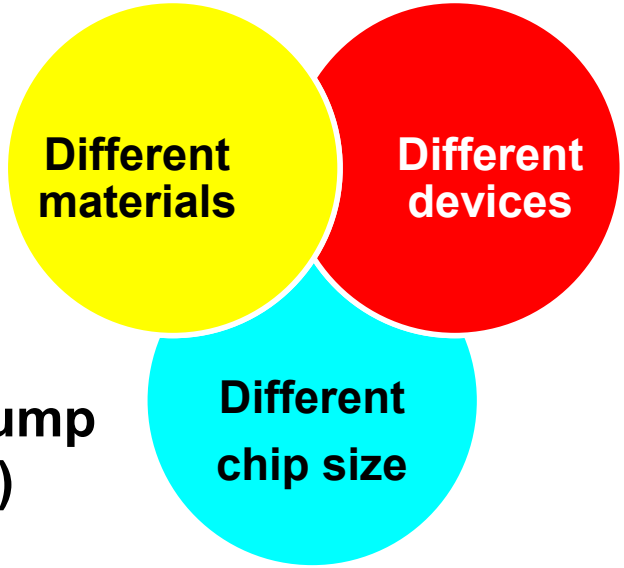
Source: R. Yamashita (Western Digital/Toshiba) ISSCC 2017

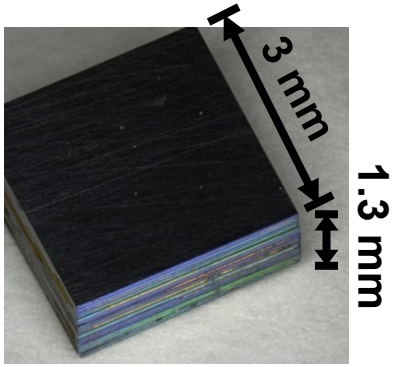
Highly Integrated Heterogeneous 3D Integrated System



MEMS chip
Sensor chip
CMOS RF-IC
MMIC
Power IC
Control IC
Logic LSI
Flash memory
DRAM
SRAM
Microprocessor

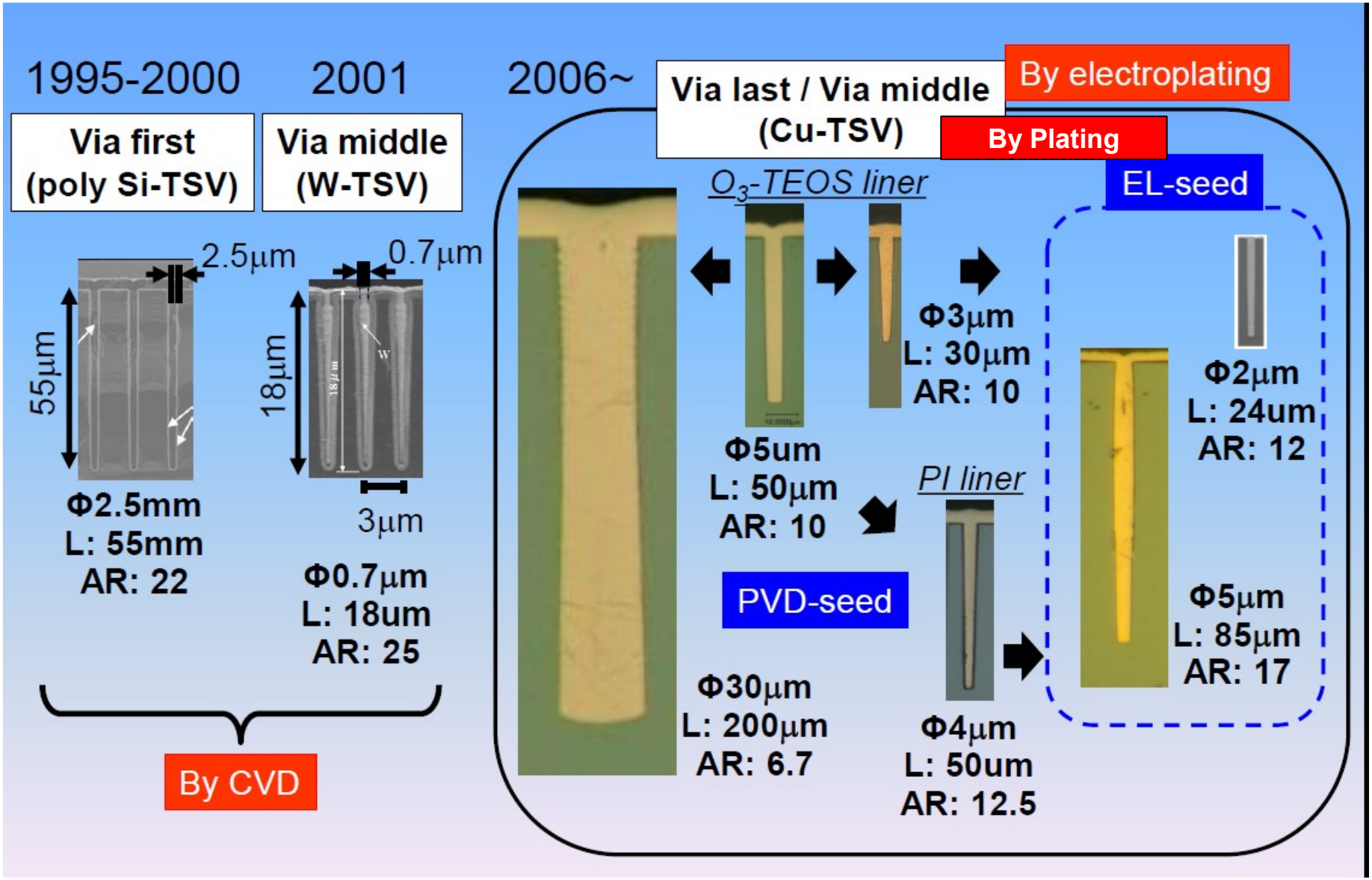
New chip stacking technologies are required



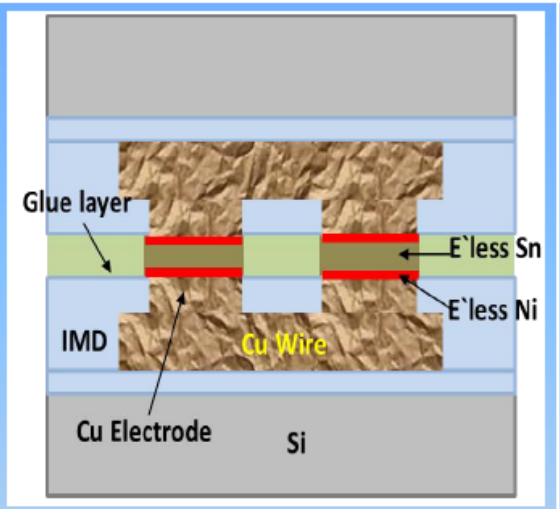
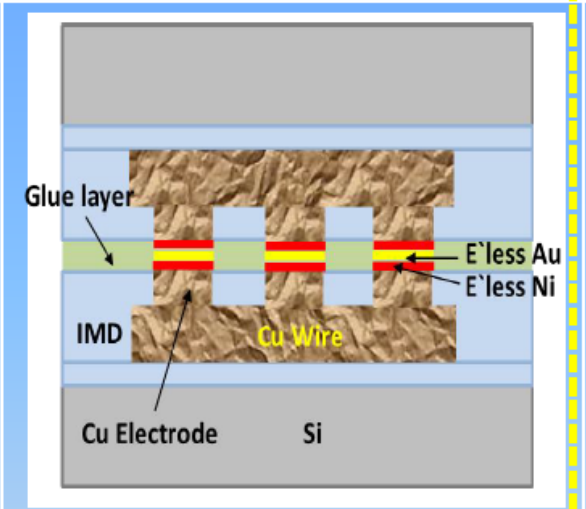
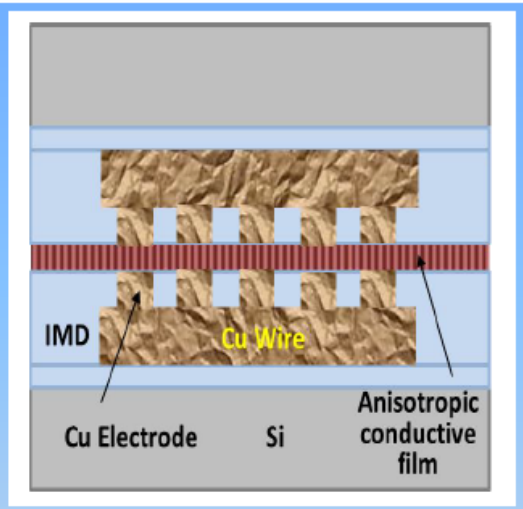


38-layer chip stack

Fine Pitch TSV

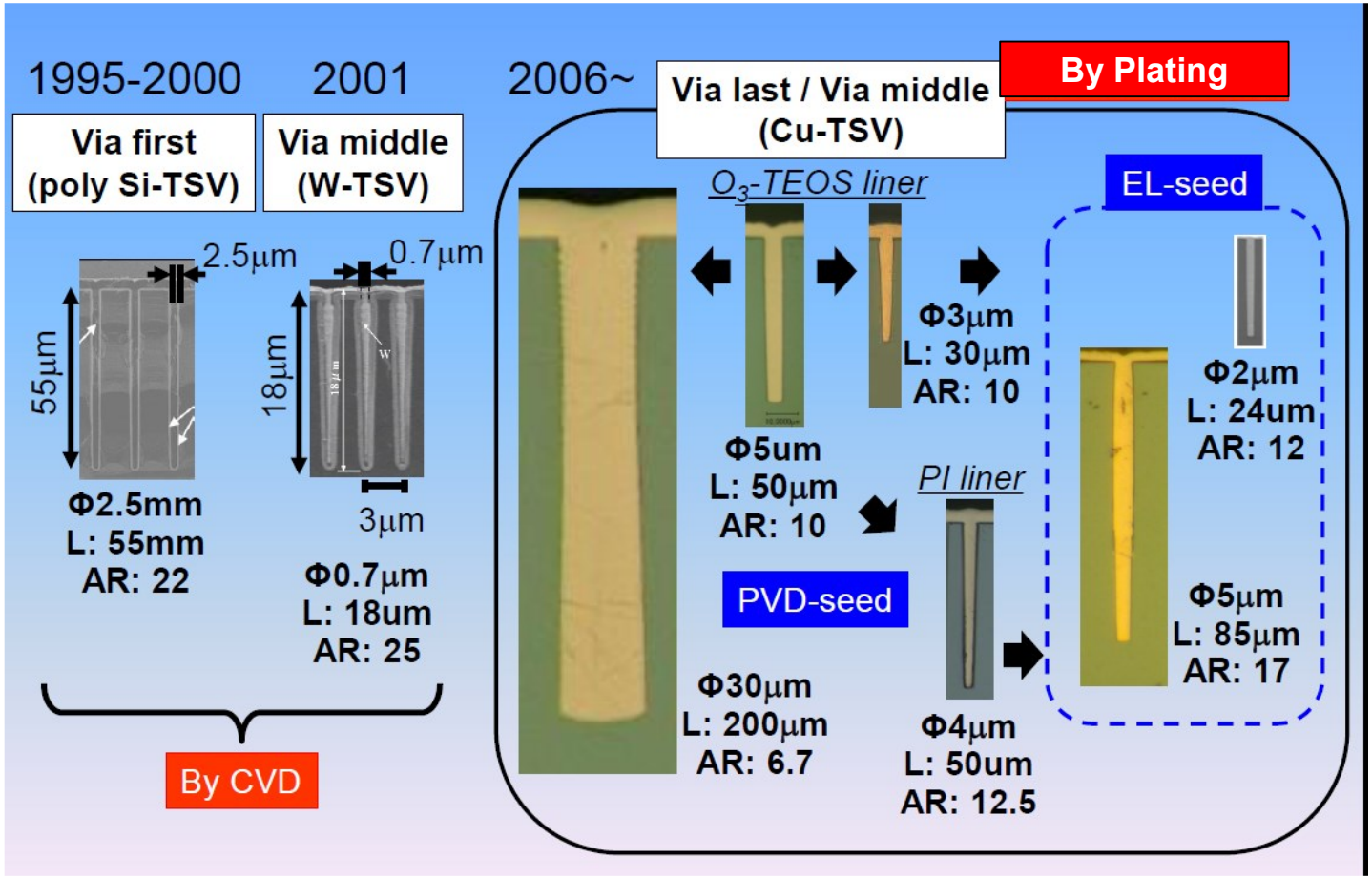


Novel Hybrid Bonding Features for Ultra-high Density 2.5D/3D Integration

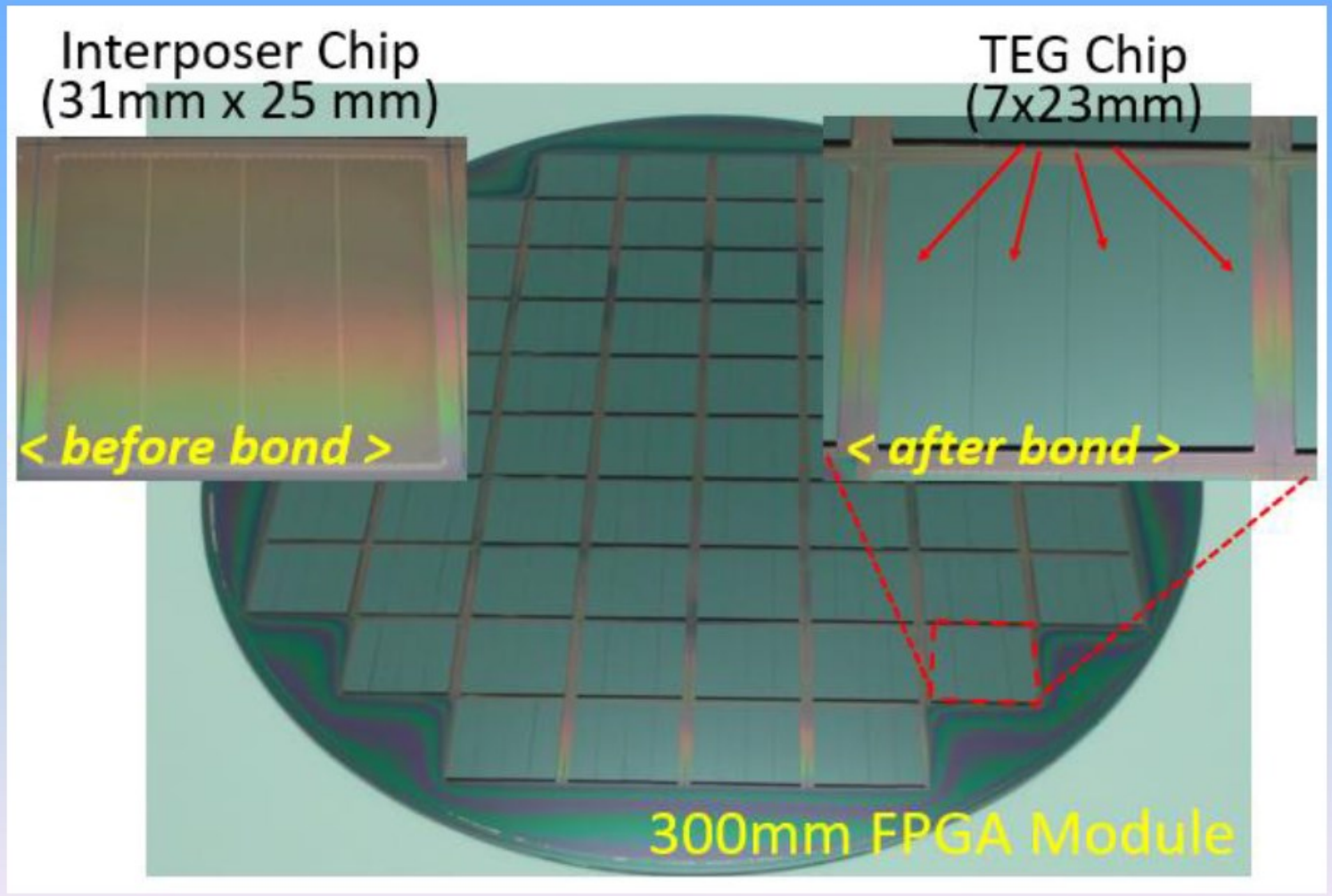
Gigascale	Terascale	Exascale
		
* Target Electrode - Size ; 3um, Pitch ; 6um - Density ; ~ million/die * Joining Structure - Electro-less thin Ni/Sn layers on extruded Cu electrode - Thin glue layer (below 1umt) containing flux composition	* Target Electrode - Size ; 2um, Pitch ; 4um - Density ; ~ Ten millions/die * Joining Structure - Electro-less thin Ni/Au layers on extruded Cu electrode - Thin glue layer (below 1umt) w/o flux composition	* Target Electrode - Size ; < 1um, Pitch ; < 2um - Density ; > Hundred millions/die * Joining Structure - Extruded Cu electrode - Anisotropic conductive film compose of ultra-density nano-Cu filaments

- *Novel hybrid bonding technology with unique features of (1) shallow extruded electrode (bump-less), (2) thin metal capping layers, and (3) unique adhesive layer for ultra-high density 2.5D/3D integration by avoiding critical issues of current standard hybrid bonding technology*

Fine Pitch TSV



Photograph of 300mm FPGA TEG Modules Fabricated by Multichip-to-Wafer 3D Stacking



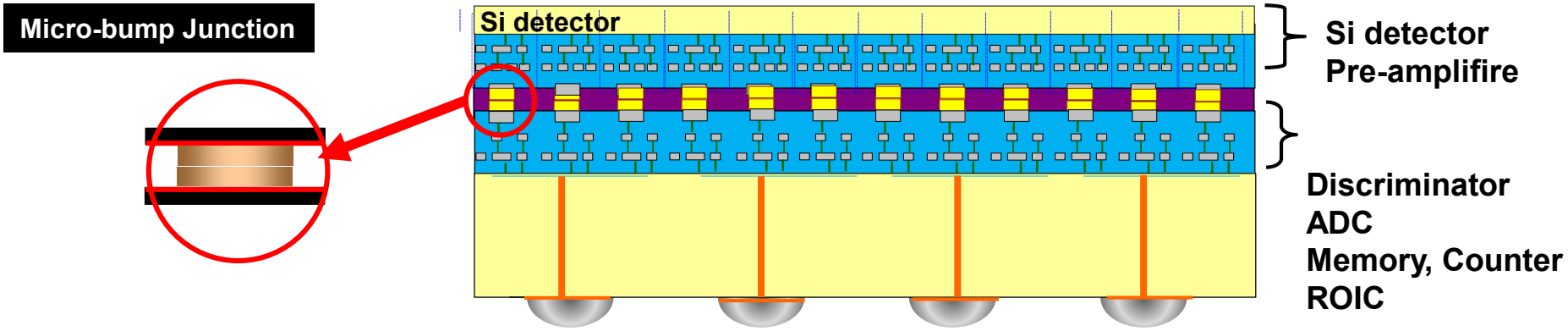
Contents

1. Background
   - -Target device
   - -Previous work
2. Au cone bump using NpD method
3. Cylinder Bump for fragile semiconductor material
4. 3D Cost reduction approach
5. Summary

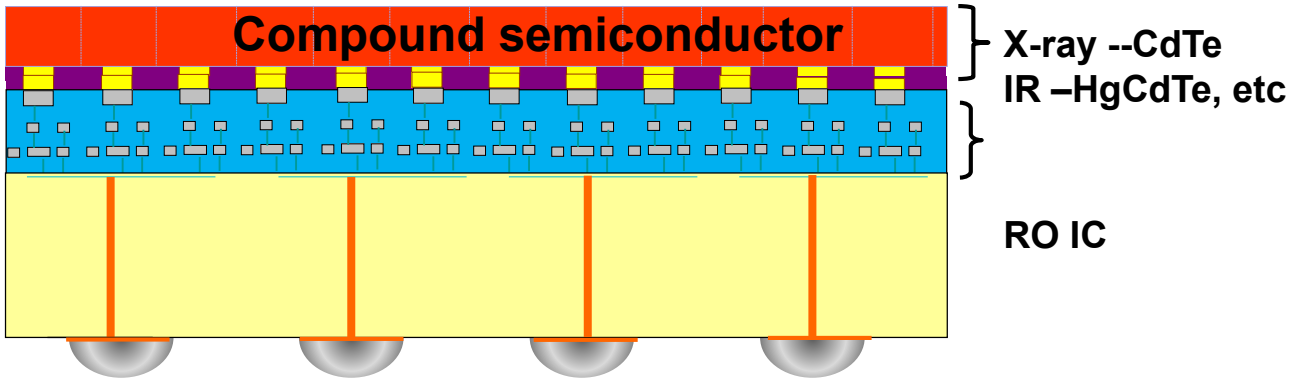
NpD: Nano-particle deposition

Target device

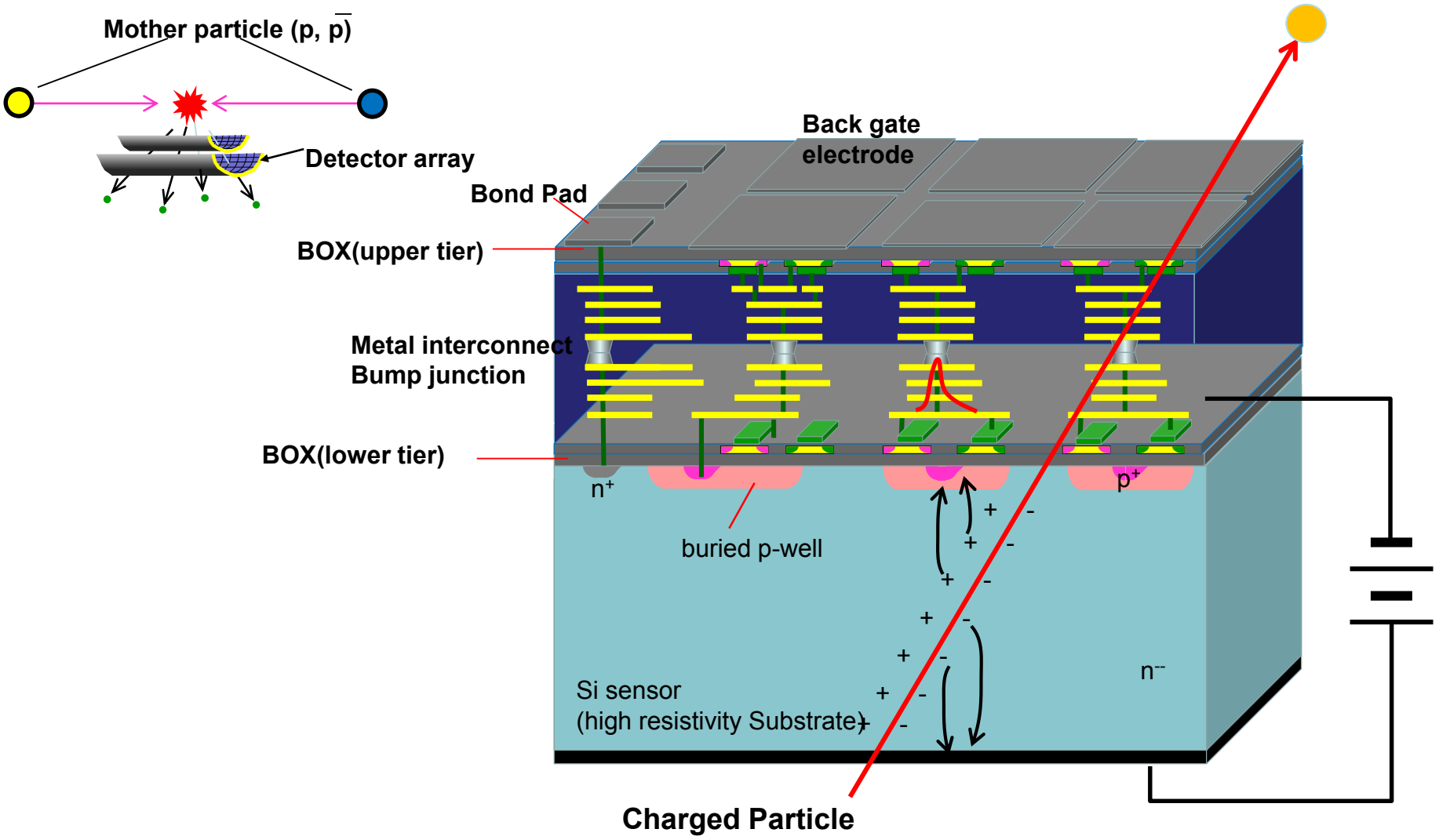
3D Stacked Pixel Detector



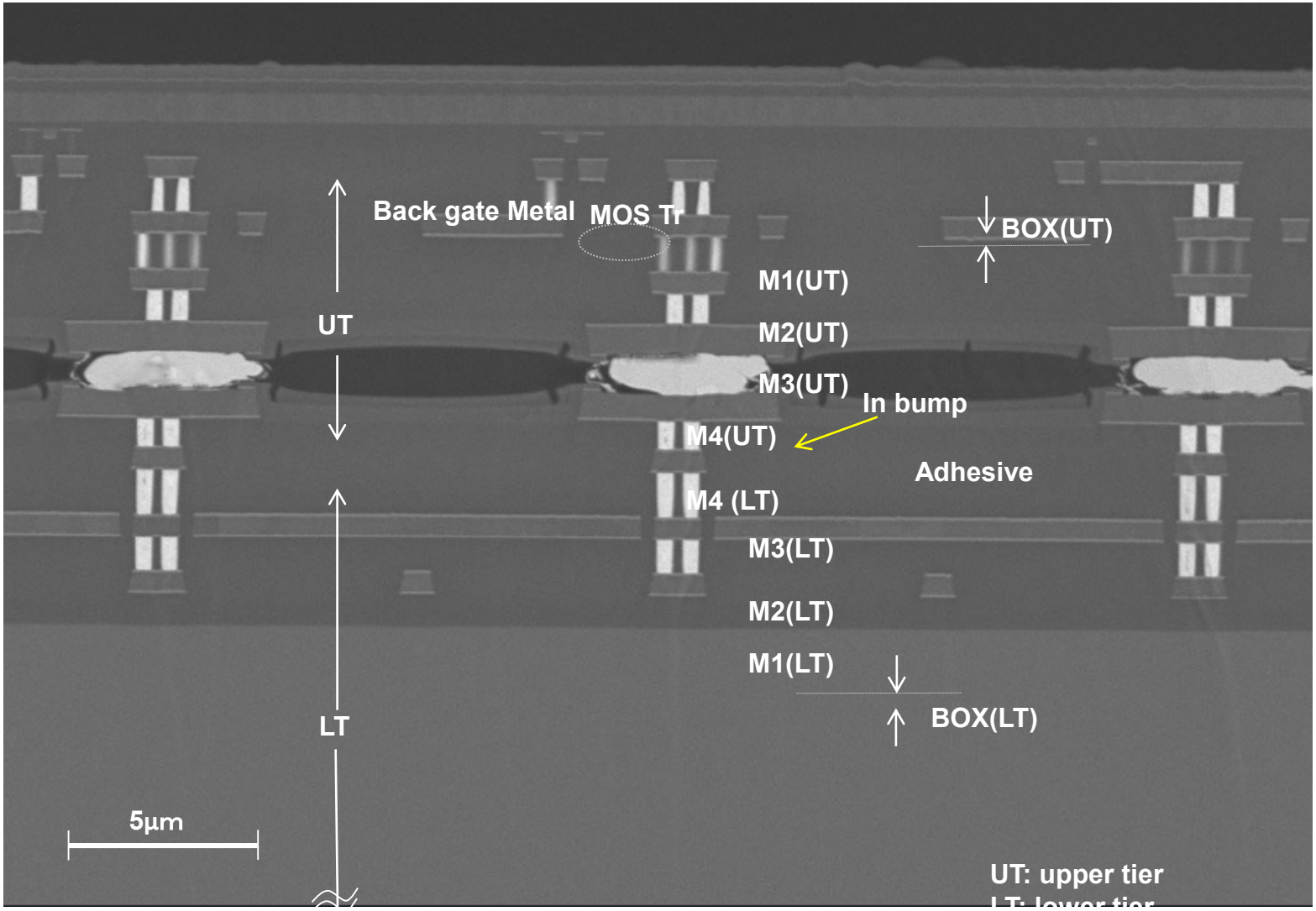
3D heterogeneous stacked X-ray / IR pixel sensor



Stacked SOI Pixel detector

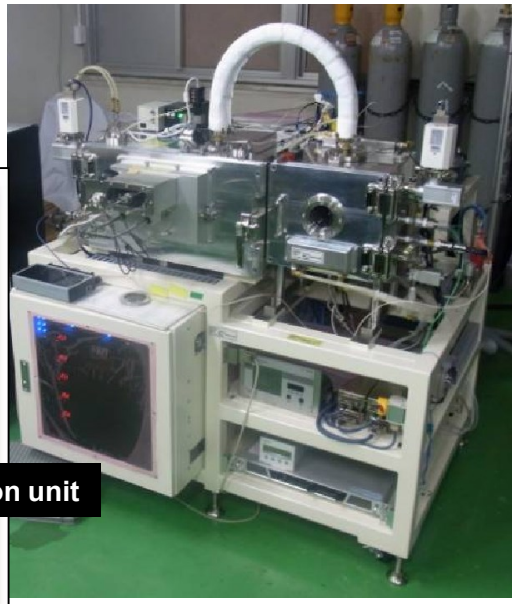


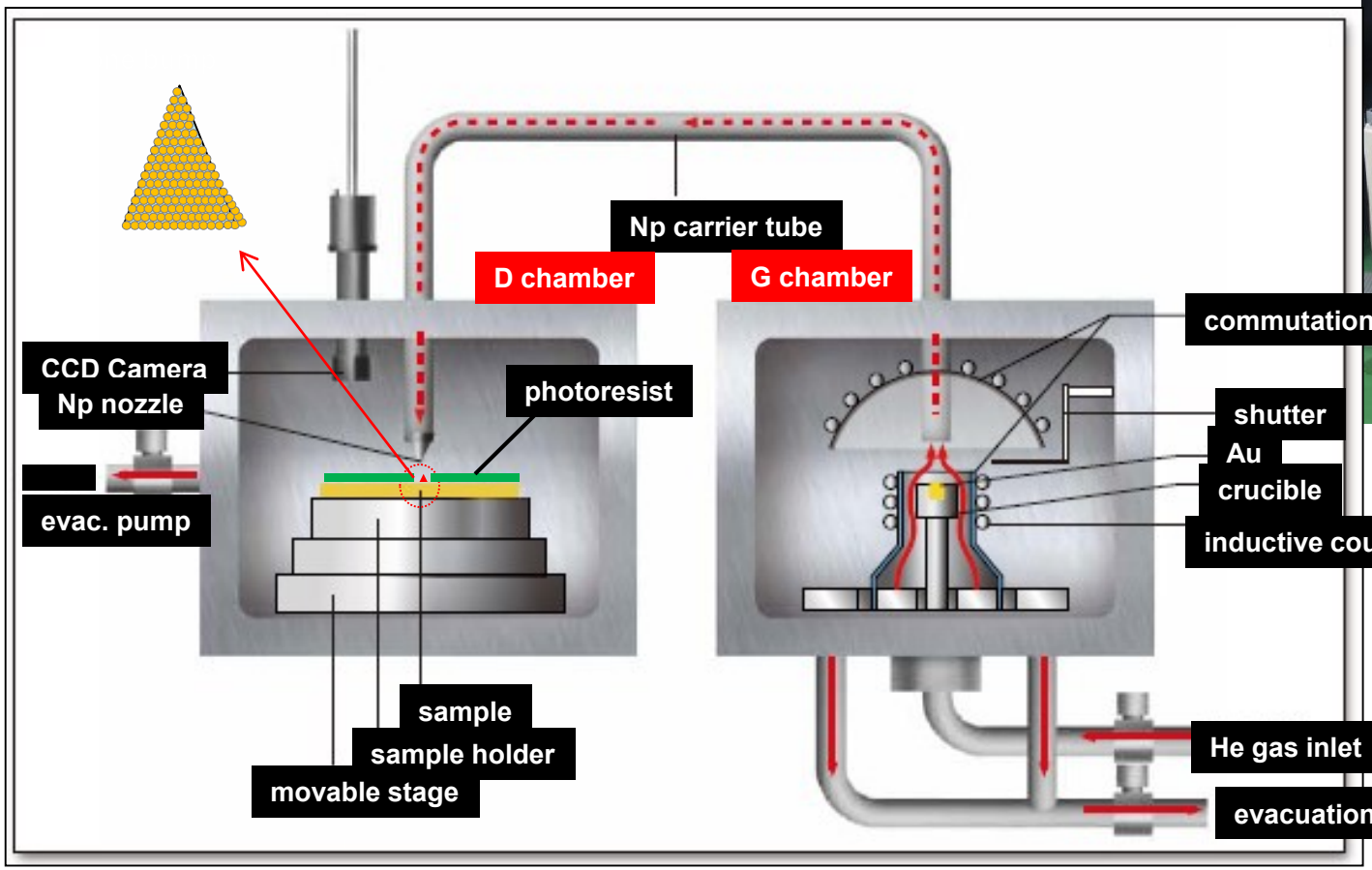
Pixel array using Indium micro-bump



2. Au cone bump using NpD

Nano-particle Deposition (NpD) System



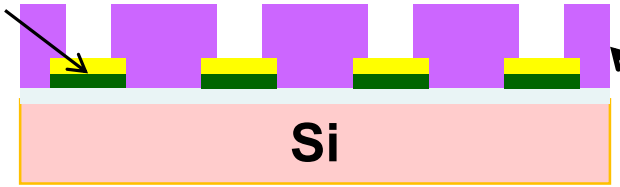


Courtesy of Mixnus Fine Engineering Co., Ltd

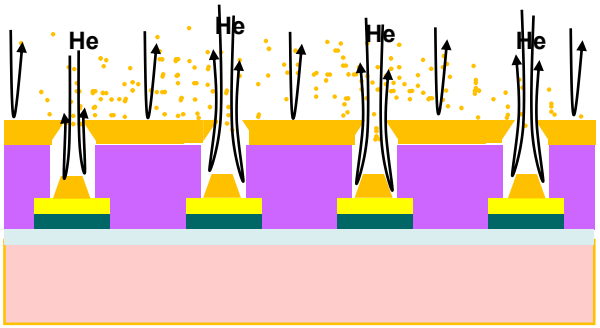
Au Cone bump formation

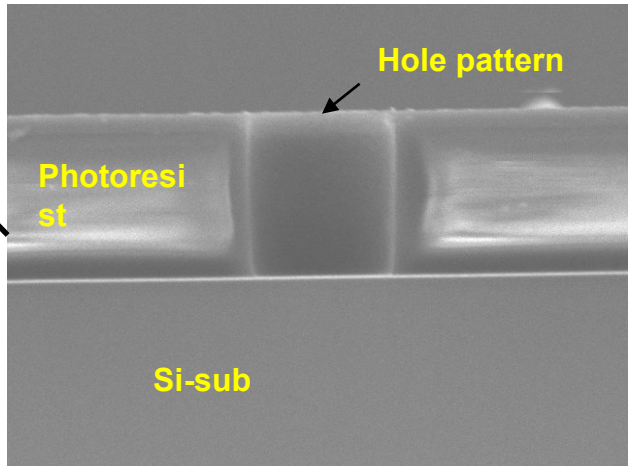
Au/barrier metal/SiO_2

Bump litho.

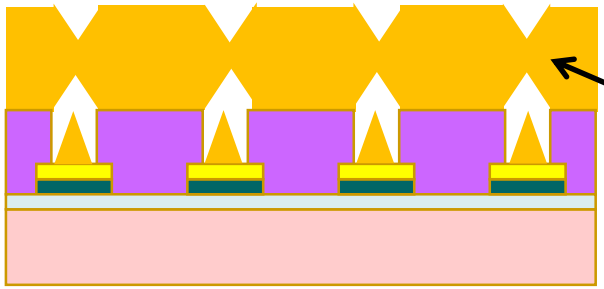


NpD

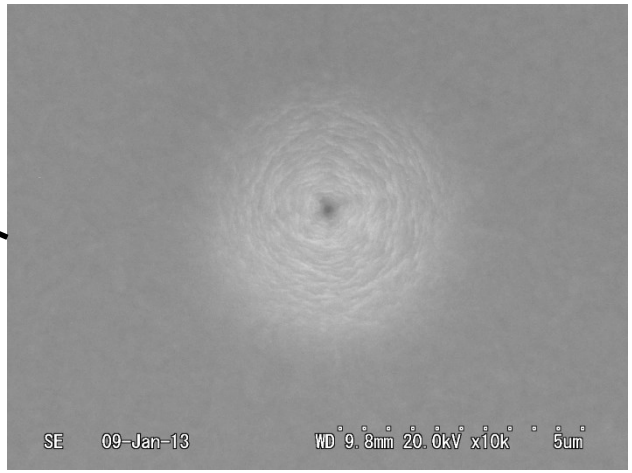




Close bump hole



After resist lift-off



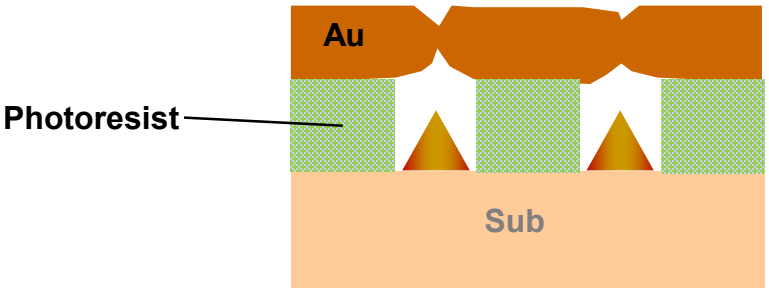
Top view after deposition

Pros & cons of Au cone bump

Pros

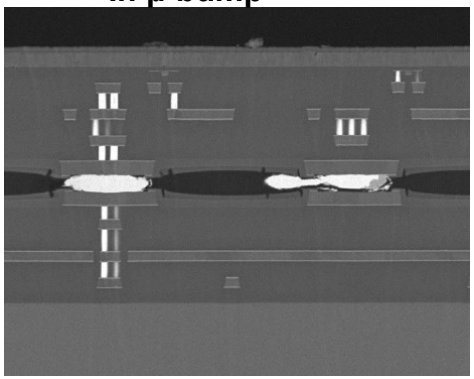
- good scalability

-bump size and height are only determined by lithography process

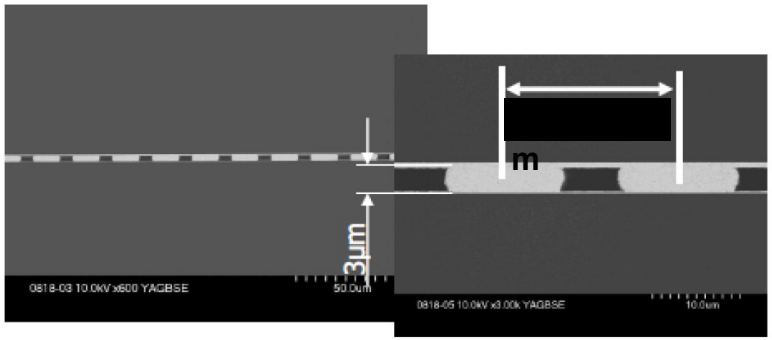


-no extrusion

In μ-bump



Au cone bump

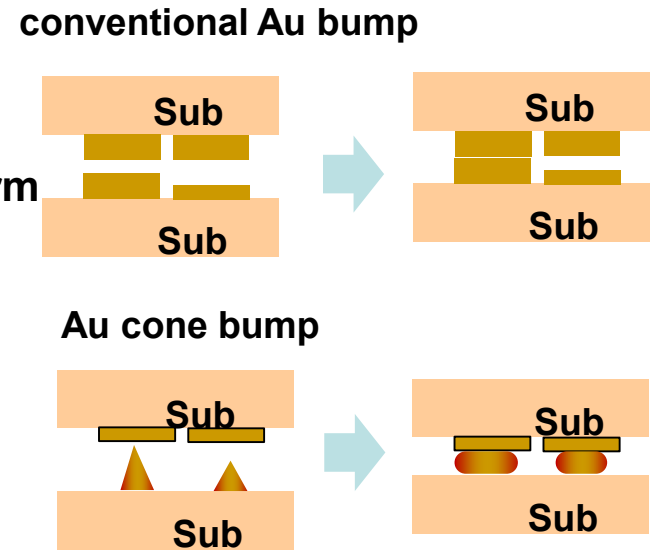


Pros & cons of Au cone bump

Pros（Continue)

- large bonding margin

NpD Au cone bump ➔ easy to deform



- low temperature process

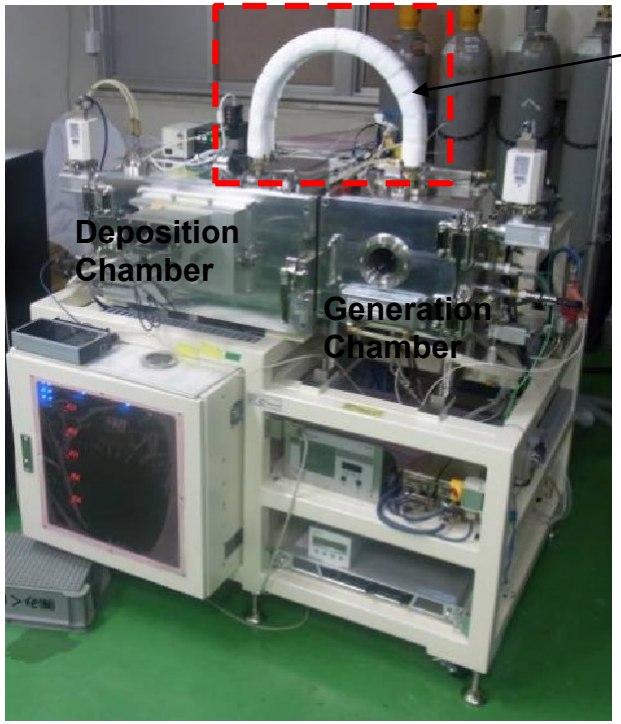
less than 200 ℃ ➔ 150℃ (present)
➔ 120℃ (Target)

Pros & cons of Au cone bump

Cons

- low throughput Current process time for 5mm x 5mm chip is around 1hour

→ An improvement of deposition speed is now in progress



Prototype NpD machine

Nano particle transport tube

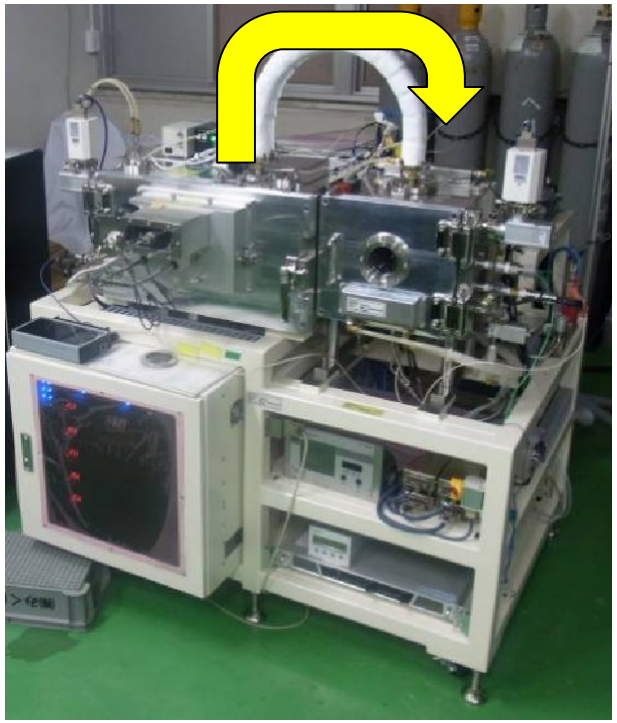
Deposit Np on the inside wall of the tube

Pros & cons of Au cone bump

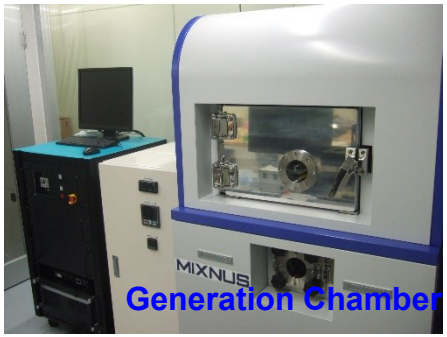
Cons

- low throughput Current process time for 5mm x 5mm chip is around 1hour

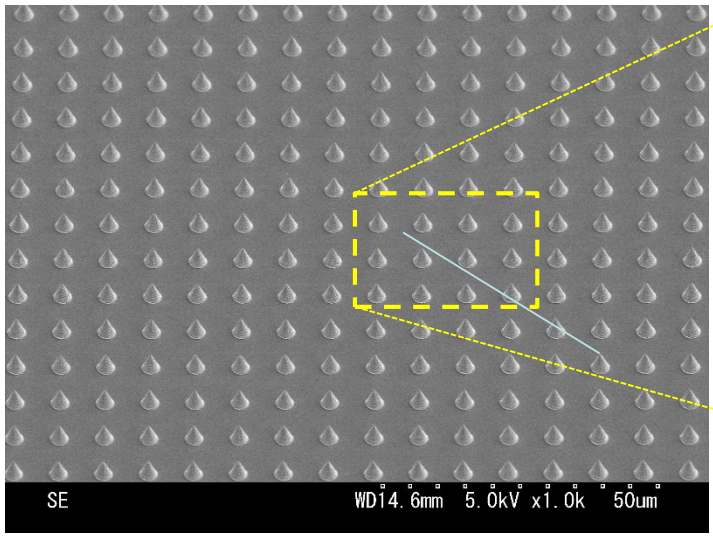
→ An improvement of deposition speed is now in progress

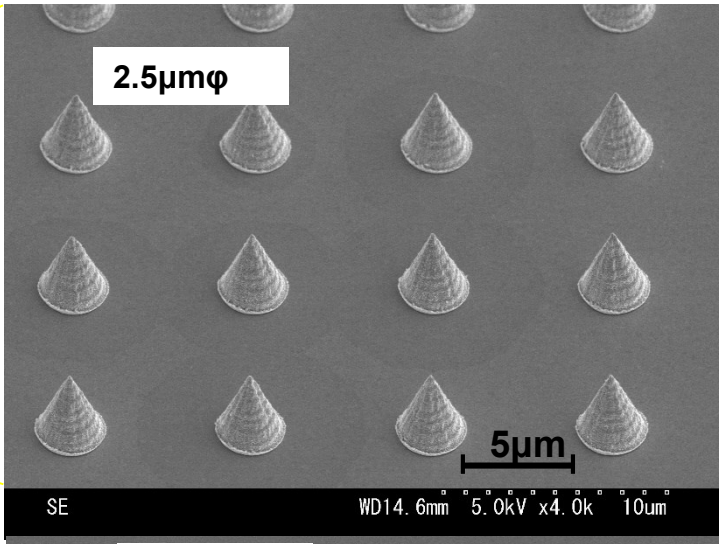


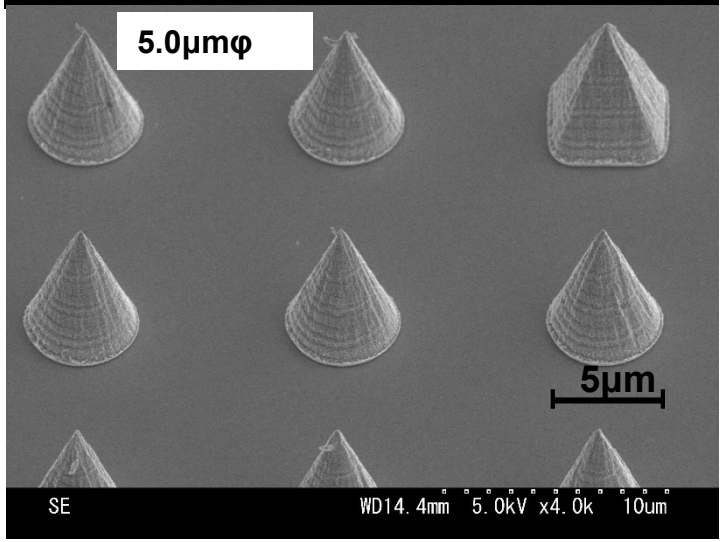
Prototype NpD machine



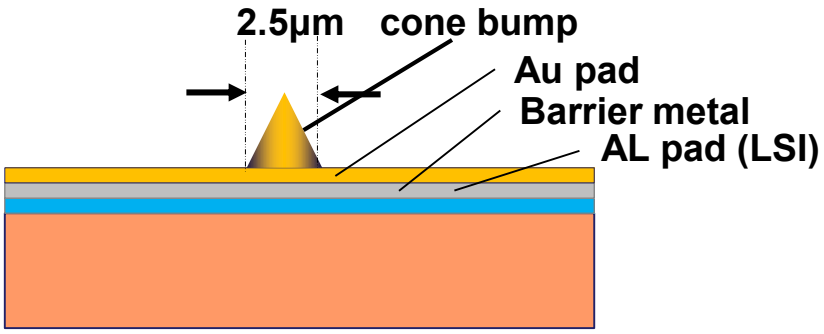
2.5/5.0μmφ Au Cone Bump







TEG cross section



Process flow for SOI Pixel detector(1)

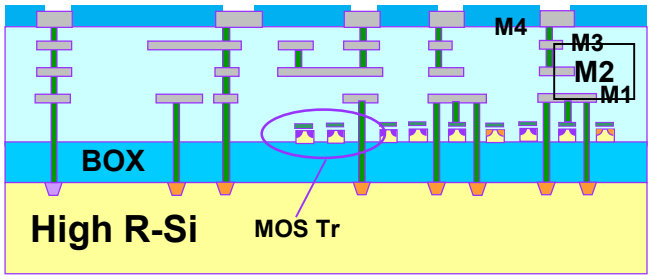
< Lower Tier >

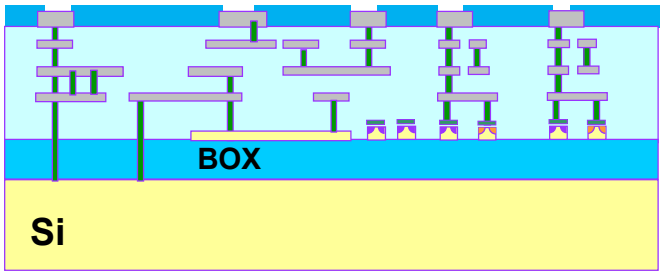
< Upper Tier >

(a) Start with FD-SOI device wafer

Active Si~50 nm
BOX:200 nm

**FD: Fully Depleted*

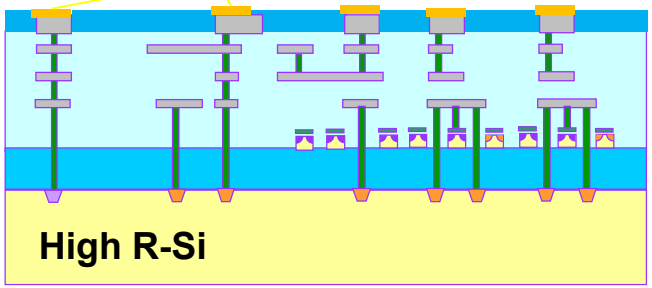


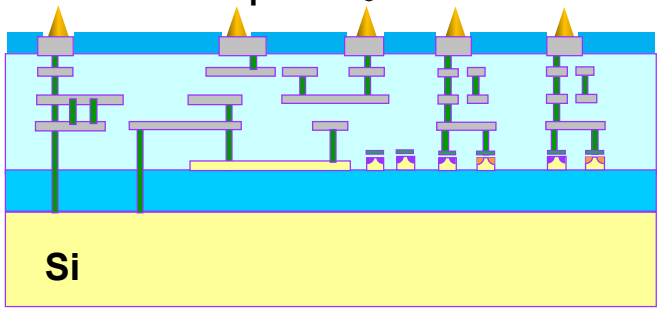


bump-landing pad

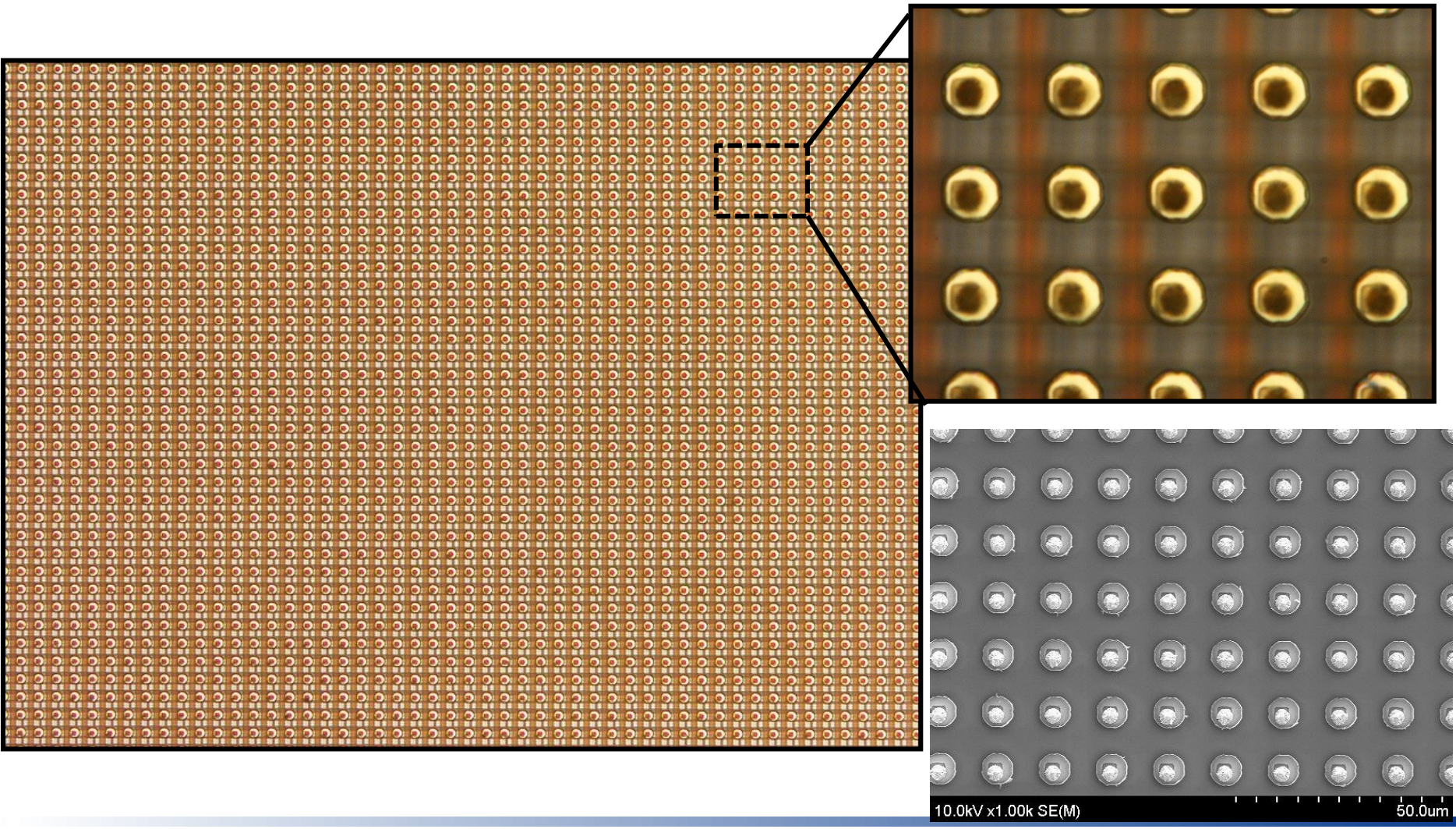
cone-bump

(b) cone bump/ landing-pad forming





After cone bump formation (@ pixel array area)



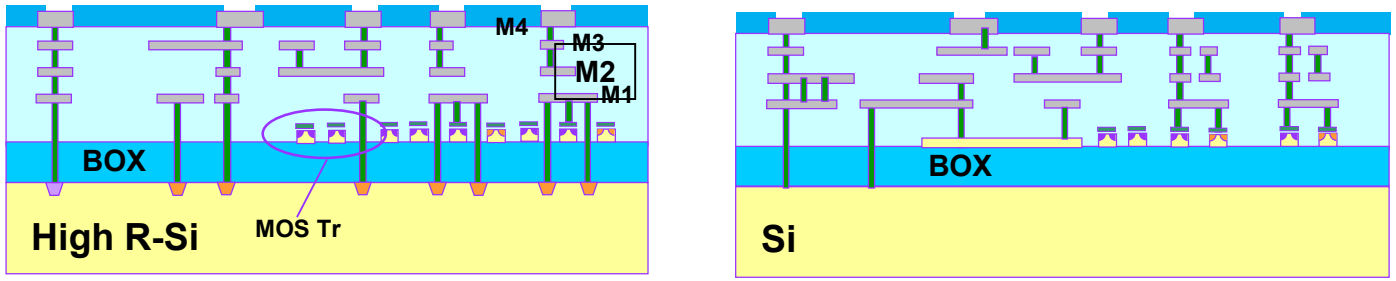
Process flow for SOI Pixel detector(2)

< Lower Tier > < Upper Tier >

(a) Start with FD-SOI device wafer

Active Si~50 nm
BOX:200 nm

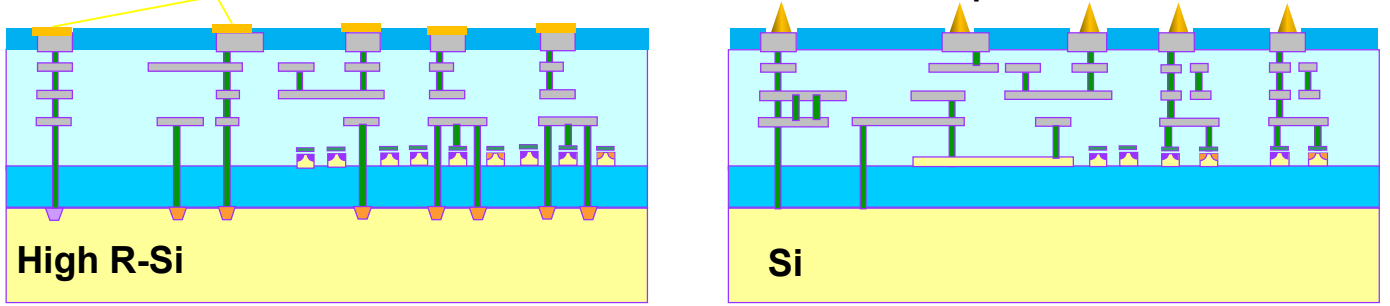
**FD: Fully Depleted*



bump-landing pad

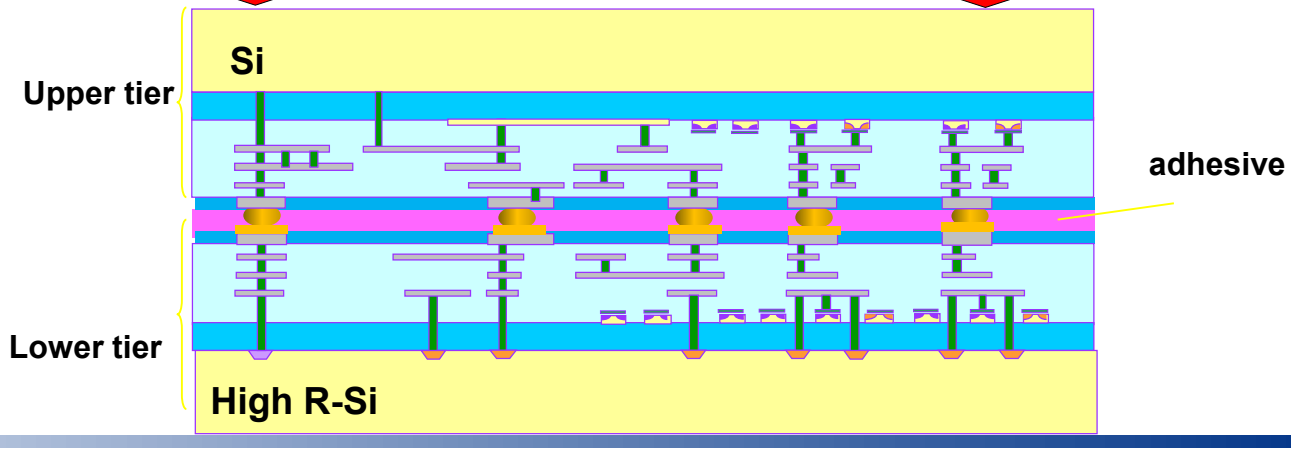
cone-bump

(b) cone bump/ landing-pad forming



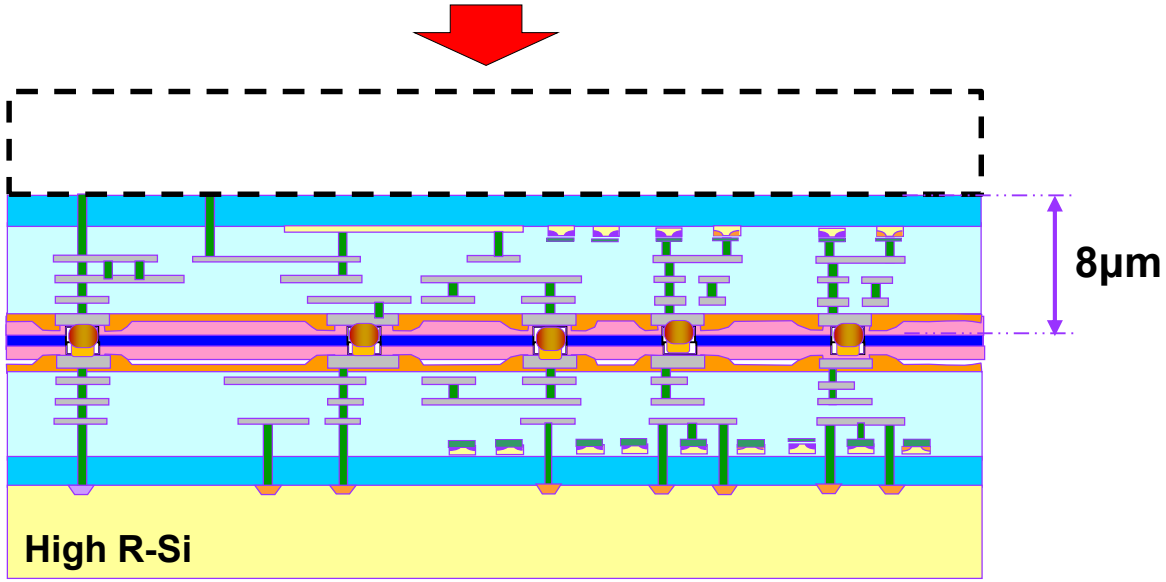
(c) Chip bonding

- face to face infrared alignment
- bonding (<200℃)
-Adhesive injection

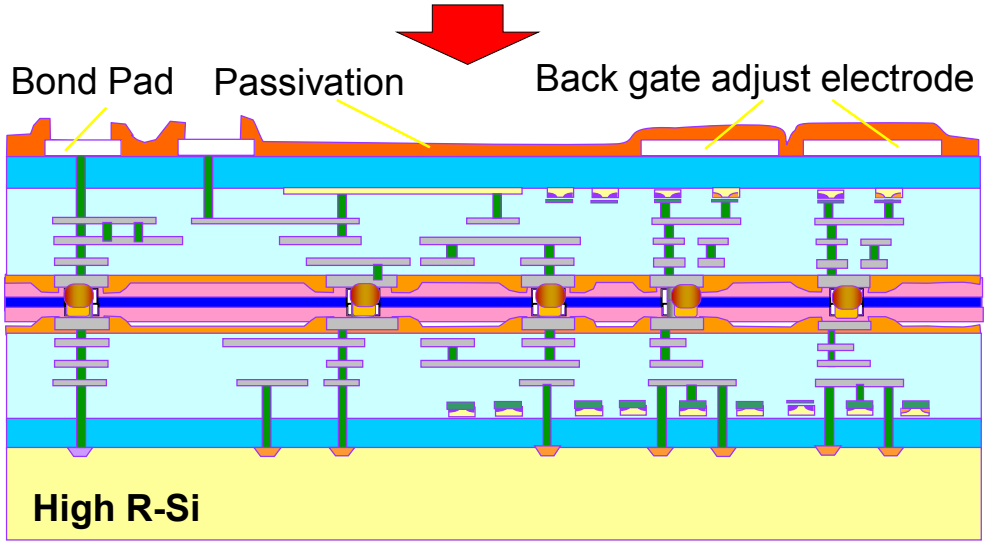


Process flow for SOI Pixel detector(2)

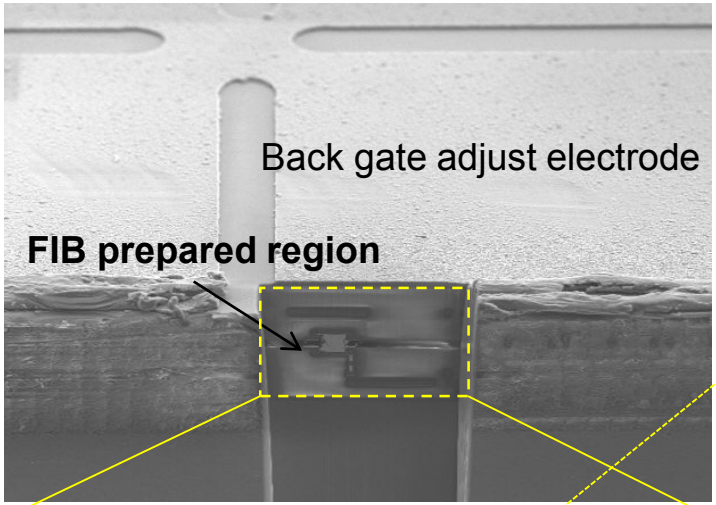
(d) Bulk-Si removal

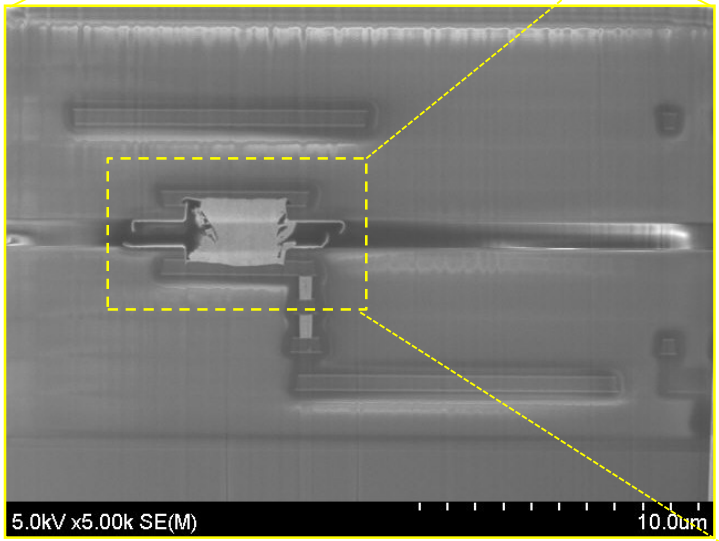


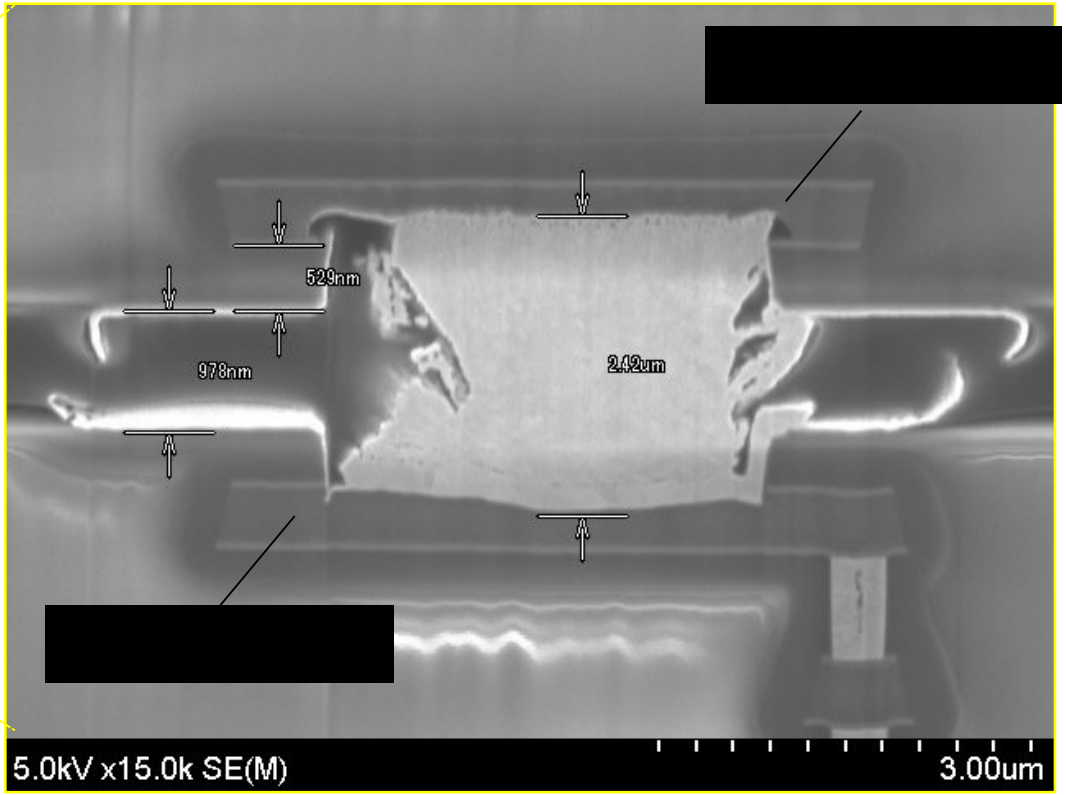
(e) Pad patterning and passivation



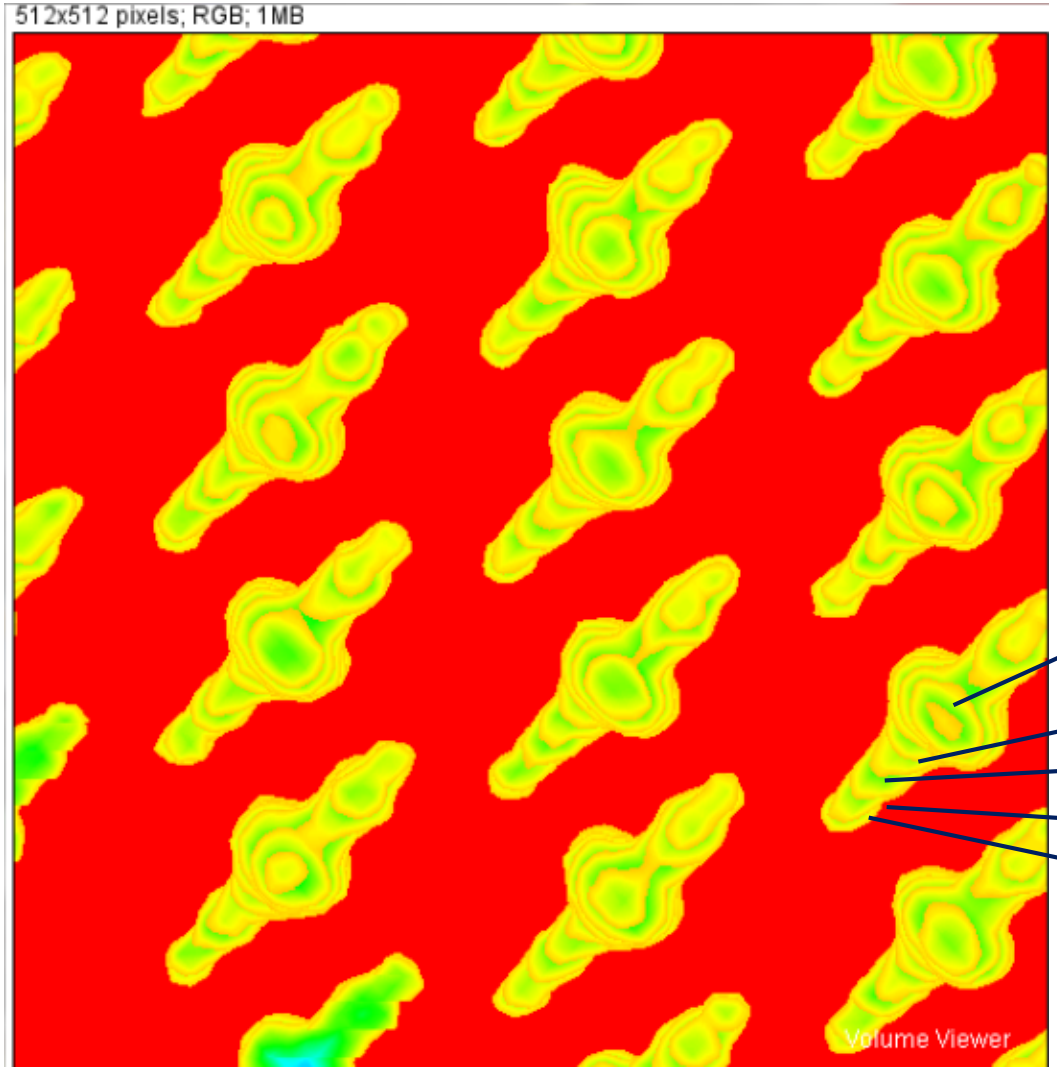
Cross section of Au cone bump junction

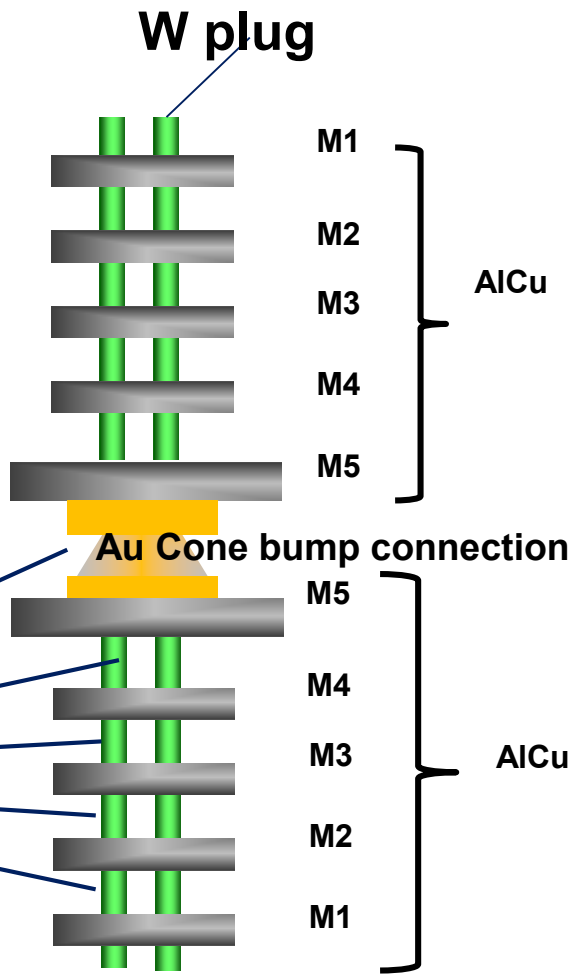




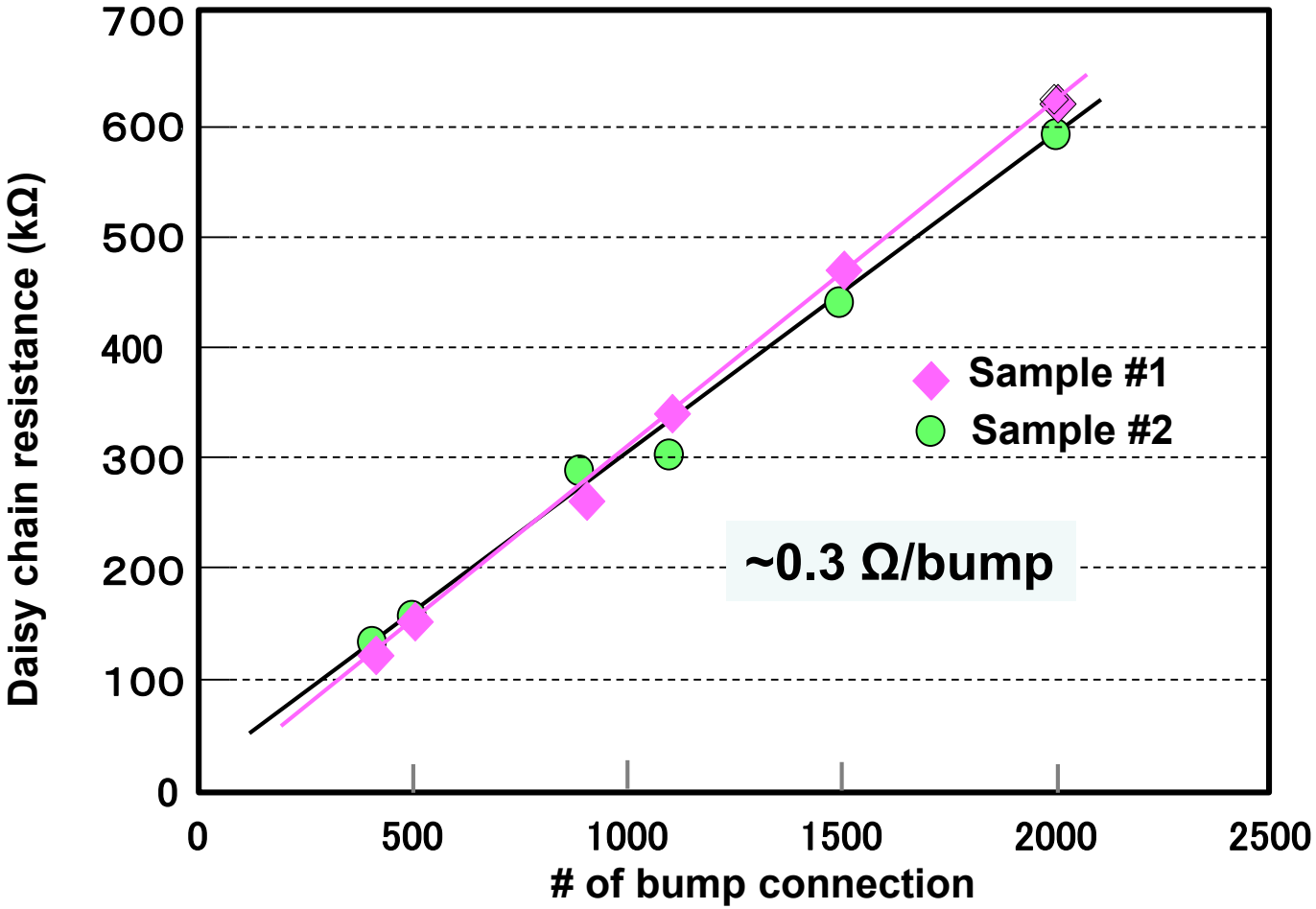


X-ray CT Image





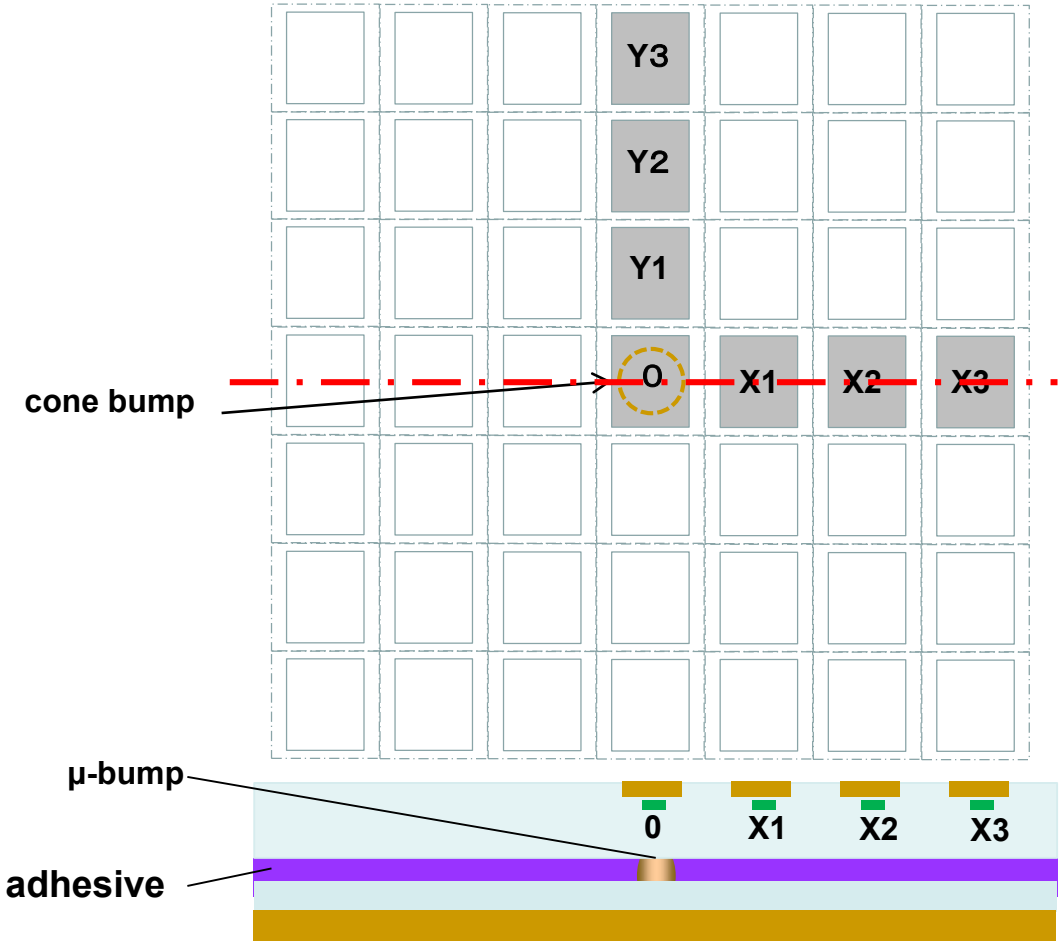
Bump resistance

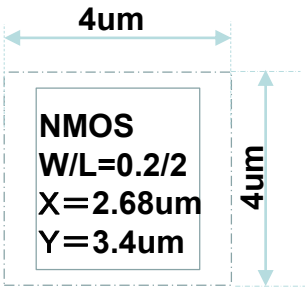


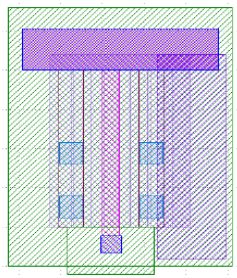
Stress evaluation

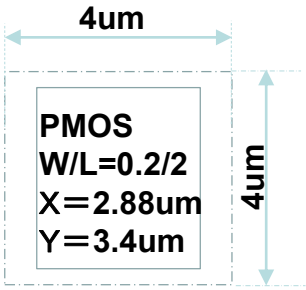
Evaluate the fluctuation of SOI-MOS Transistor caused by the stress of bump bonding

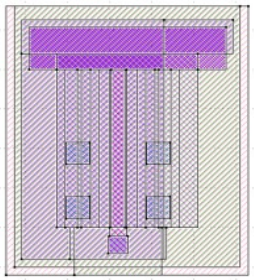
Device dimension N/P MOS Transistor W/L=2/0.2um



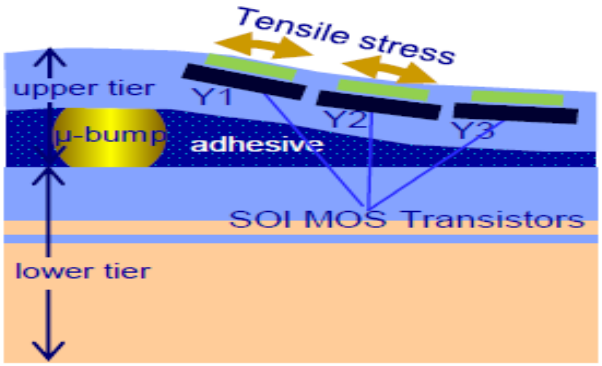


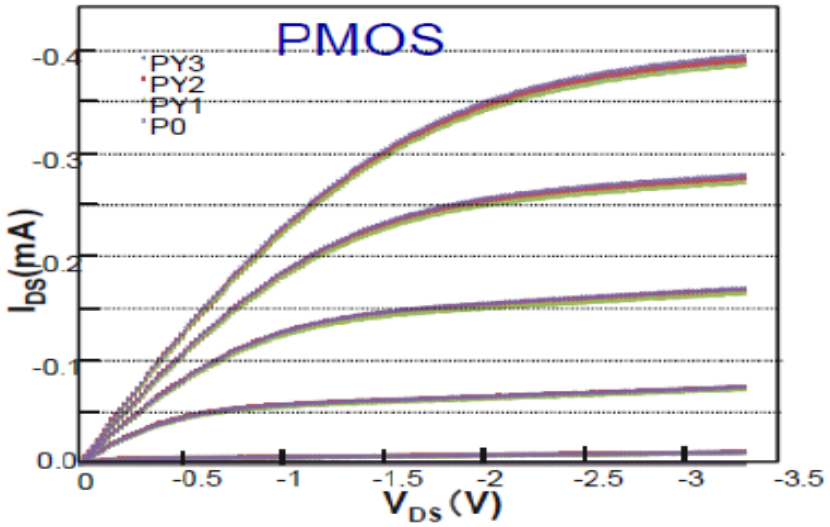


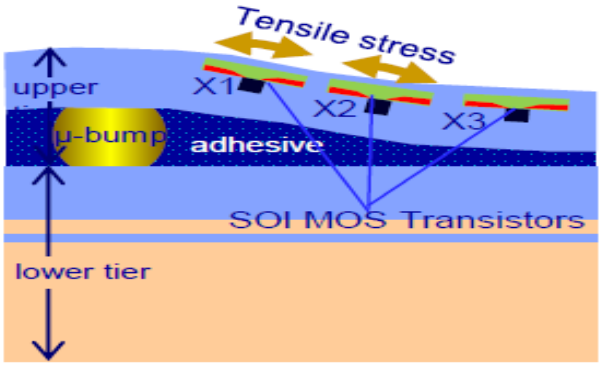


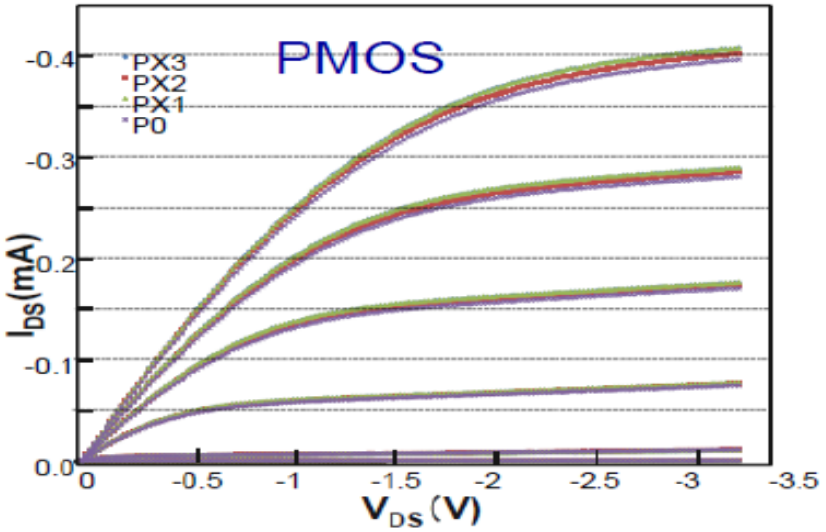


SOI PMOS- I_{DS} vs V_{DS} Characteristics

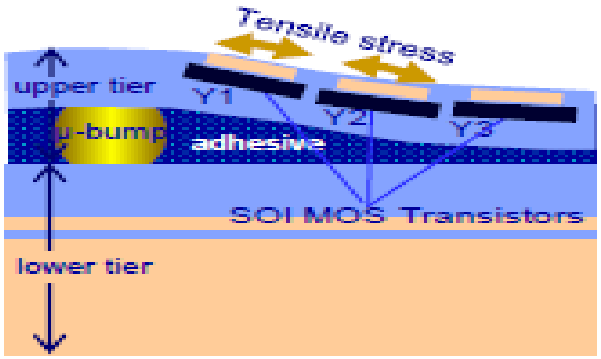


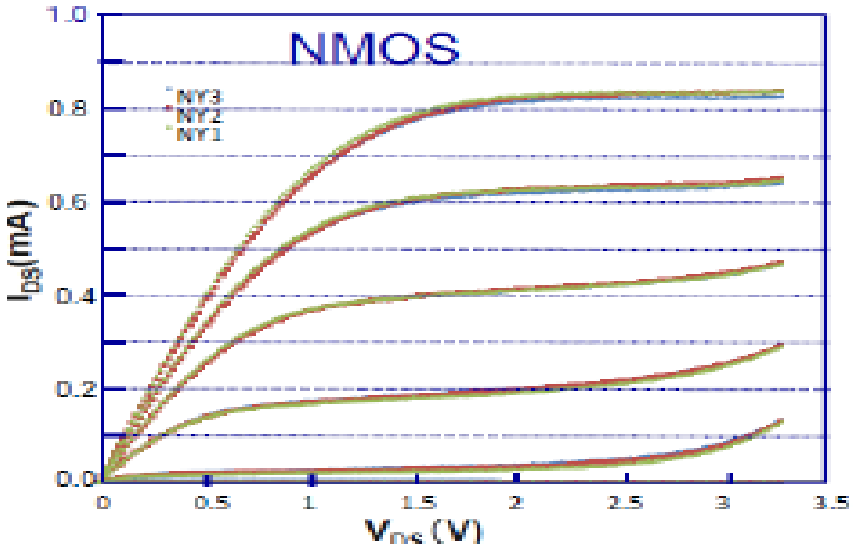


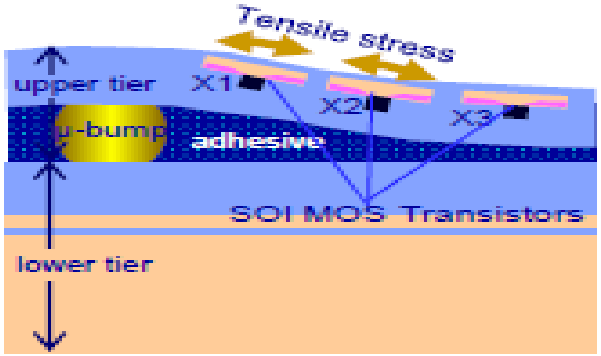


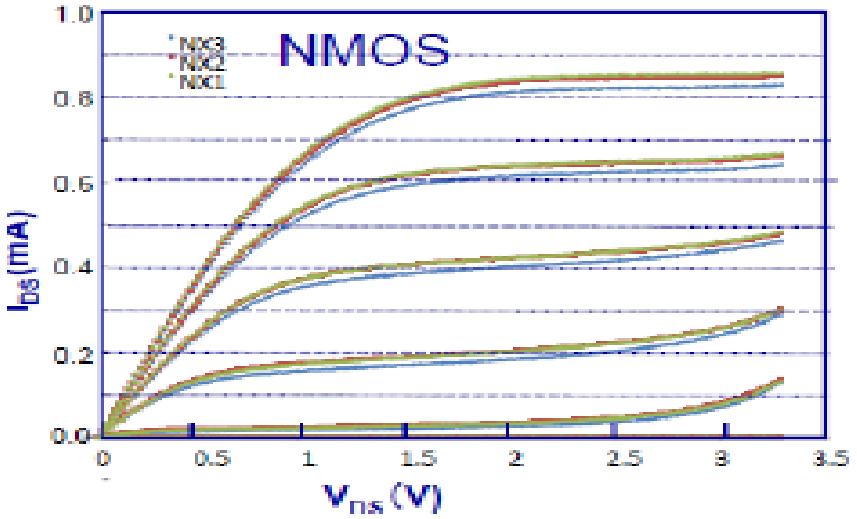


SOI-NMOS I_{DS} vs V_{DS} Characteristics

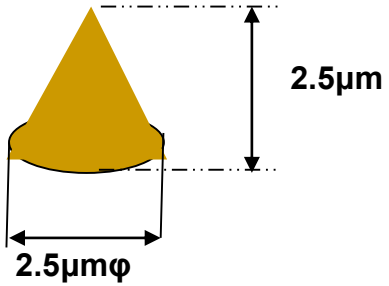




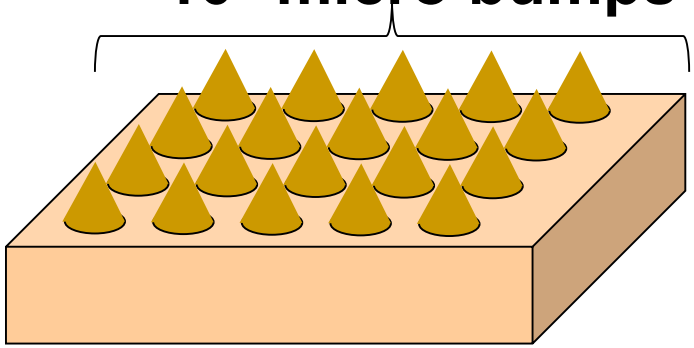




Material cost of Au bump

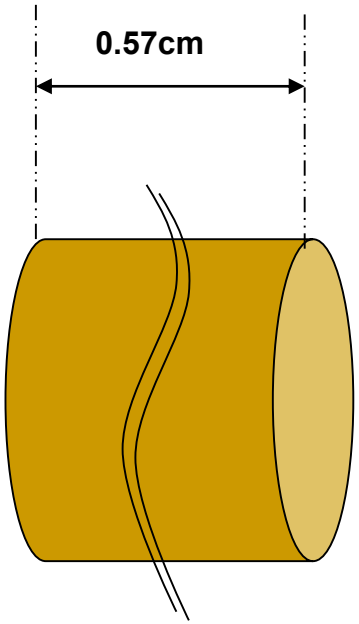


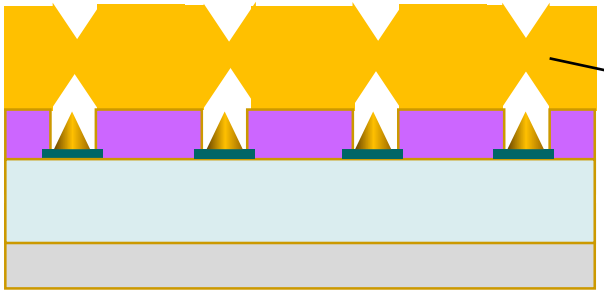
10^6 micro bumps



=

30μmφ
Au wire

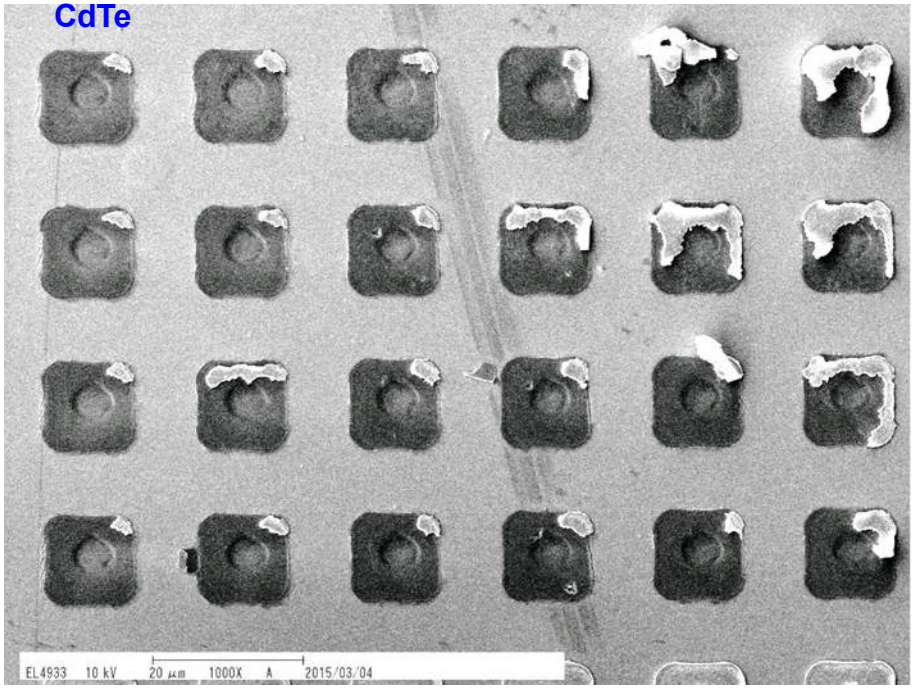


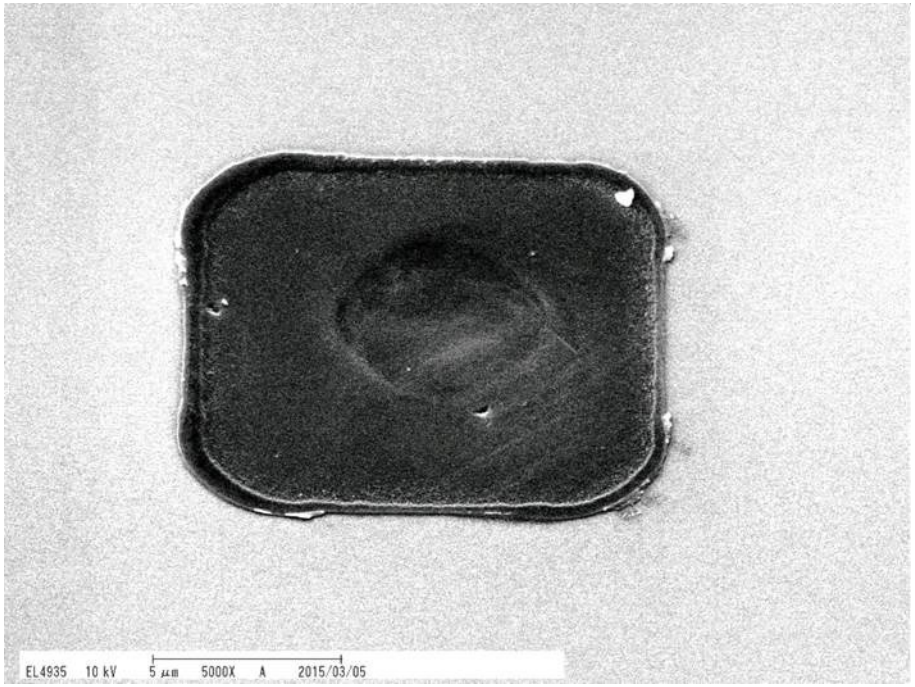


Reuse the deposited Au on photoresist

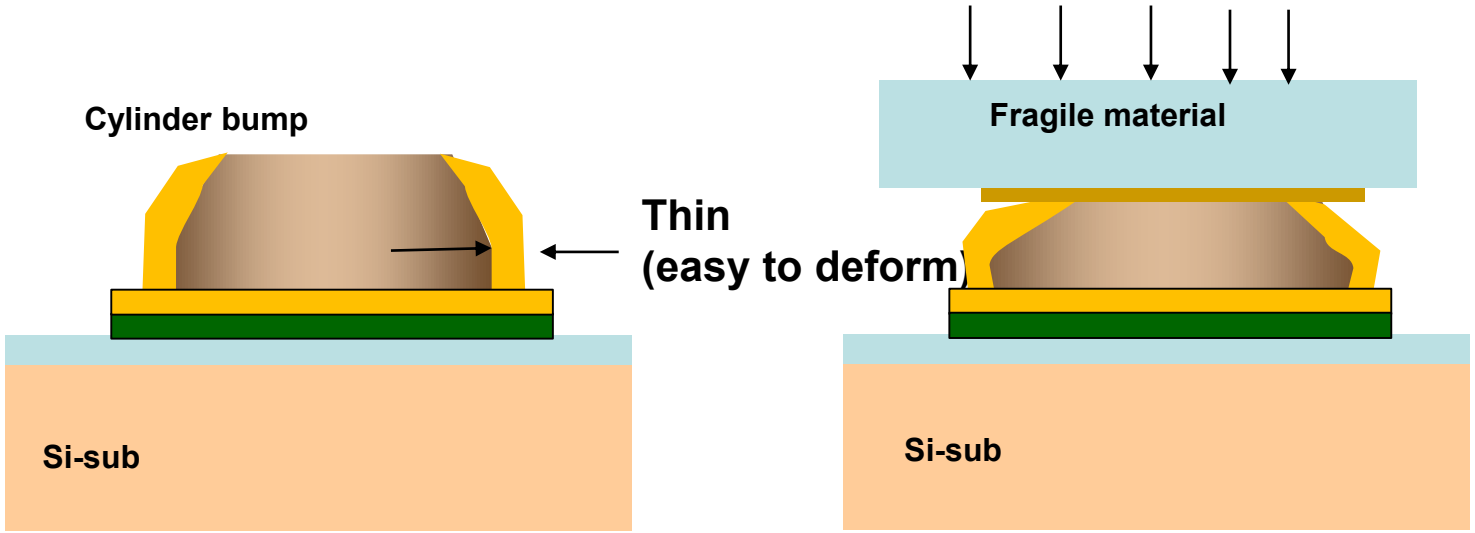
Cylinder Bump for fragile material

CdTe surface after CdTe/Si-ROIC bonding with Au bump



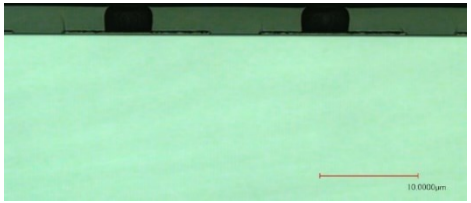


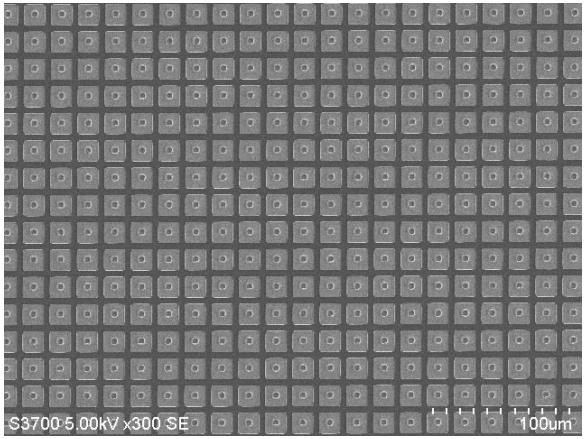
Bump bonding with cylinder Au bumps



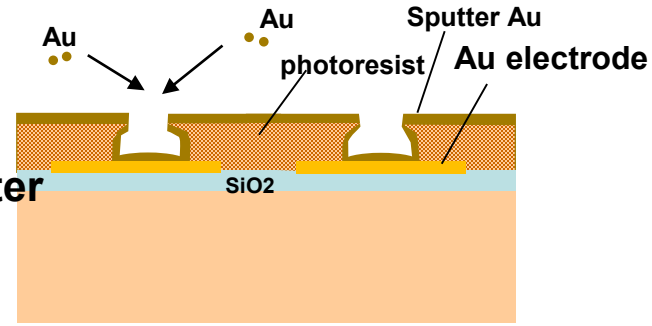
Bump bonding with cylinder Au bumps

Bump hole patterning

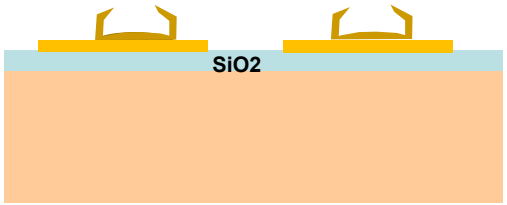


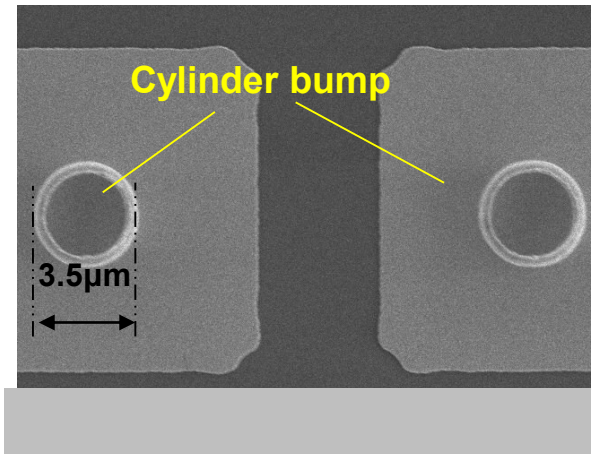


Short Throw（SL)Au spatter

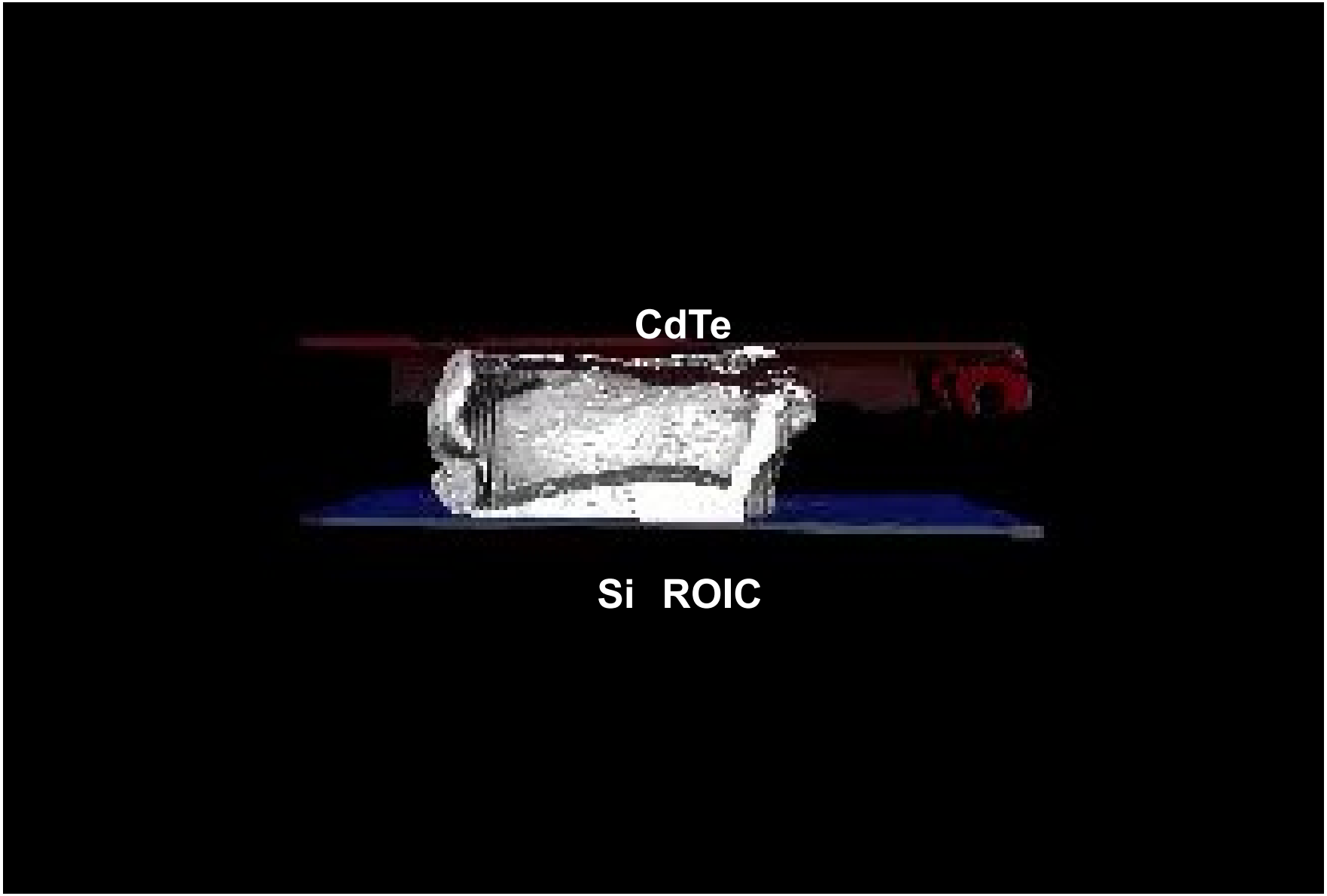


after photoresist lift-off





SEM cross sectional view



Process cost reduction for the Heterogeneous Integration

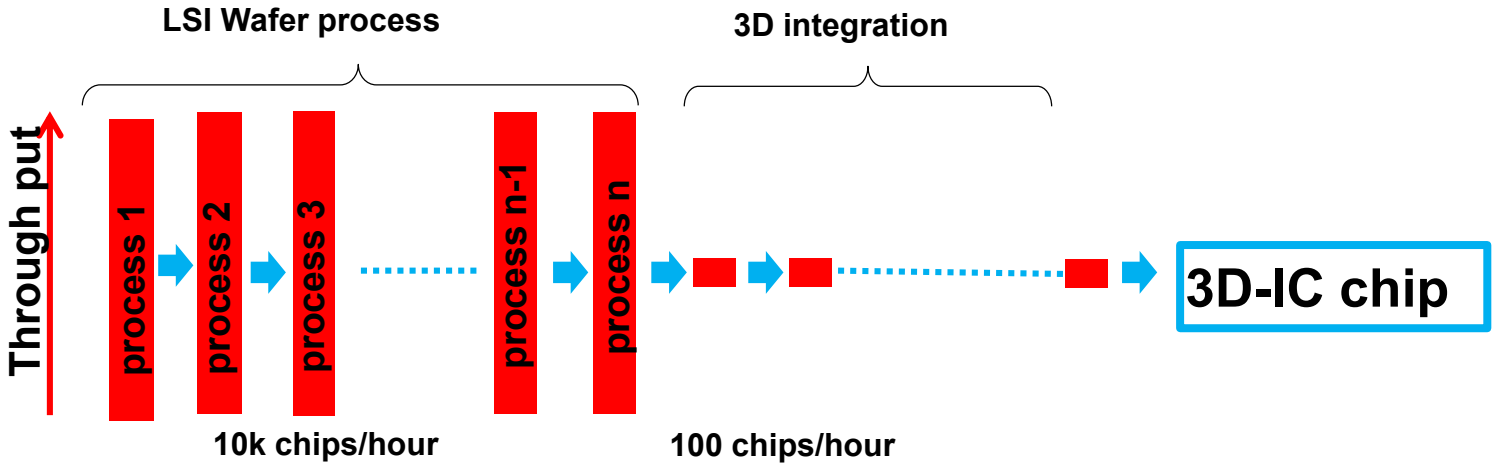
3D stack approaches

	CtC (chip to chip)	CtW (chip to wafer)	WtW (wafer to wafer)
			
Process cost	High	High ~ Middle	Low
Stack chips with different chip size	possible	possible	Impossible
Chip alignment accuracy <0.5μm (3σ)	Difficult from economical stand point		possible ?
Miscellaneous			Need high yield wafers $Y_{total}=Y_{W\#1}$ x····x $Y_{W\#n}$ Need same size wafers

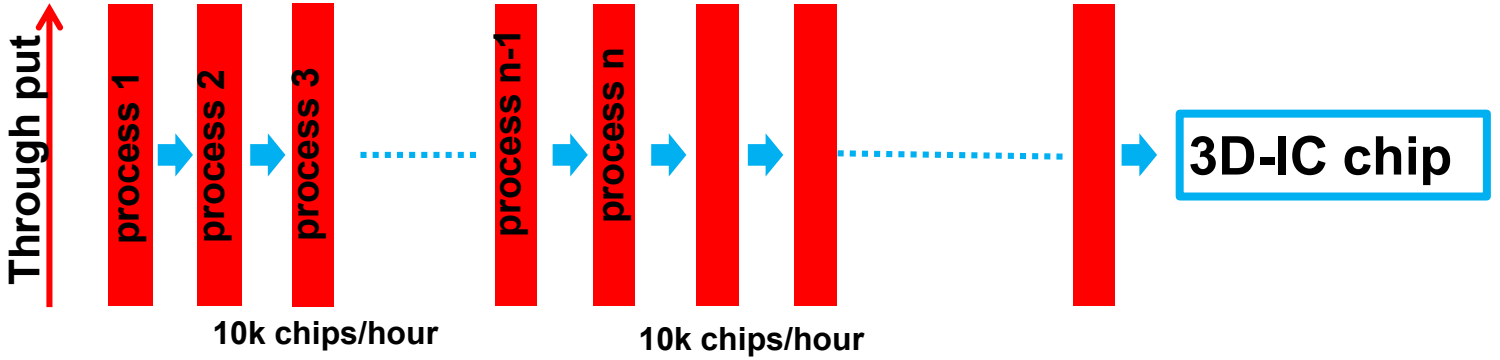
Need a high speed COW technique with the high alignment accuracy and the practical process cost

Economy of 3D LSI manufacturing

(a) Current 3D Production



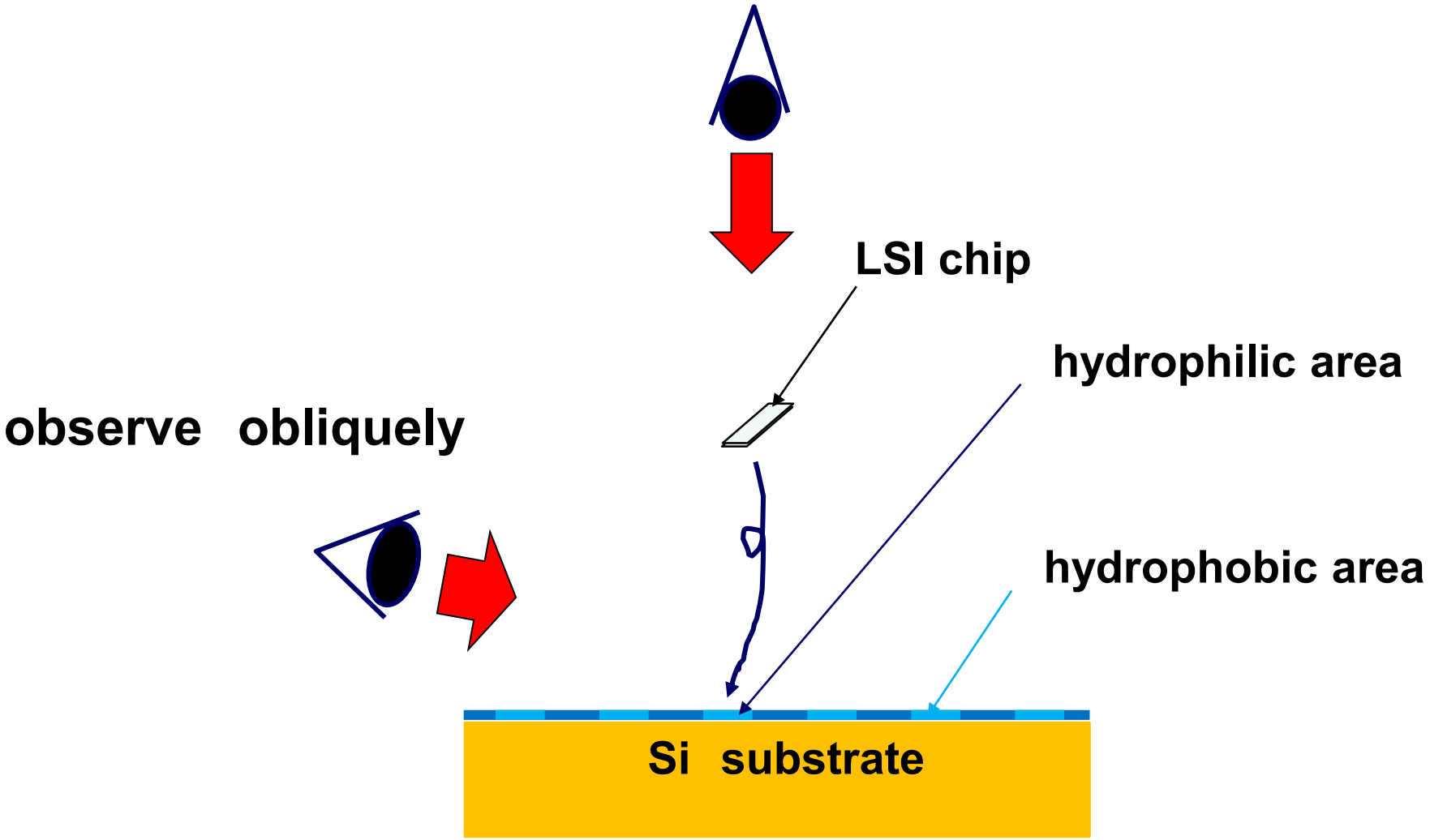
(b) Our Target



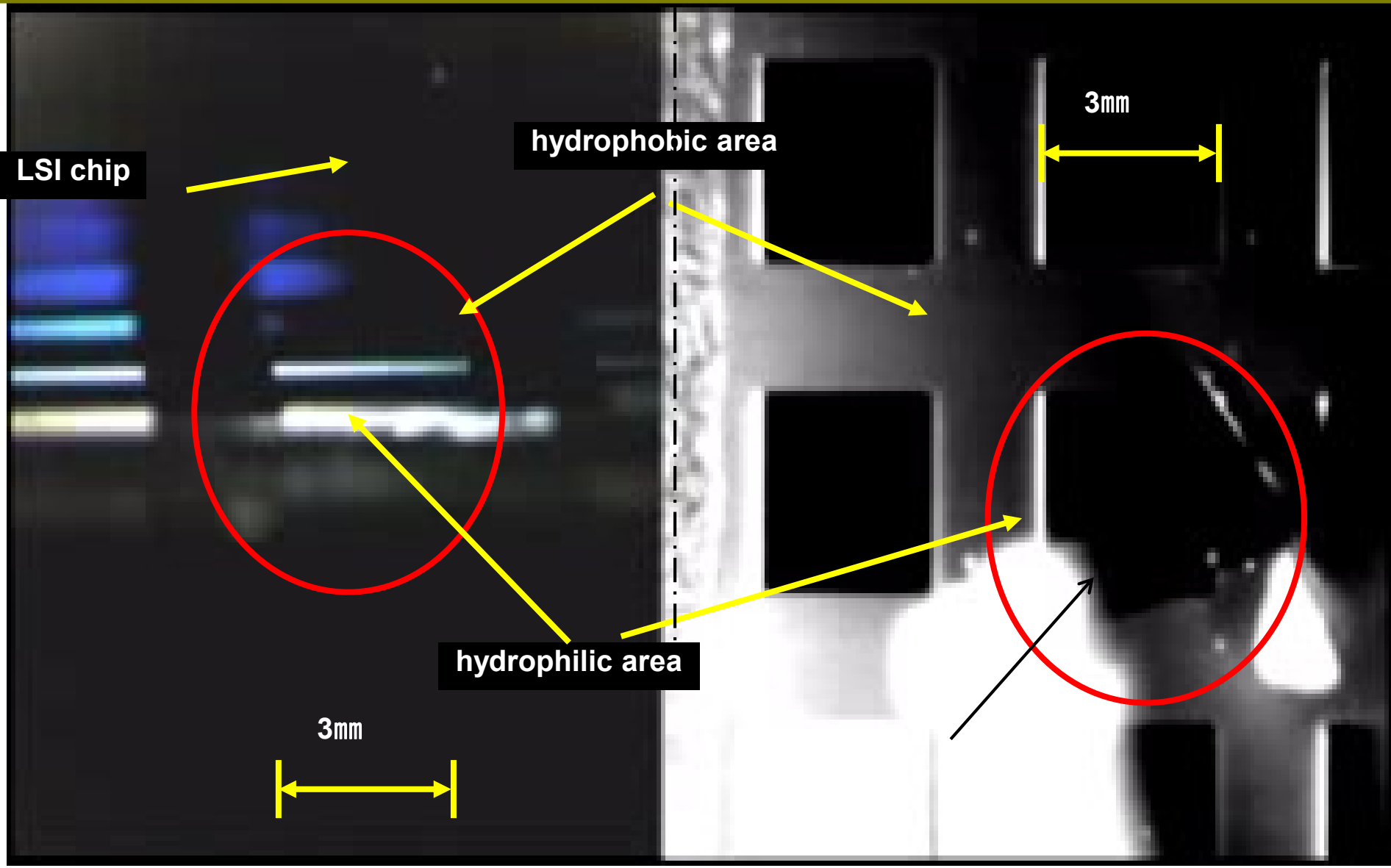
“Super Chip”
Self-assembly Technique

Self-assembly technique

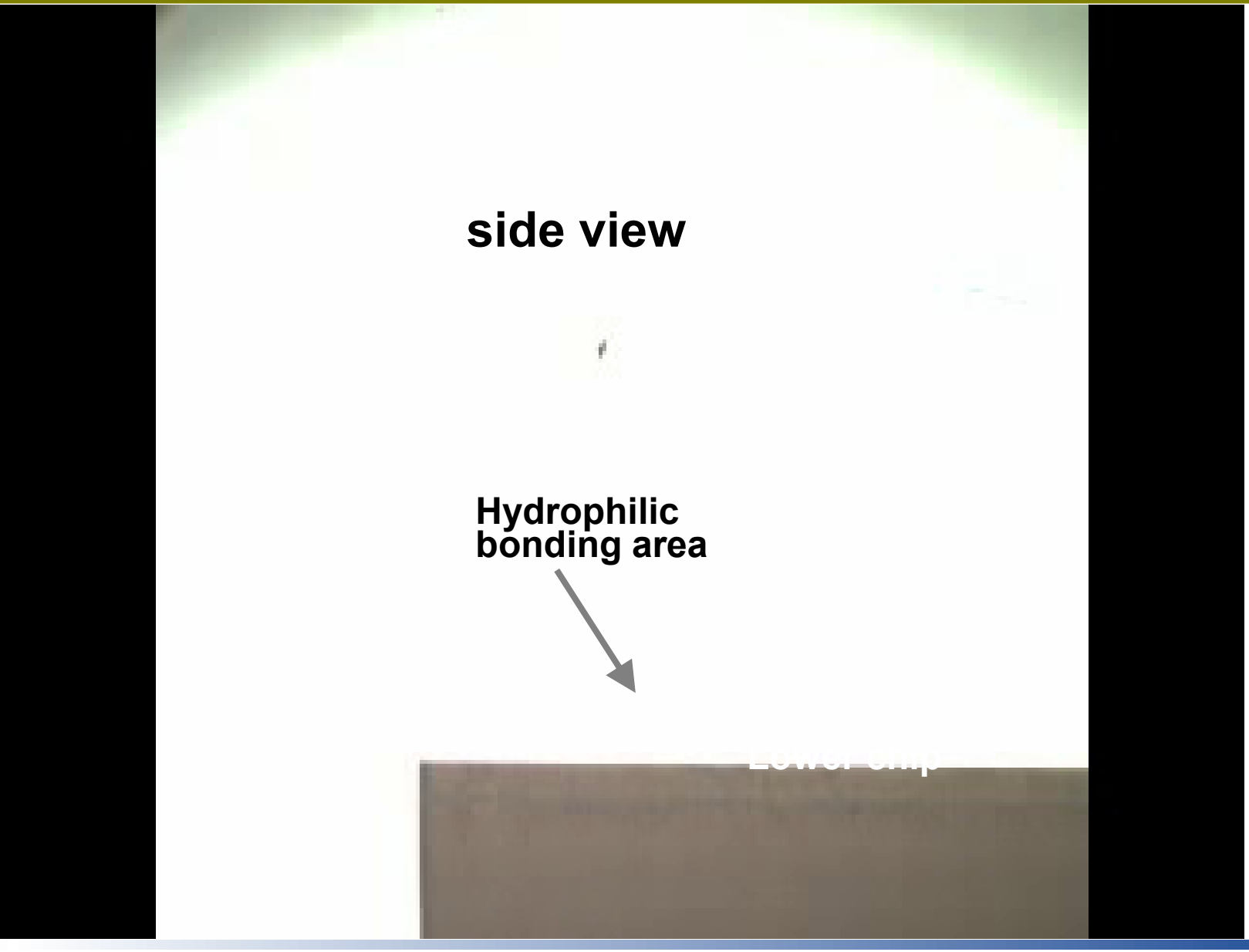
observe from direct above



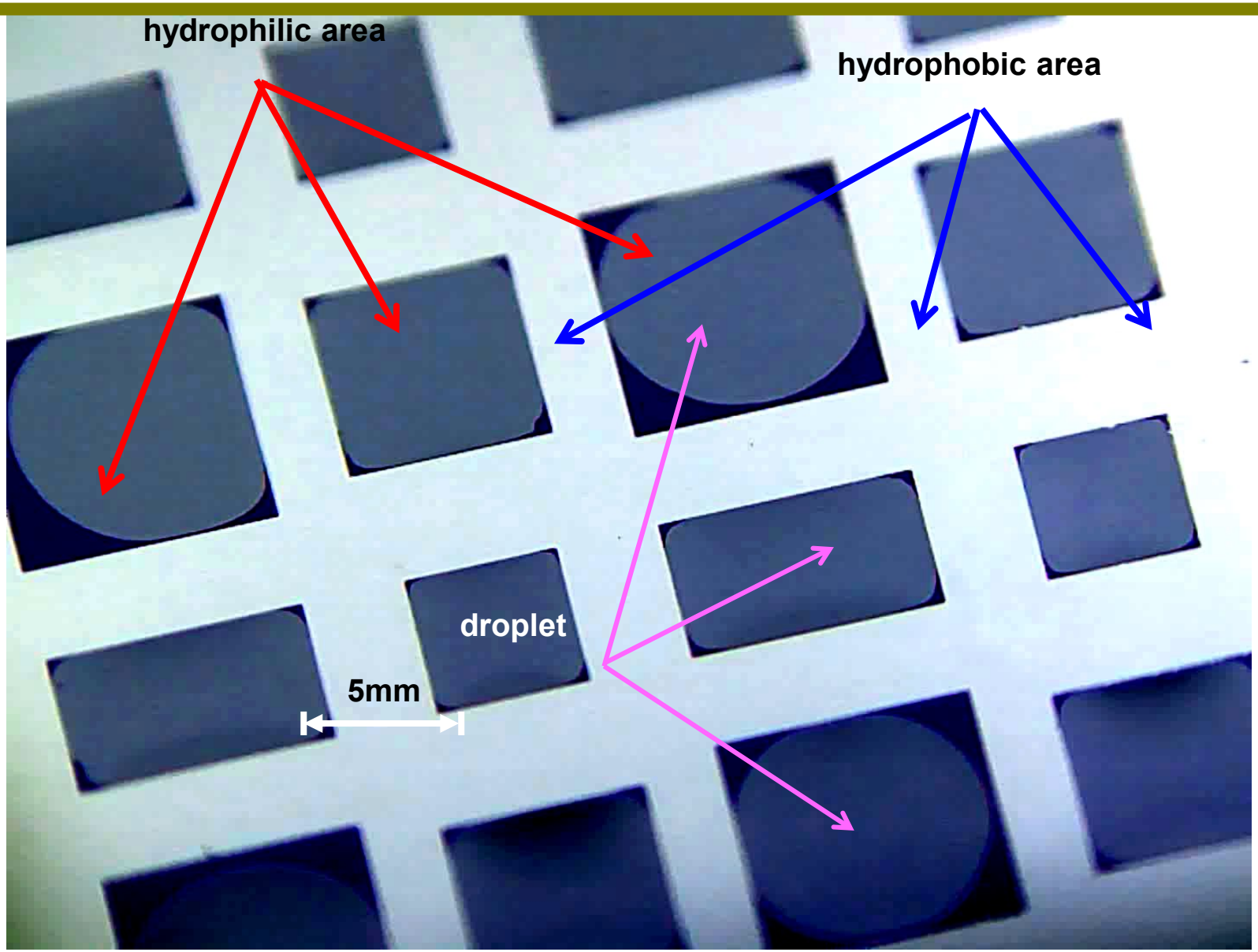
Self-assembly technique



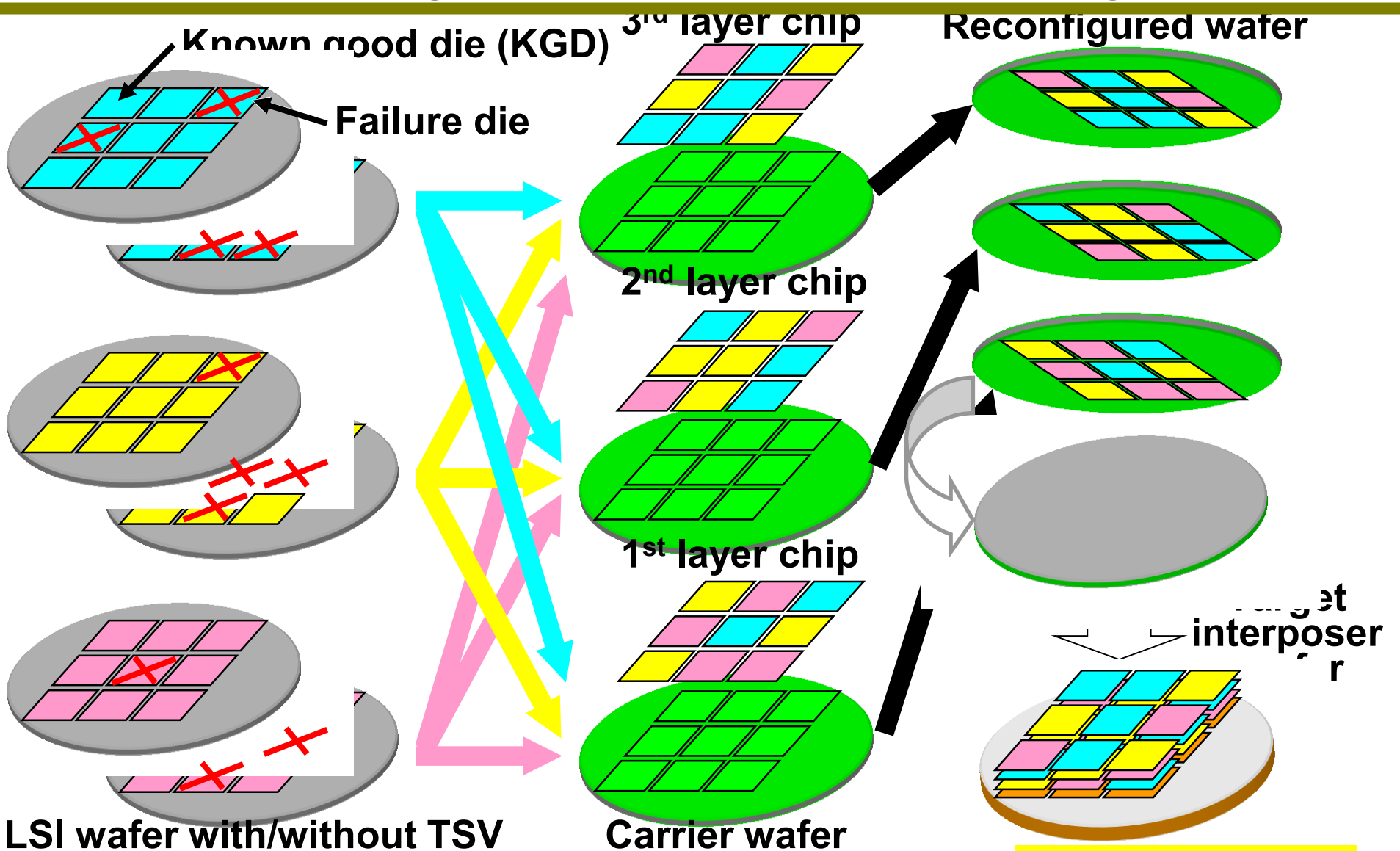
Self-Assembly Event observation using a High-Speed Camera



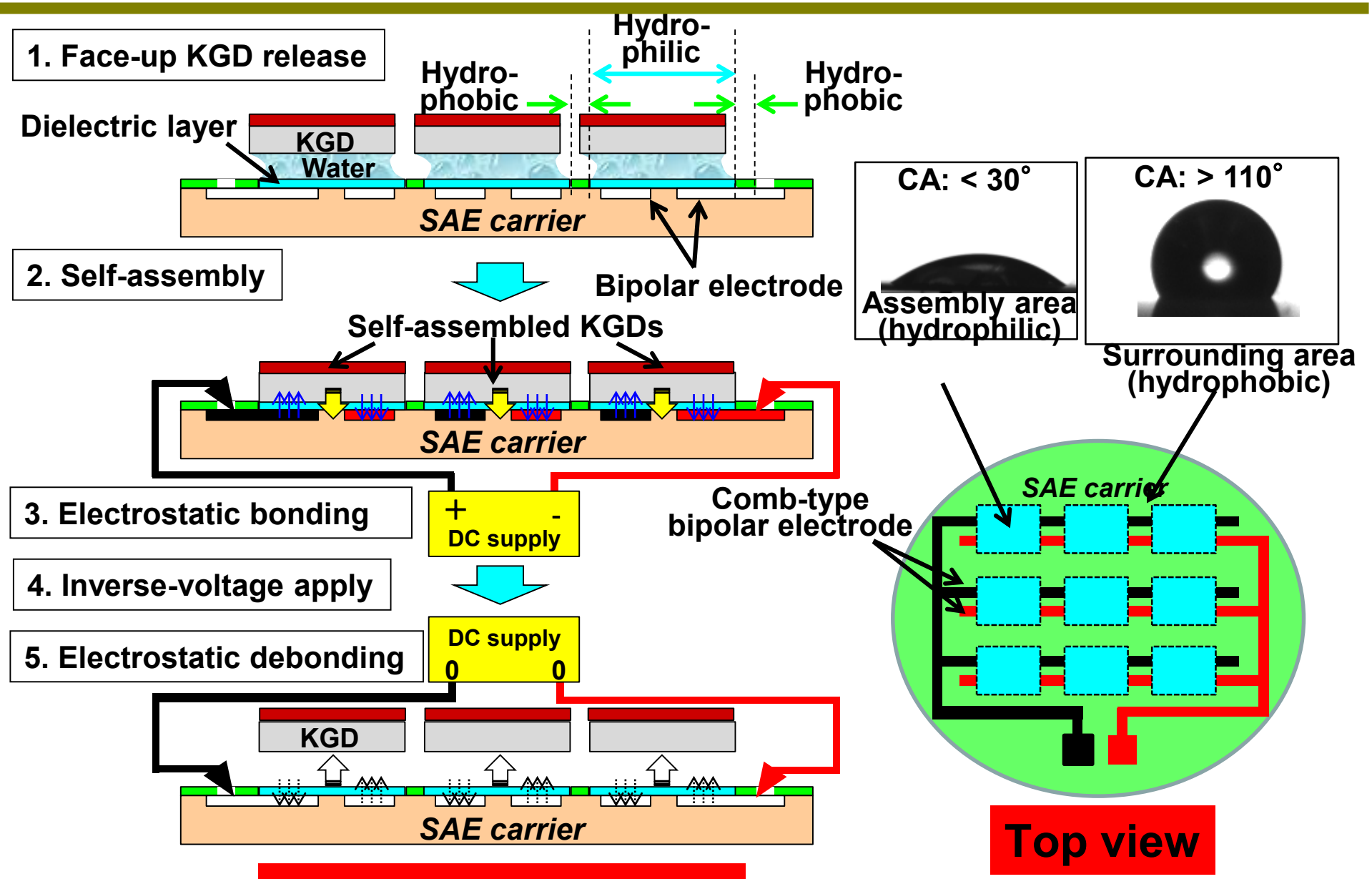
Self-assembly technique



New Reconfigured Wafer-to-Wafer 3D Integration



Self-Assembly & Electrostatic (SAE) Bonding















Summary

1. The recent 3D-IC trends and with TSV were described.

2. Advantages of 3D-LSIs are
   - (a) Increase of electrical performances
   - (b) Increase of circuit density
   - (c) New Architecture (Hyper-parallel processing, Multifunction, etc)
   - (d) Heterogeneous integration
   - (e) Cost reduction

3. Many 3D-Integration approaches have been reported.
   Considering supply chain of the base LSIs and variety of applications, it is difficult to unify.

4. 3D LSI Integration technology using 2.5μmφ Au cone bump is verified using SOI stacked pixel detector as circuit level test device.

5. 3.5μmφ Au cylinder bump for soft & fragile material, such as CdTe, is developed.

6. We confirmed that the CtW approach with a self-assembly-lump bonding technique will be effective for cost reduction.