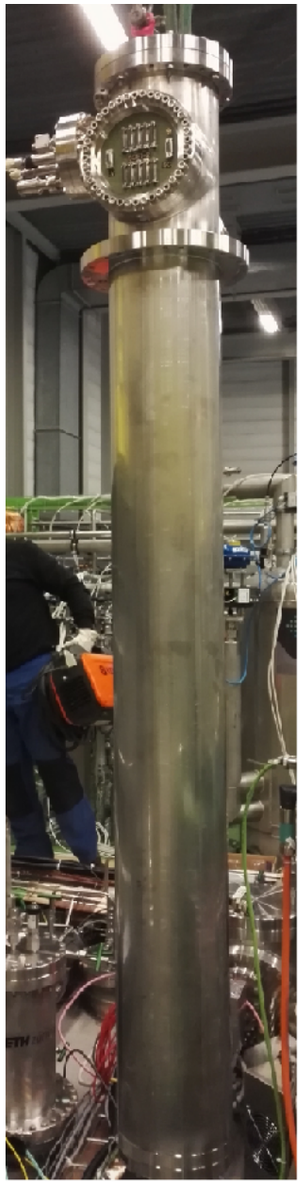
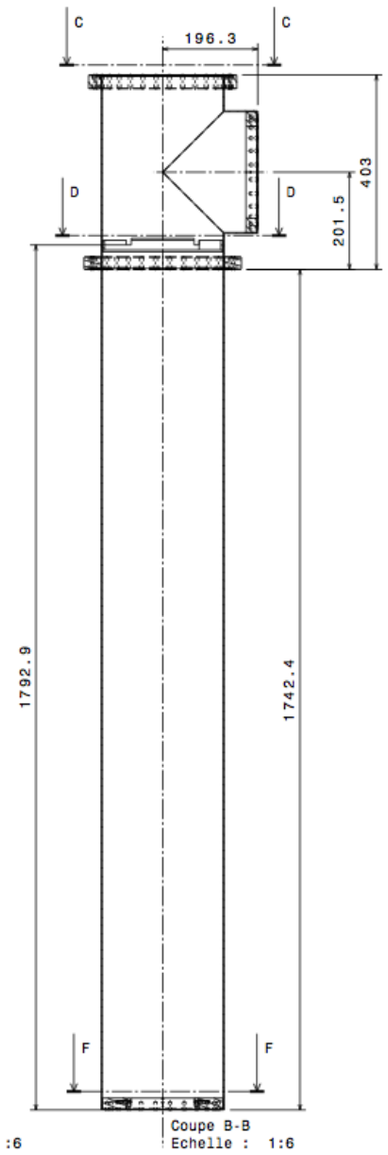
Design of SGFT and decoupling capacitor

Signal feedthroughs



3x1x1:
-320 channels (5 cards)
-DN-200 tube

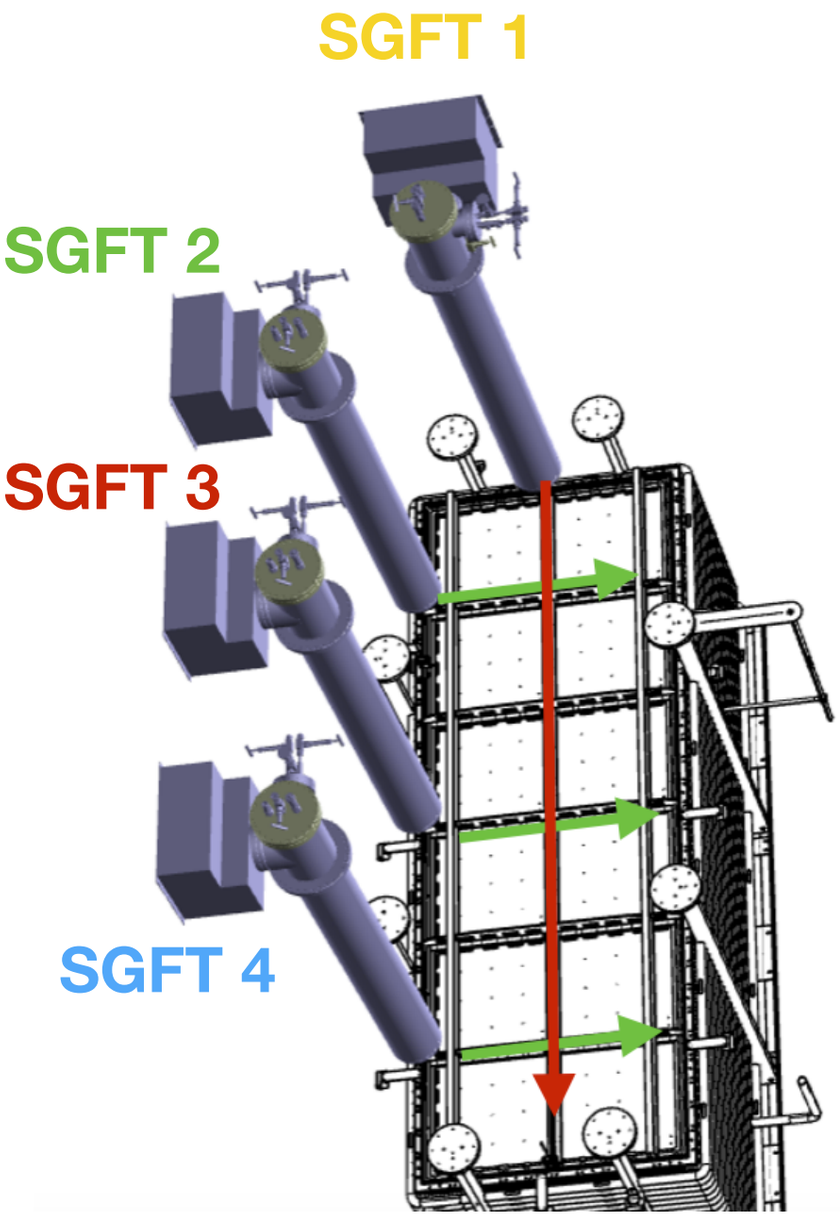


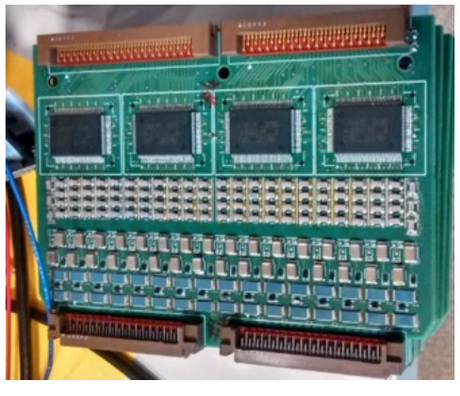
pD-DP:
-640 channels (10 cards)
-DN-250 tube
-preliminary 2D on CERNbox

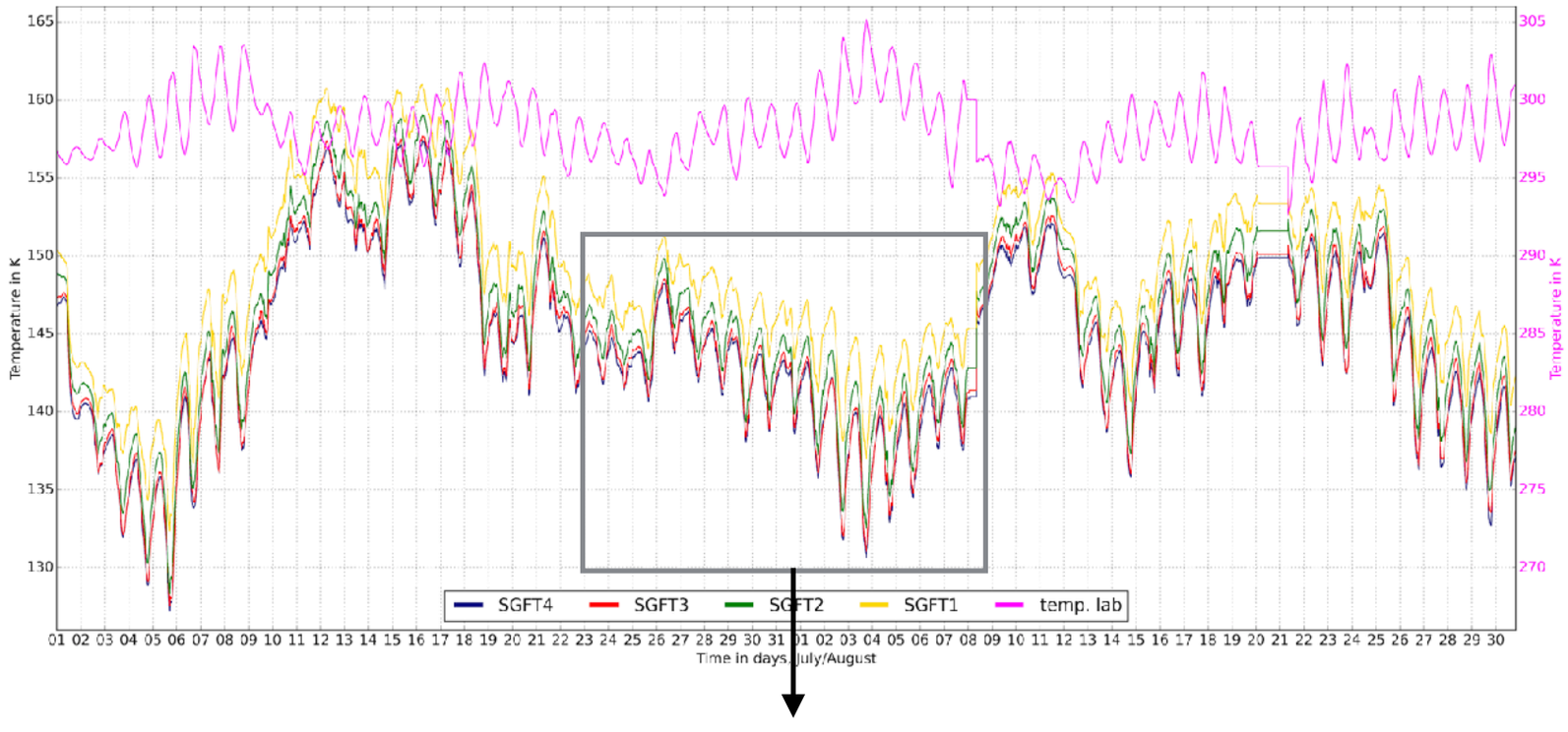
experience from 3x1x1:
-production of the tube takes a lot of time (many months)
-important to have a 1st prototype asap
->for the 6x6x6 simplify the design (faster and cheaper)
->parallelise fabrication (multiple companies)
->converge on final design now to start tendering and ordering

Critical path any delays directly impact the detector installation schedule

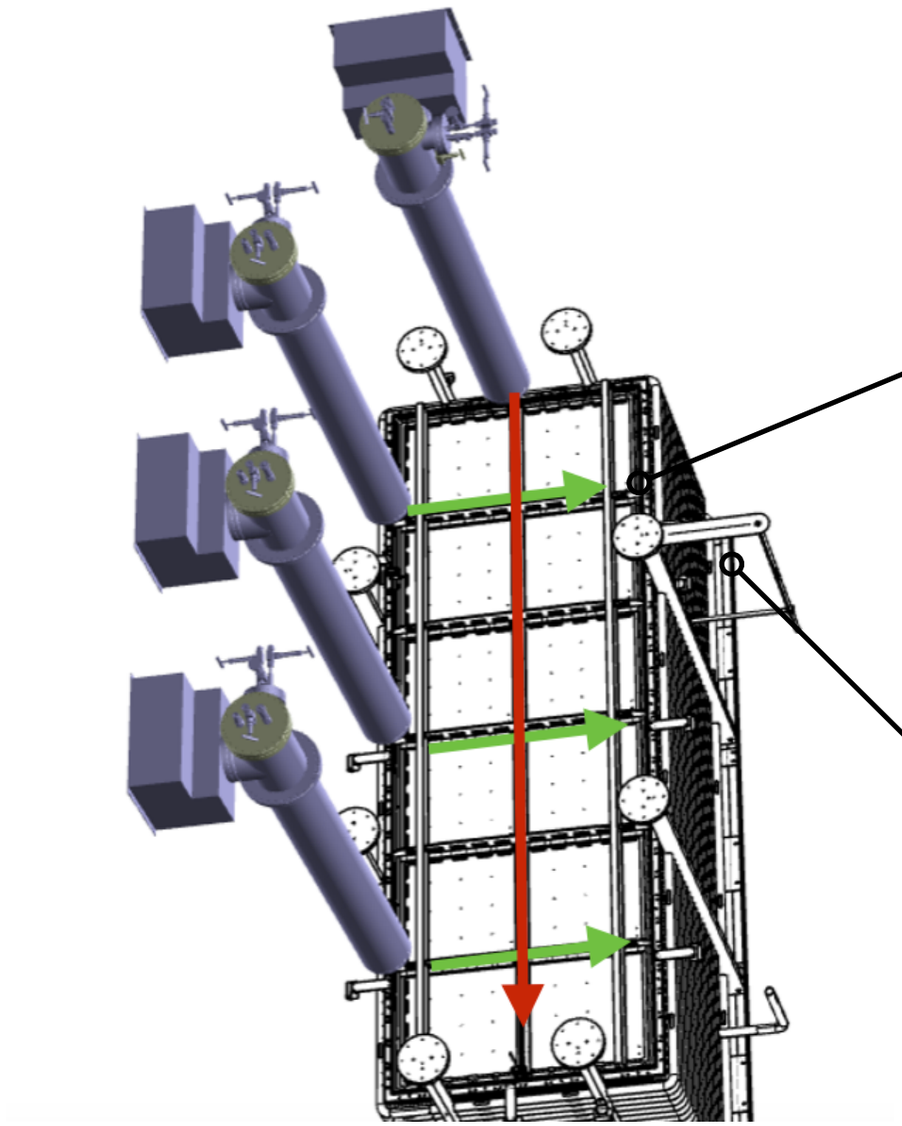
Charge Readout principle (3x1x1)



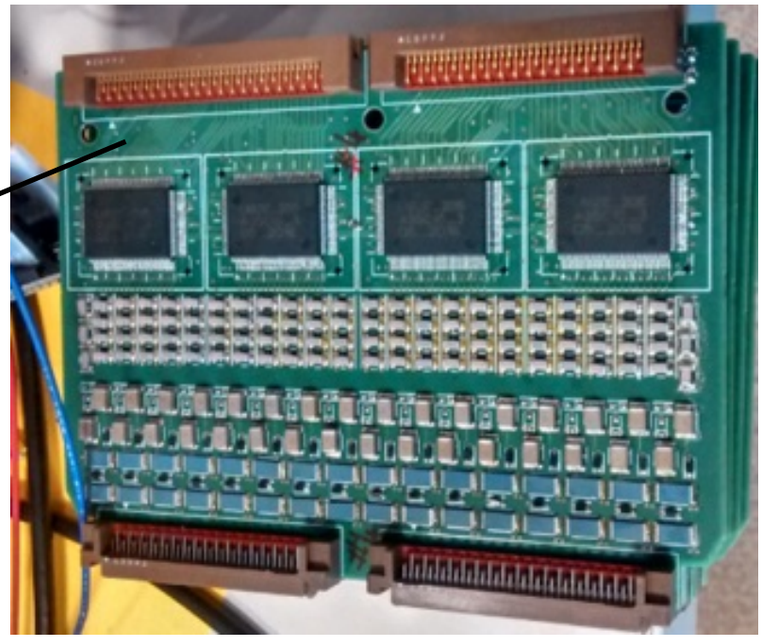


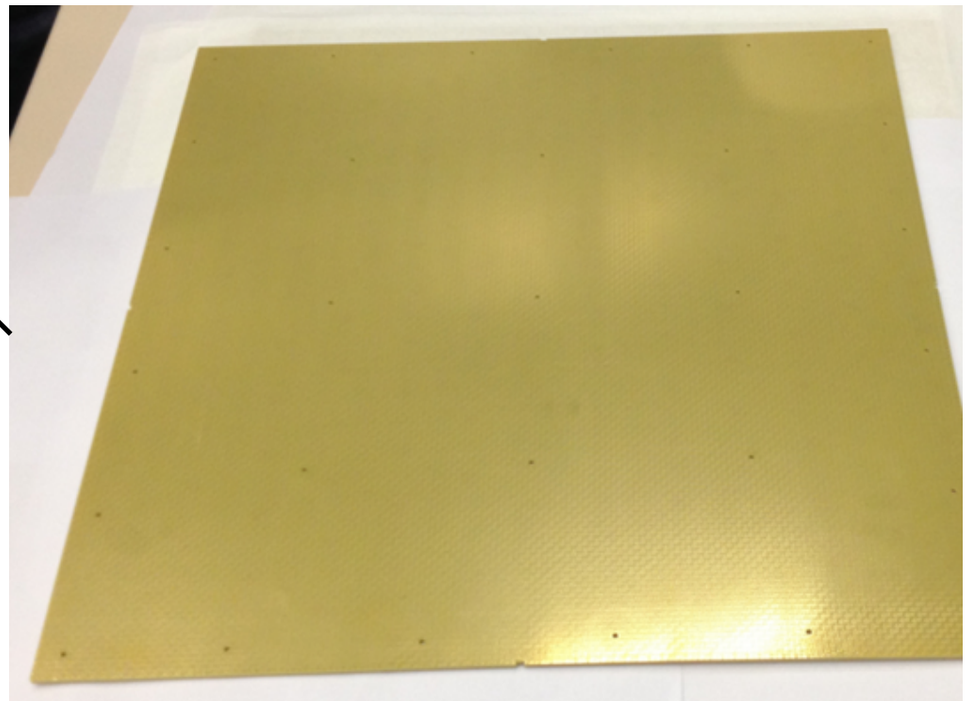


Charge Readout principle (3x1x1)



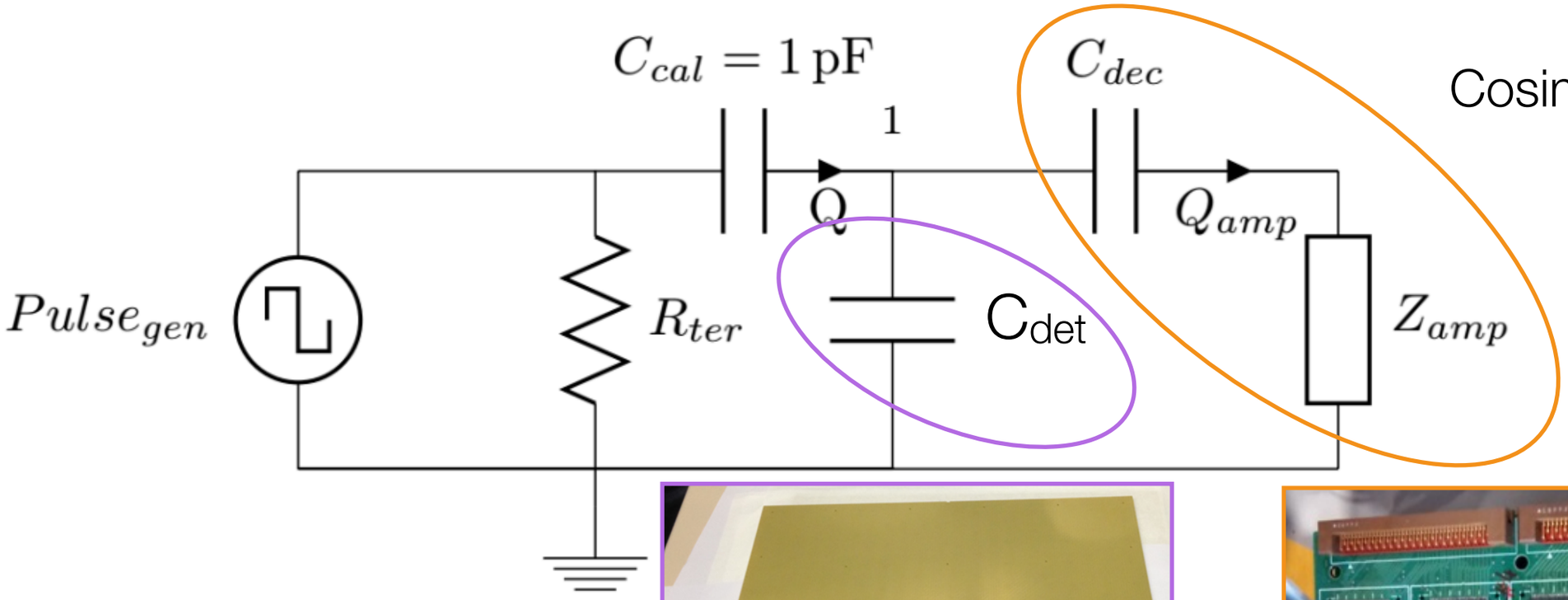
analog front ends (inside chimney ~140 K)

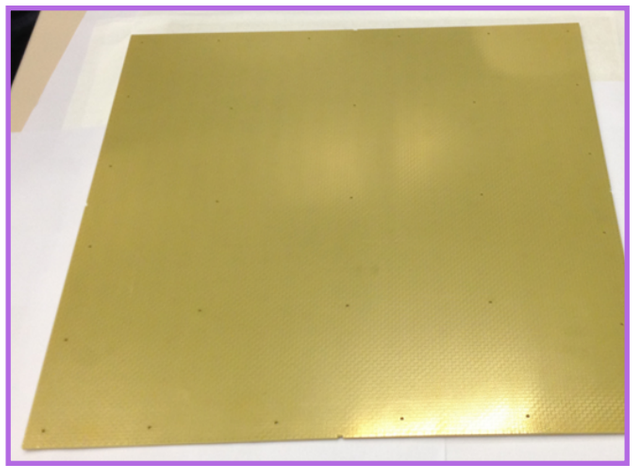


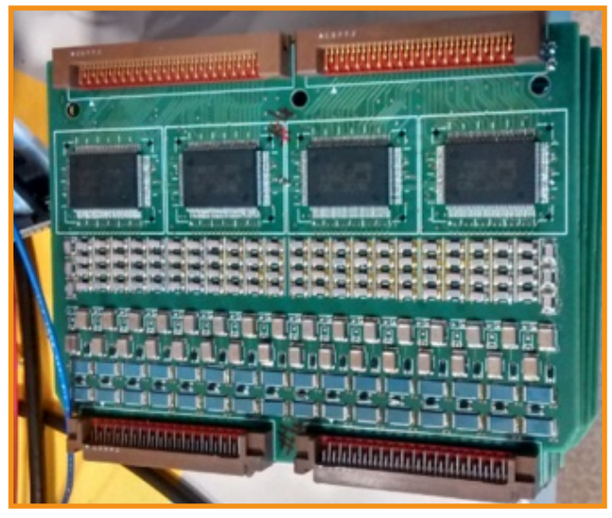


Simplified anode/preamp model

Cosimo C.







$$\frac{Q_{amp}}{Q_{inj}} = \frac{1}{1 + \frac{C_{det}}{C_{dec}}}$$

as low as possible (anode design)

as large as possible (availably of components + FE design)

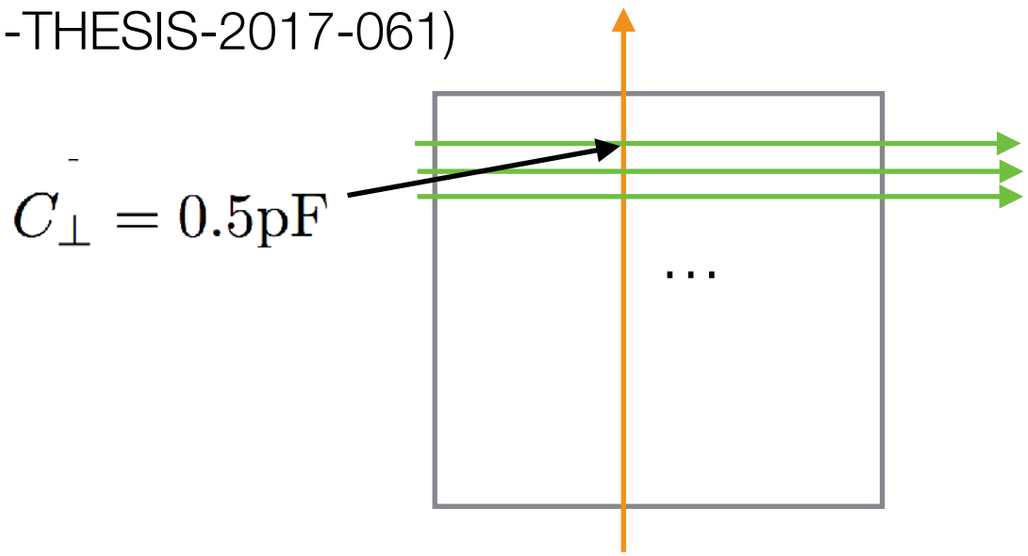
Capacitance of the anode (C_{det})

We now have a detailed understanding of the anode inters-trip capacitances and the capacitance of one anode strip to GND (C_{det})

- First measured by Franco (150 pF/m) in 2014 on 10x10 proto anode (JINST 9-03-03017)
- Simulated by Pin Jung C. in spring (master thesis ETHZ)
- Measured by Caspar S. in spring (master thesis CERN-THESIS-2017-061)
- Measurements confirmed at IPNL last July

All results are consistently point to

$$C_{det} = N_{cross} \times C_{\perp} + 2 \times C_{||} + C_{ground}$$
$$\simeq N_{cross} \times C_{\perp}$$
$$\approx 160 \text{ pF/m}$$



the detector capacitance seen by one strip is dominated by the inter-strip capacitance of each perpendicular strip it crosses.

	Measured	COMSOL Simulations
Capacitance 1 strip to all others	78 pF	36.14 pF
Capacitance 1 strip to anode back strip	1.7 pF	/
Capacitance 1 strip to closest parallel strips	7.6 pF	1.3 pF
Capacitance 1 strip to 2nd closest parallel strips	1.2 pF	/
Capacitance 1 strip to 3rd closest parallel strips	0.5 pF	/
Capacitance after 4th closest parallel strips	< 0.4 pF	/
Capacitance to perpendicular strips	0.4-0.5 pF	0.15 pF

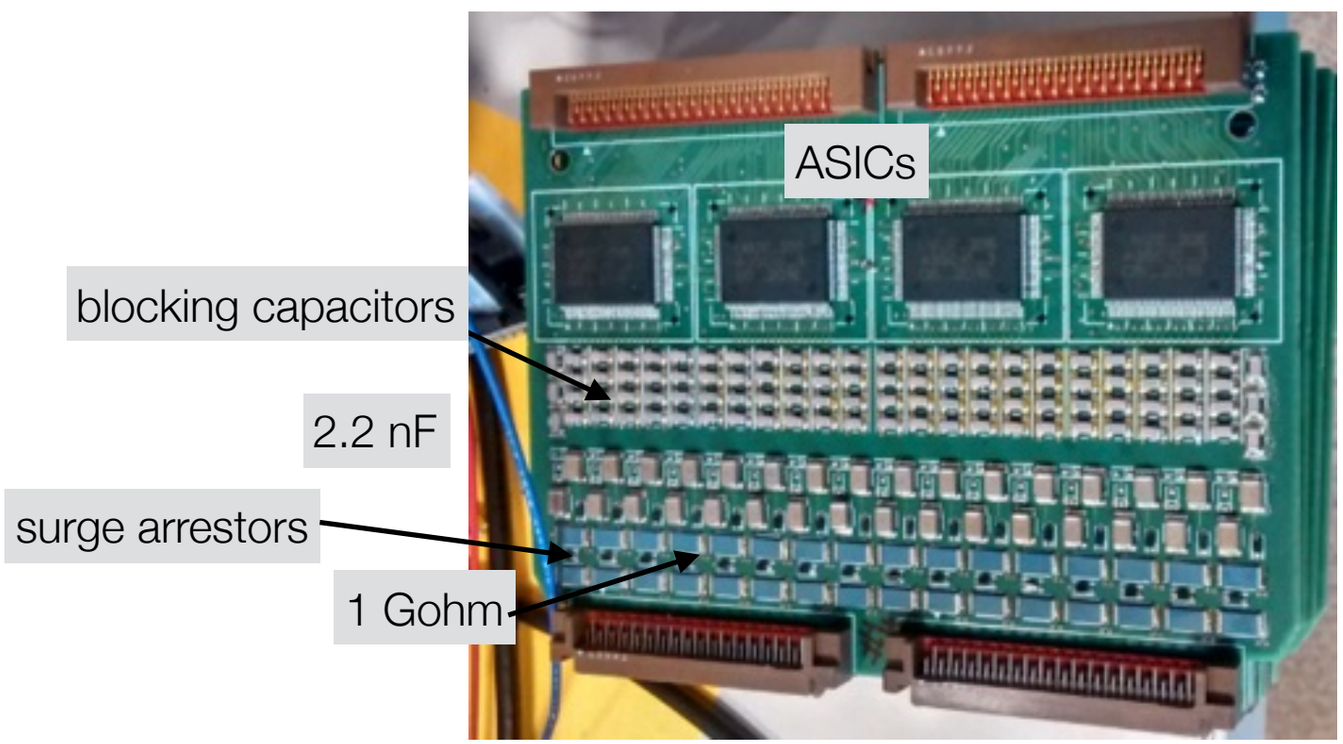
3 m view (N_{cross}= 960) C_{det} ~500 pF

1 m view (N_{cross}= 320) C_{det} ~160 pF

FE decoupling capacitor (C_{dec})

March 2016: discussions to validate the scheme for the passive FE components on the cryogenic amplifiers cards for the connections to the strips:

- Bias resistor to put the strips at GND: 1 GOhm
- Decoupling capacitor : set a requirement of >=2 nF, considering 450 pF of strips capacitance to GND. At that time inter-strip capacitance was not know but charge loss is the same for 450 pF of capacitance to GND or 450 pF related to inter-strip capacitance.
- Surge arrestors (several components extensively tested with a sparks generation system in the previous months)



FE decoupling capacitor (C_{dec})

Constraints on the capacitors :

➢C >= 2 nF

➢Working reliably at cold

➢Standing HV (preventing damages from sparks), similar requirement for the 1 GOhm resistor

➢Contained costs

➢Fitting in the FE cards total envelope

The space on the card is fully exploited also for the components thickness and the FE components (R,C, surge arrestors) for the other half (32) of the channels are at the back of the card

Tried to get the largest possible value of capacitance

Selected the 2.2 nF capacitors by NOVACAP in COG (NPO) MLLC technology:

- Rated for 2 kV
- Packaging 1812 (H 1.55, L 4,57, W 3.18 mm)
- Cost: 2 eur/piece (they are quite expensive and with the bias resistors dominate the cost of the FE card, the cryogenic ASICS are at the level of 1 eur/channel, extra cost not initially foreseen)

FE decoupling capacitor (C_{dec})

Initially wrongly thought there was a factor ~2 attenuation between the 1 m vs 3 m strip (see later). This pushed further the search for having a larger decoupling capacitance before the ASICs.

Possible solutions:

A. <u>add an extension card before the FE card with additional capacitors</u> (preserves existing FE cards):

1) Given the circuit topology this can be added only in series, would imply to remove the existing decoupling capacitors on the FE cards and short-circuit these connections (otherwise these would dominate the capacitance), would imply displacing also the bias resistors and surge arrestors on this extension card
2) Not clear how to attach the FE card which is designed to be directly plugged on the cold flange to this extension card in order to guarantee a stable contact during the blade insertion/extraction

->Would imply in any case some modification to the FE cards

Capacitors on the extension card could be many of the actual capacitors in parallel or new larger capacitors

For instance to reach 10 nF/channel would imply putting 5 capacitors in parallel -> ~10 eur/channel, ~80 keur for the 6x6x6, the extra cost is always quite important, also considering larger capacitors (see next slide)

B. <u>Modify the FE cards by extending them in height and including new capacitors</u> (either many of the existing ones in parallel or larger ones)

1) Easier mechanical attachment
2) Extra time to redesign the cards, not recovering the 20 cards from the 3x1x1

FE decoupling capacitor (C_{dec})

Many capacitors in parallel or larger capacitors?

Searched for larger capacitors on the market -> Examples shown in the table of NOVACAP HV capacitors in COG (NPO) technology, looked also at products from other companies like KEMET which are more expensive

C (nF)	Cost per piece (eur)	Packaging	H (mm)	L (mm)	W (mm)
2,2	2	1812	1,55	4,57	3,18
8,2	10	3333	6,35	8,38	8,38
15	18	4040	7,62	10,2	10,2

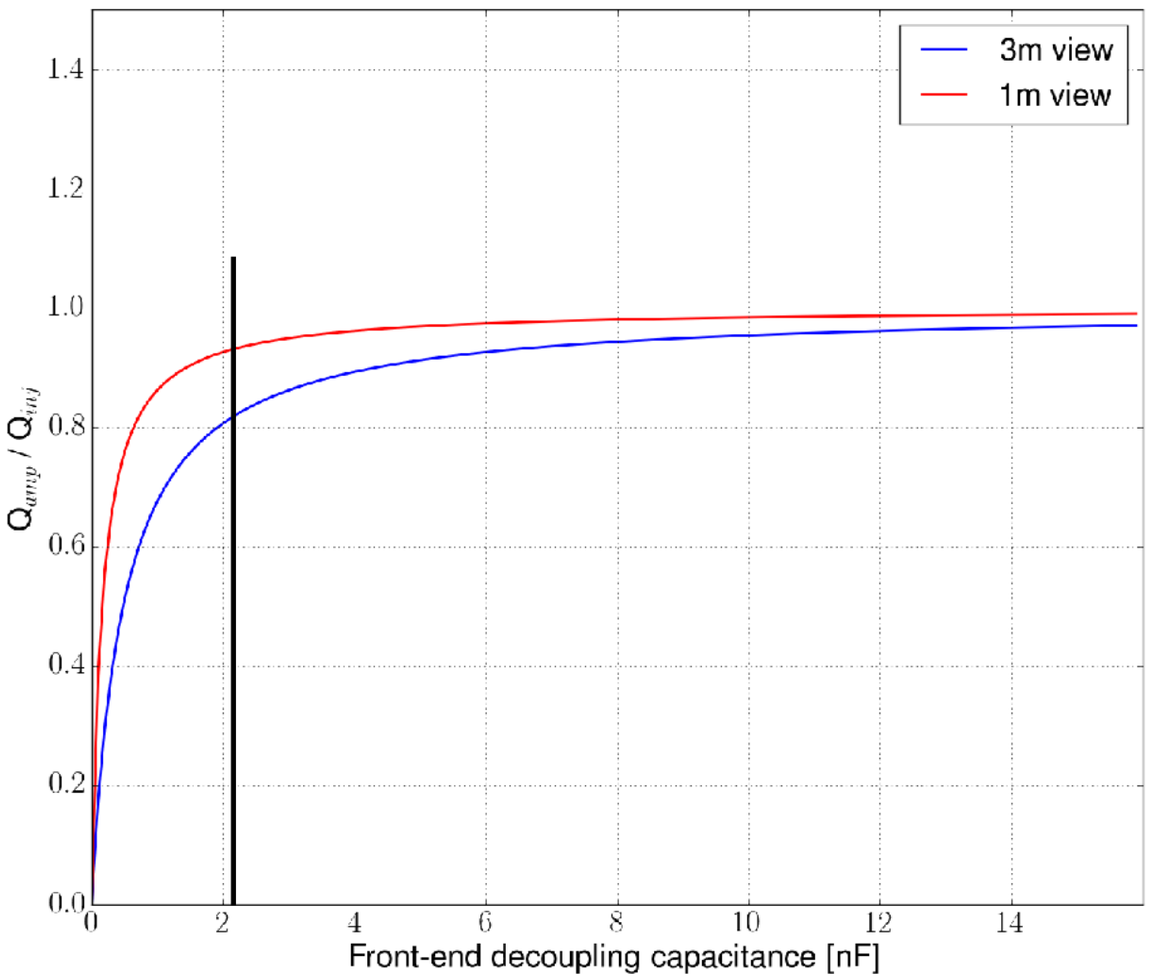
- Larger capacitors are quite bulky (e.g. 6.4 mm thickness and 8.4 mm footprint for a 8.2 nF capacitor)
- The thickness can be really an issue since the cards already now have almost no perpendicular dead space when sliding on the blades
- There is no clear gain in cost with respect to the option of using many of the existing capacitors in parallel

The increase in capacitance, which was investigated in view of mitigating the apparent factor 2 in the pulser data among the 3 m vs 1 m strips (which is now excluded), implied several complications needing a redesign and modification of the FE cards (extension cards are not practical to implement for mechanics and modifications needed to existing cards) and important costs : ~80 keur in capacitors needed for instance to reach 10 nF

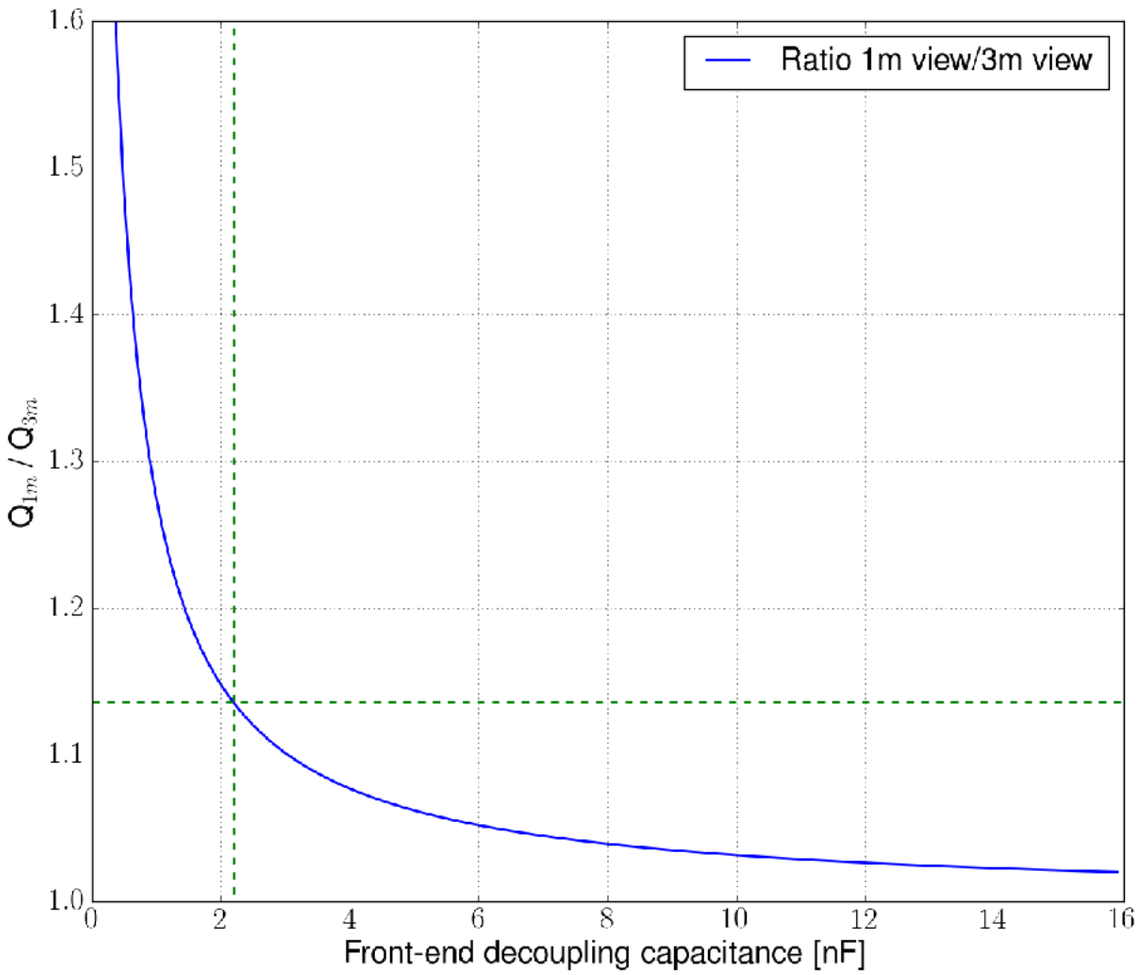
Expected attenuation with C_dec of 2.2 nF

$$\frac{Q_{amp}}{Q_{inj}} = \frac{1}{1 + \frac{C_{det}}{C_{dec}}}$$

with C_dec= 2.2 nF we expect:
-about 81% of the charge on the 3m strip (C_det= 500 pF)
-about 93% of the charge on the 1m strip (C_det=160 pF)



The ratio between the two views is expected to be around 15%



Kevin F.

Measured 3m vs 1m - pulsing data

From pulsing data: the measured ratio of the charge (integral of waveform) between 3m and 1 m strip is **15%.**

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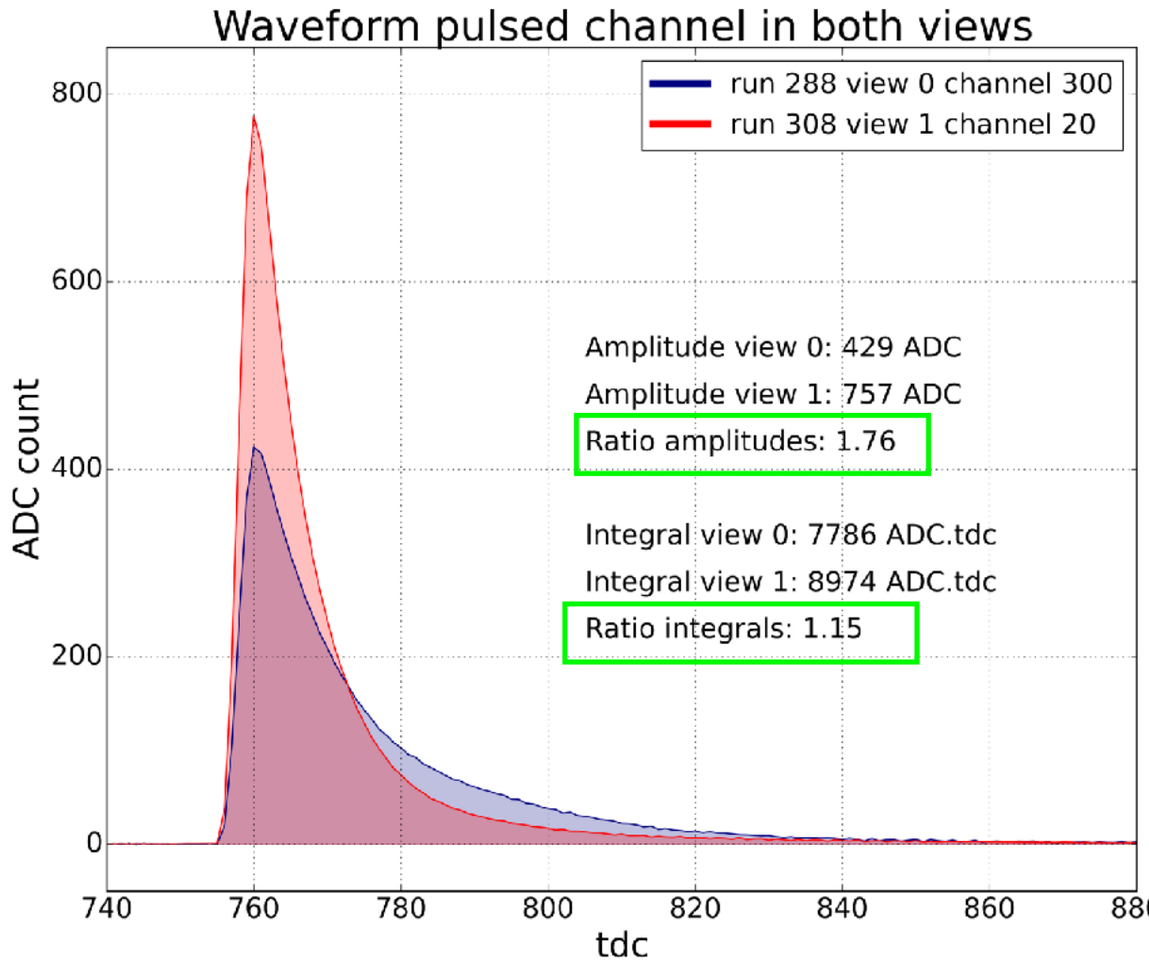
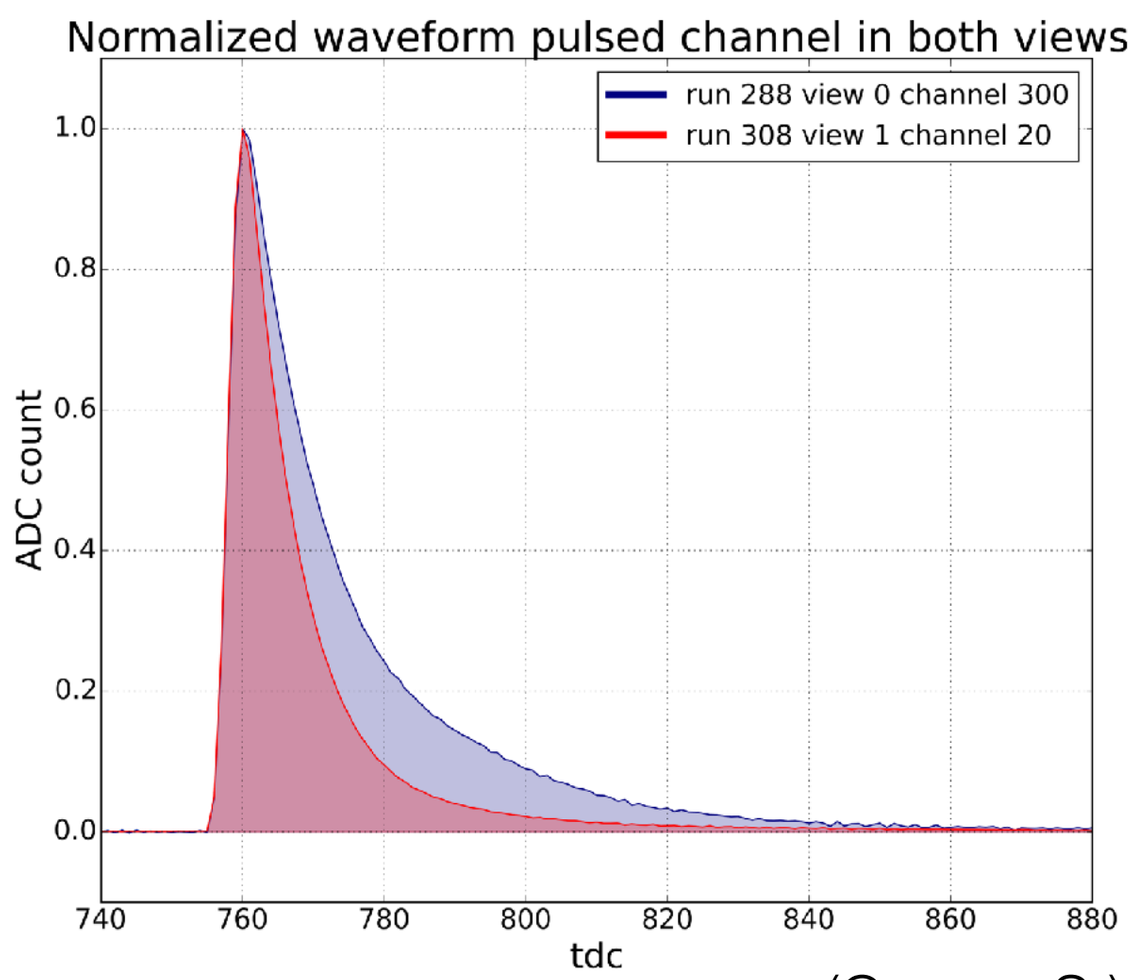
averaged waveform on ~300 events





pulsing data December 2016 (pulser=150 mV pp, 100 ns risetime) (Caspar S.)

3m vs 1m reconstructed MIP data

The measured ratio on the dQ/ds measured for a MIP between 3m and 1 m strip is also consistent with ~15%

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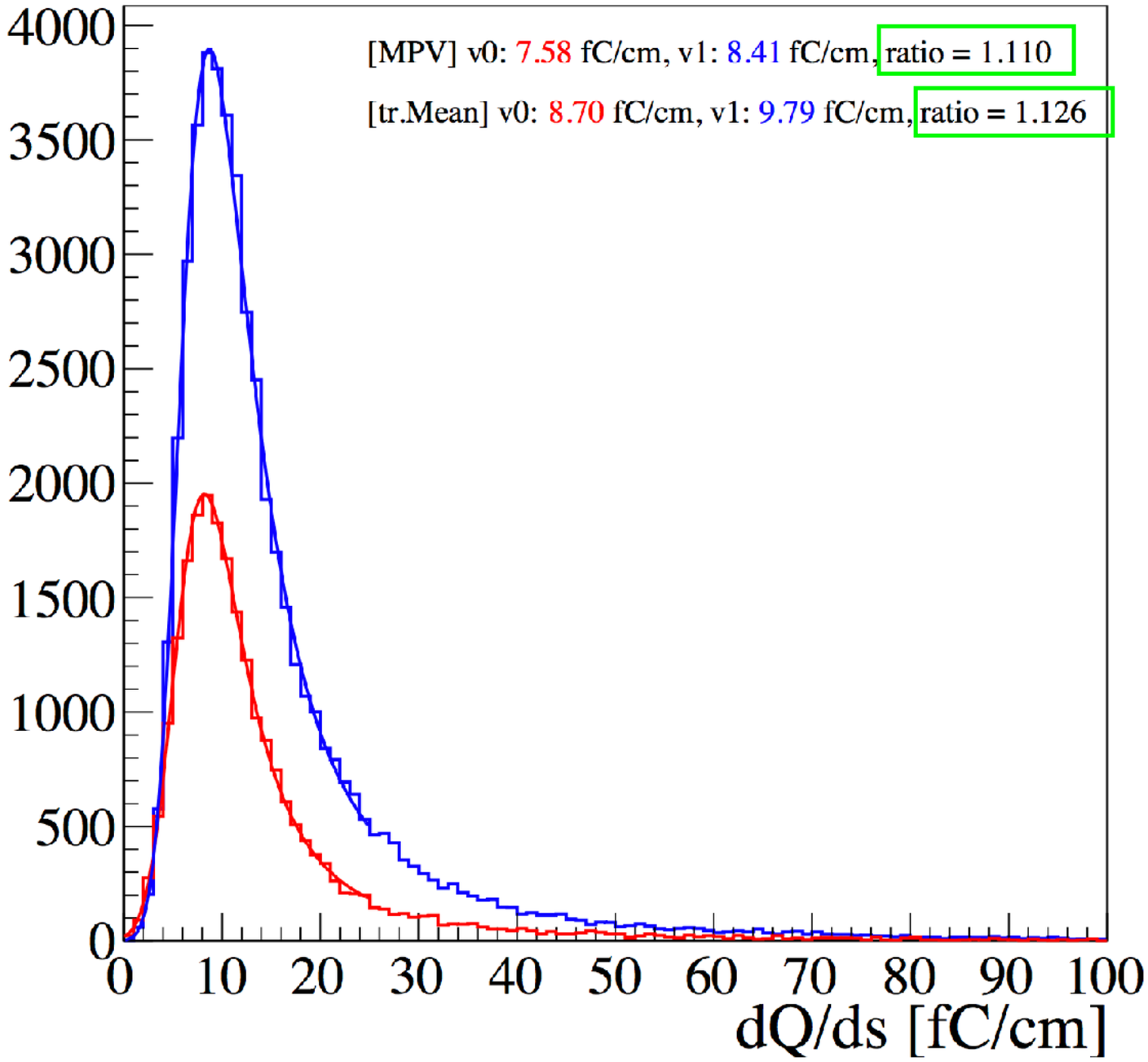

Conclusions

- for pD-DP and with the current setup of anodes + FE (3 m strips) we can confirm that about 80% of the charge will reaches the preamps.
- This is what we would have expected initially and it is confirmed by the analysis of the 3x1x1 data.
- Initial analyses performed pointed to a factor 2 which is now understood to be wrong.
- Design of the anode is years of R&D to try and find the best compromise between 2 view charge sharing and minimal dC/dl. We also have gained a deep understanding of all its inter-strip capacitances and C_det.
- Motivated by the initially assumed factor 2 attenuation investigations were pushed further to find solutions to have larger C_dec. Those found solutions solutions carry major implications:
  - 1) complete redesign of the current FE cards
  - 2) add a significant amount of cost (80 keur for 10 nF)
- We have found the best compromise to increase C_dec as much as possible and reduce C_det to the minimum. **=>propose to freeze the current design of the SGFT and FE cards to proceed with their timely ordering.**