Review of Production ASIC Testing for ProtoDUNE Cold Electronics

Review Date: September 11, 2017
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Motivation for the Review:

The production order of front-end and ADC ASICs have been delivered to BNL. These ASICs will populate the front-end mother boards (FEMBs) for APAs #2-6. Five thousand of each chip type are in hand.

Given the experience of testing the first batch of chips (quantity ~400) we know that testing of this number of chips will be a daunting task. Cold testing the first 400 ADC chips proved to be difficult and inefficient due to reliability issues with the testing apparatus. It is recognized that significant improvements to the testing procedures need to be implemented before moving to the testing of the large quantities now in hand.

All chips will be tested warm. A fraction of front-end chips will be tested cold, while the current plan is to test all ADC chips that will be needed to populate the remaining motherboards, both warm and cold.

The focus of this review is to review and comment on the proposed plans and procedures for testing the large quantities of production front-end and ADC chips now available.

Preparation for the Review:

The BNL team was asked to present detailed plans and procedures for how the chips are being tested, including the handling and storage of the ASICs, from the point of their arrival at BNL through the testing cycles to the point of their final disposition (i.e. either assigned to an FEMB, or not).

Both the hardware and software tools that are being used in the testing process were to be presented, including plans for recording test results and the environment (i.e. test stand, test board, etc.) in which the chips are tested.

In addition, the plan for how the test results are analyzed and evaluated to select the chips to be used was to be presented.

Finally, plans for testing and certifying the completed FEMBs after the ASIC chips have been installed on them was also to be presented.

Goals for the Review

As an outcome of the review we want to be able to comment on the following:

- The team's ability to meet the required schedule for delivery of cold electronics for APA#2-6
- Quality Control in the testing procedure
- Efficiency of operations
- Environment, Safety and Health considerations

Review Presentations

Material presented at the review can be found at:

https://indico.bnl.gov/conferenceDisplay.py?confId=3560

Comments and Recommendations

The review committee commends the Cold Electronics team for the successful delivery and installation of the Cold Electronics boxes for APA#1. This is an important milestone for the project. We all look forward to the first results from operation in the Cold Box.

The testing shift schedule was presented. Shifts are run five days per week with three shift periods of four hours per day covering 12 hours. In addition to shifters, a shift leader is identified for each day from a pool of local experts to choreograph testing, execute the run plan, debug problems and maintain working test equipment. The committee supports this plan. We believe it supports both efficiency and quality control.

Testing procedures were available at each of the testing stations. The testing procedures are also available on the computer terminals to verify the latest revision. The committee recommends that the team consider developing and using a basic written checklist to guide shifters through the testing procedures. We feel that this is important when the shifters are asked to multi-task and rotate around a number of different testing stations.

The review committee supports the decision to have the testing of the front-end ASICs in the cold as well as the testing of the assembled mother boards being performed by the "expert" team members, rather than the routine shift teams. We believe this will produce the highest quality results for these elements of the system.

The committee was presented with the various databases that are being used to track the testing and history of the elements of the system, from ASICs through completed CE boxes. In general, the record keeping is good and the data appears to

be easily traceable, though we noted that it is distributed among three different systems: the master database, the spreadsheets on the testing stands and the e-log. All of these have valuable information and plans should be developed for preserving the information for the long term.

The committee was also presented with the testing procedures for the oscillators and flash memory (commercial chips) on the FEMB that are not designed for use at cryogenic temperatures. The committee feels that the testing plans and results for the oscillators and flash memory are in good shape.

The committee recommends that the team consider developing a control test that could be carried out on a regular basis (weekly) to ensure that the test stands and test boards, as well as operational procedures are remaining consistent in performance and outcome.

The committee observed a neat and well organized laboratory space. Safety procedures and use of PPE were being followed. Demonstrations at each of the test stands were given. We were happy to see that the "expert" testing stations were moved into a different laboratory, giving more room in the main testing area. The committee recommends that continuous effort be put into maintaining the organization of the space. If the MSU Cold Testing Stands are approved for use, testing space will need to be added to ensure there is adequate room to perform the testing with these additional test stands.

The committee noted that there could be an improved procedure for noting ASICs which have "bad pin" data after testing such that those chips not get ranked in the analysis, since they will not be selected anyway.

A plan to develop a new test board which incorporates a "socket in a socket" was discussed. The committee notes that this may be an improved test board, we encourage careful evaluation (perhaps using lower quality chips), prior to putting it into the production testing plan. The need for improved testing boards is understood and the committee noted that several improved board arrangements have been developed (horizontal board and quad board).

The committee noted that the plan for spares at the 20% level is good, and being implemented in the production and testing of the front-end motherboards (FEMBs), but recommends that this be propagated down into the chip testing numerologies.

The committee supports the testing plan that was presented whereby a quantity of ADC chips are tested up until the selection of 80 chips (for 10 FEMBs) are needed and those are then selected based on their Q-value ranking within the pool of tested chips.

Summary and Conclusions

The committee feels that the testing procedures and plans for producing the needed rate of tested chips for producing the FEMBs for the remainder of the ProtoDUNE APAs are now in place.

The shift teams are being staffed and the rate of testing appears to be adequate.

The documentation of the testing history appears to be in place via the database.

The laboratory space is organized and appears to be adequate for the testing procedures.

Recommendations noted during the review:

1. Develop a basic written checklist to guide shifters through the testing procedures to ensure procedural steps are not overlooked as the shifters move between multiple testing stations.
2. Develop a Records Management plan for the archiving of the master database, the spreadsheets on the testing stands and the e-log for preservation of the information.
3. Develop a control test that could be carried out on a regular basis (weekly) to ensure that the test stands and test boards, as well as operational procedures are remaining consistent in performance and outcome.
4. If testing capability is expanded with the use of additional MSU Cold Test Stands, add testing space to the lab to ensure there is adequate room to perform the testing.
5. Review the testing procedures for identification of ASICs which have “bad pin” data after testing such that those chips do not get ranked in the analysis, since they will not be selected anyway.
6. Prior to putting a new test board into production such as the planned new test board which incorporates a “socket in a socket” design, perform an evaluation to ensure the design will provide the expected results.

These recommendations are provided as opportunities for improvement and a response is not required.