DUNE's Noise & Trigger

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Noise, trigger and DAQ

- Detector performance and Readout Noise shape the DAQ and trigger architecture.
- Two classes of triggers:
  - **Deterministic** triggers that might not need of L1 (online) trigger and they could be done in offline with full event reconstruction like : a) Beam b) Calibration and c) random triggers and so on.
  - **Non-Deterministic** triggers that might need to be done in L1 (online) trigger (primitive and farm):

    a) Supernovae trigger, low energy events that back ground physics are issue, long buffer

    b) Proton decay and Atmospherics Muon triggers, high-energy events (with help of Photodetector info). Short buffer.
  - Depends on where (Front/Back-end DAQ) and on what platform (FPGA/GPU/CPU) we want to run the algorithms, they could be significantly different in both code and algorithms.
  - ***There are a tremendous trade-off and interdependence between Noise ⇔ Trigger Alg ⇔ DAQ architecture (more detail in Giles' talk and internal note*** **DUNE-doc-4481** ***)***

Noise implementation and trigger Alg

1. The noise performance and level of DUNE TPC are not very well known and they might change during years of operation. So We are modelling the all possible noise sources and **implement dynamic noise adding through in analysis** rather than Mc level (except Physics background).
2. Implementing trigger algorithms only for **Collection plane** (960 /APA) because they higher S/N ratio and reduces needed processing resources.
    1. Hit finding with induction plate seems a little difficult due to variation of noise then threshold level.
3. Implementing the FIR filter and signal processing before generating trigger primitives to study the effect of the filter in trigger performance.
4. In further steps, We are considering implementing geometrics dependent noise (coherent noise; HV noise, and DC2DC convertor and cross talk effect)
5. We need a quick estimation for resources needed for trigger for architecture design
    - We already have some number for FPGA but nothing GPU (Oxford working on it right now)

Table 4.2: Parameters of the four planes of wires on an APA

Label	Function	Orientation (from vertical)	Pitch (mm)	Number	Bias Voltage (volt)
G	Shield/grid plane	0°	4.79	960	−655
U	1^{st} induction plane	+35.7°	4.67	800	−365
V	2^{nd} induction plane	−35.7°	4.67	800	0
X	Collection plane	0°	4.79	960	+860

Back up slides

SuperNova Trigger primitives (Oxford scheme)

- We propose **Trigger primitives (FPGA based) and local event buffer** architecture based on Distributed Trigger Processing Farm (DTPF) to reduce the data stream rate. The DTPF performs a number of processing tasks on both front-end DAQ and back-end DAQ with time tagged frames to select candidate events and create trigger signal and information.
- Trigger primitives and ring buffer; Supernovae trigger, Requires maximum 10 seconds. Roughly **125GB** for a full event buffer scheme (no compression, no tag/headers)

- 10s buffer is independent of how fast our algorithm detect a SN event.
  DAQ has a bandwidth limit that force buffering all SN before sending off detector
- Design is based on Cold-electronics' specs; **what if it's removed**?