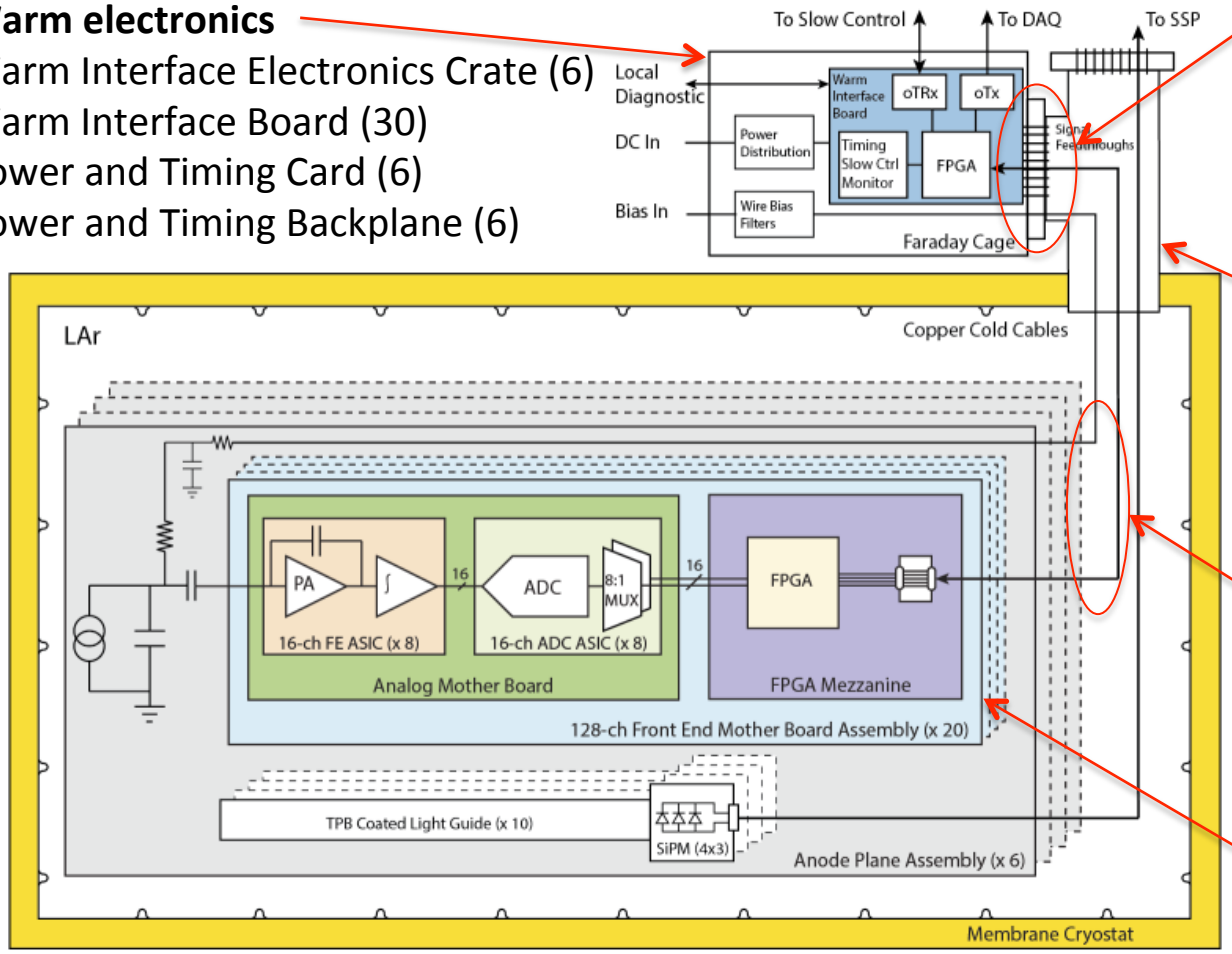
protoDUNE-SP CE Status Report

Matthew Worcester (BNL)
representing the protoDUNE CE team

DUNE Cold Electronics Consortium Meeting
9/18/17

ProtoDUNE-SP Cold Electronics

Warm electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable to FEMB
LV and data cable (120+120) and APA wire-bias SHV cable (48)

Front End Motherboard
(FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

Scope

Table 2.6: Electronics components and quantities

Element	Quantity	Channels per element
TPC	1	15,360
APA	6	2,560
Front-End Mother Board (FEMB)	120, 20 per APA	128
FE ASIC chip	120 × 8, 8 per FEMB	16
ADC ASIC chip	120 × 8, 8 per FEMB	16
FEMB FPGA	120, 1 per FEMB	128
Cold cable bundles	120, 1 per FEMB	128
Signal flange	6, 1 per APA	128 × 20 (i.e., 2,560)
CE feedthrough	6, 1 per APA	128 × 20
Warm interface boards (WIB)	30, 5 per APA	(128 × 20) /5 (i.e., 512)
Warm interface electronics crates (WIEC)	6, 1 per APA	128 × 20
Power and timing cards (PTC)	6, 1 per APA	128 × 20
Passive backplane (PTB)	6, 1 per APA	128 × 20
LV power mainframe	2	7,680
LV supply modules	6, 1 per APA	128 × 20
Wire-bias mini-crate	2	7,680
Wire-bias supply modules	6, 1 per APA	128 × 20

FE ASIC

- ~5mW/channel for long lifetime
- 16 independently programmable channels
  - 4 gains: 4.7, 7.8, 14, 25 mV/fC
  - 4 shaping times: 0.5, 1, 2, 3 µs
  - 2 baselines: 200 mV/900 mV
  - Analog test output
  - 6 bit internal DAC for calibration
- 2012 design of Front End (FE) ASIC deployed in multiple LAr TPCs:
  - MicroBooNE (**ENC ~400e-**), CAPTAIN, LArIAT, 35-ton, ARGONCUBE@Bern, ICARUS 50l TPC@CERN
- 2 subsequent revisions:
  - P1 version tested at MSU/BNL since July 2016
  - 268 P2 FE ASICs tested at BNL for APA1 in June/July
    - Selected 200 for APA1
  - 5000 production FE ASICs received at BNL at the end of July

Bandgap Reference

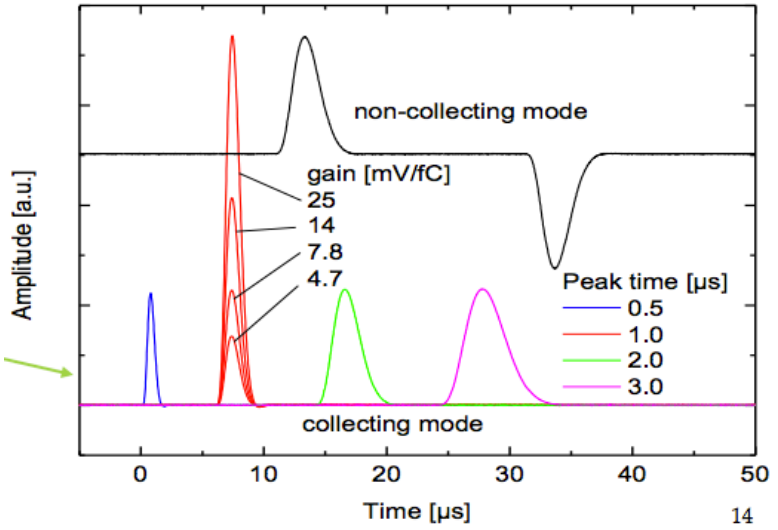
$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{at}\ 300\ ^\circ K \\ 1.164\ V \ \text{at}\ 77\ ^\circ K \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{at}\ 300\ ^\circ K \\ 259.3\ mV \ \text{at}\ 77\ ^\circ K \end{cases}$$

~ 2.86 mV / °K



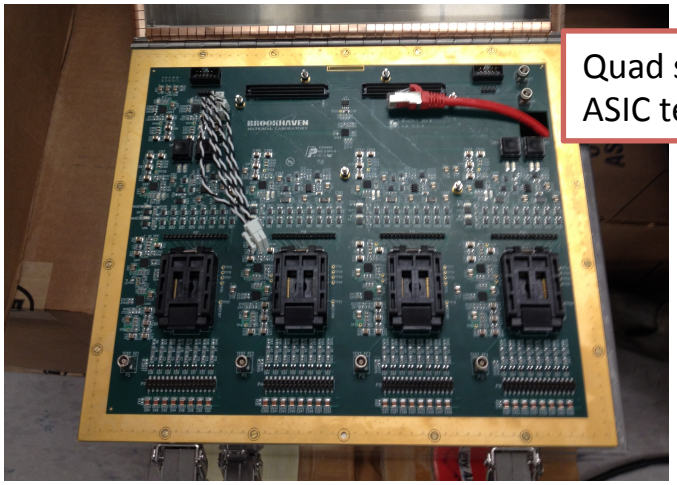
Datasheet: DUNE Doc 1484

FE ASIC QC Plan

- Strategy
  - Every FE ASIC will be tested at RT
  - Cryo yield will be measured with ~10% of the ASICs prior to FEMB assembly
  - All FE ASICs will be tested in LN2 under 2+ thermal cycles on assembled FEMB

  CE QA/QC Electricals Plan Dune DocDB 1809
- Criteria for passing:
  - All 16 channels functional at every setting in Table 2
  - Internal FE DAC functional at all 64 amplitudes, all channels
  - Selection cuts for uniform FE response
    - Rejects ~4% of the chips
- Quad socket FE ASIC testboard schematics

  Dune DocDB 3345
- All test results stored in CE QC database
  - Tracked from standalone testing to FEMB assembly and testing

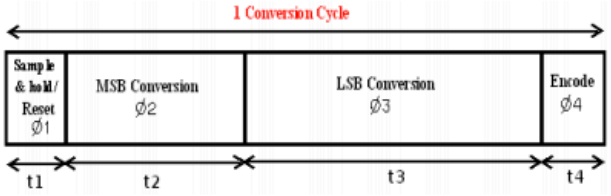


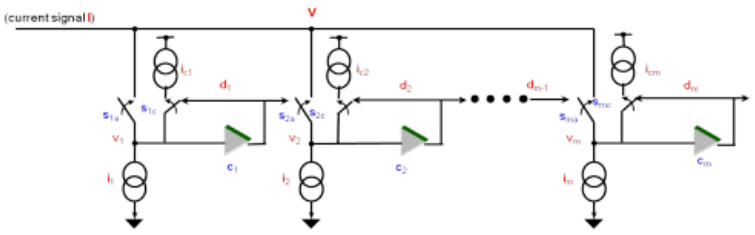
Quad socket FE ASIC testboard

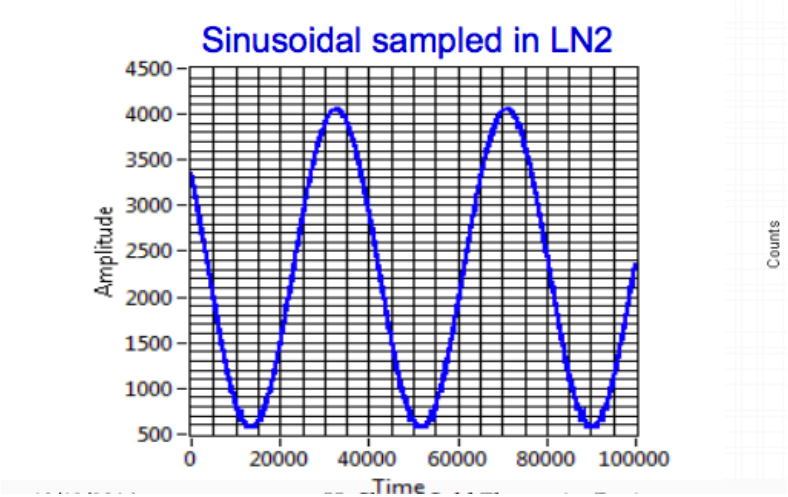
Parameter	Values	# of test cycles	Channel/ Global
Gain	4.7, 7.8, 14 and 25 mV/fC	4	CH
Filter peaking time	0.5, 1, 2, and 3 μs	4	CH
Baseline	200/900 mV	2	CH
Test capacitor	enable/disable	2	CH
Coupling	AC/DC	2	CH
Buffer	enable/disable	2	CH
Channel 1 setting	signal/monitor monitor = temperature or bandgap	3	GL
Leakage current	0.1, 0.5, 1.0, 5.0 nAmp	4	GL
Analog out	enable/disable	16	CH

Table 2: Summary of P2 FE ASIC parameter test cycles.

ADC ASIC







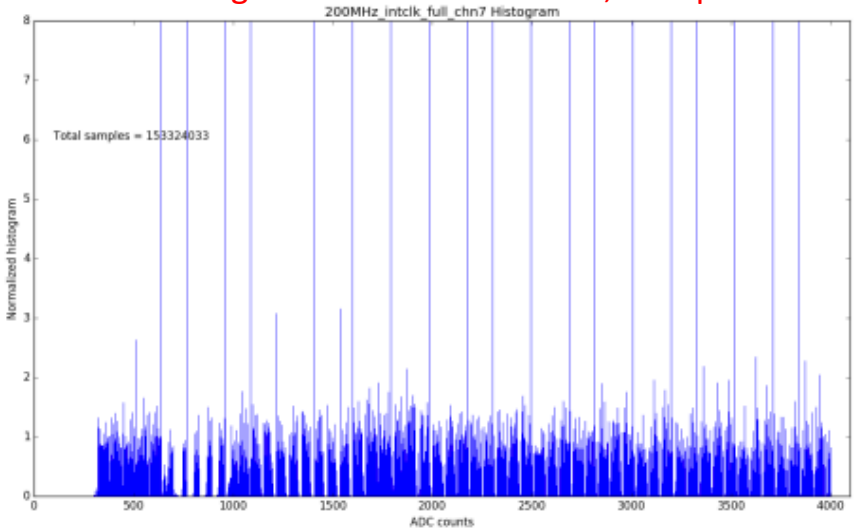
- ~5mW/channel for long lifetime
- Current-mode domino architecture with 4 phase operation
- 16 programmable channels
- 12 bit ADC up to 2 MHz internal or externally-applied sampling clock
- 2014 version of ADC ASIC deployed in 35-ton prototype
  - Stuck codes observed
  - All high-speed digitized data links (2048 channels) functioned in LAr
- 2 subsequent revisions
  - V* ADC tested at BNL since Jan 2016
    - Used to qualify FEMB prototypes up through P2 FEMB
  - 395 P1 tested and ranked for quality
    - Selected 200+ for APA1
  - 5000 production ADC ASICs received at BNL at the end of July

Datasheet: DUNE Doc 1485

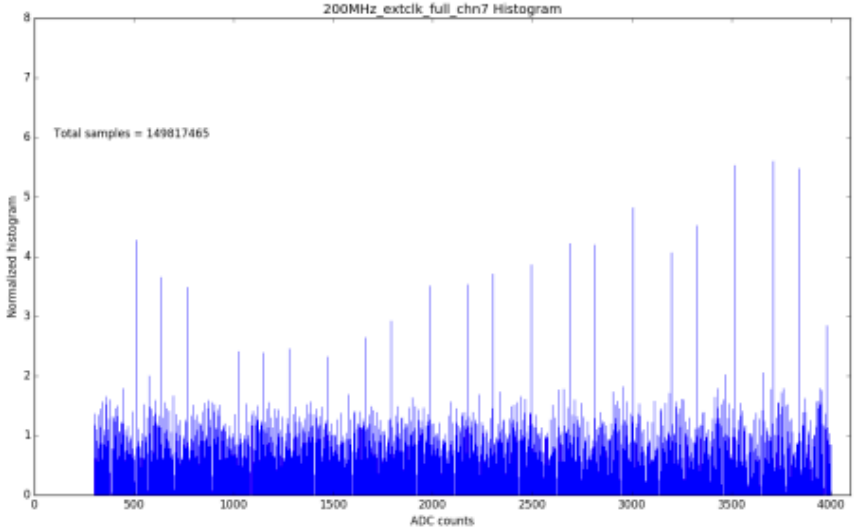
P1 ADC DNL "stuck codes"

- Test ADC with a high-precision ramp voltage in LN2:

Using 200 MHz internal clock, 2 Msps



Externally generated 200 MHz clock, 2 Msps

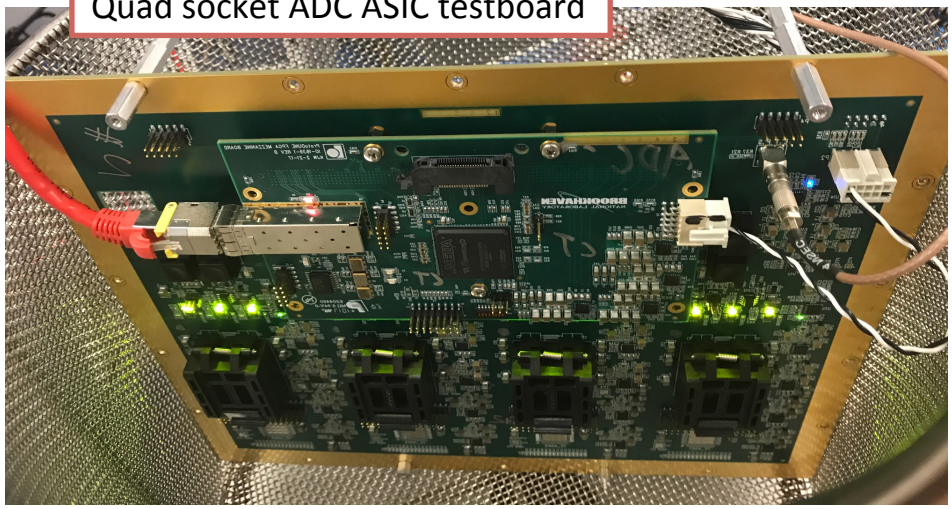


- Preferred operation mode of P1 ADC has been established
  - Full steering current
  - External control clocks
  - AC coupling with bias to eliminate low ADC range

ADC ASIC QC Plan

- Every ADC ASIC will be tested at RT and in LN2 prior to FEMB assembly
  CE Electricals QA/QC Plan Dune DocDB 1809
- Criteria for passing (Table 3):
  - ADC functional with internal/external clock sources for all channels
  - Preferred operation mode with FE ASIC input functionality OK
  - External ramp test
- ADC ASIC testboard schematics
  - Single and quad socket
  Dune DocDB 3345
- All test results stored in CE QC database
- ASICs will be selected from ranking and assembled onto FEMB
  - FE & ADC ASICs for APA1 were selected by end of July
  - FE & ADC ASICs for APA2-3 will be selected by end of September

Quad socket ADC ASIC testboard

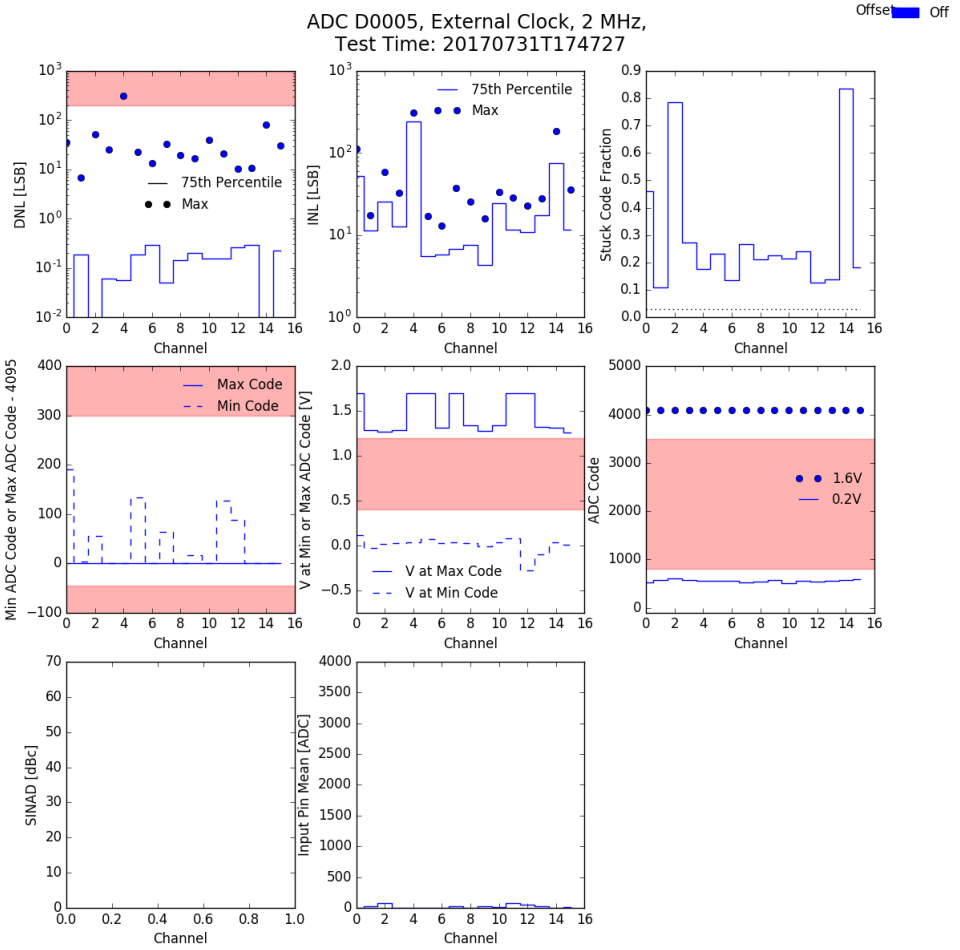


Source	Values/Test	# of test cycles
Digitize clock	external 1.0 and 2.0 MHz internal	4
FE ASIC	multiple FE ASIC settings normal operation of ADC	32
External ramp	Stuck code, saturation, roll-back, & linearity	1

Table 3: Summary of ADC ASIC parameter test cycles.

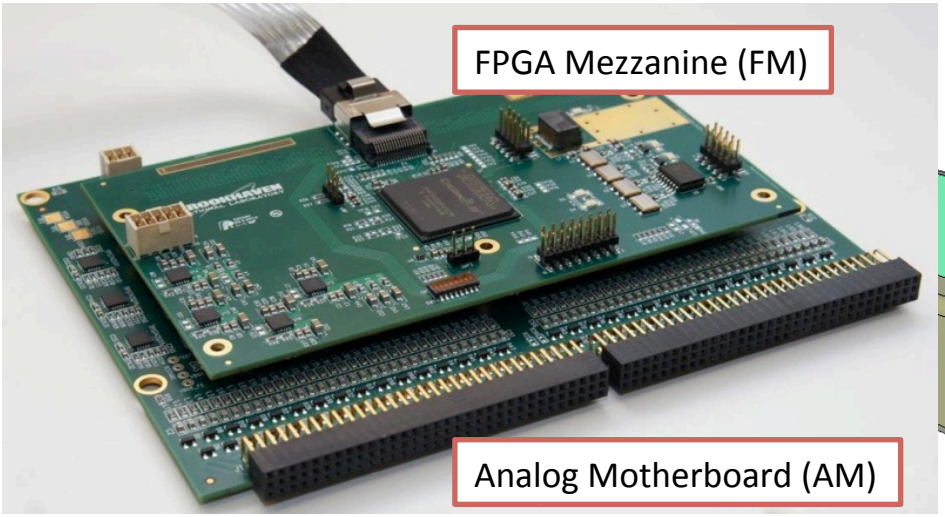
ADC Functionality Tests

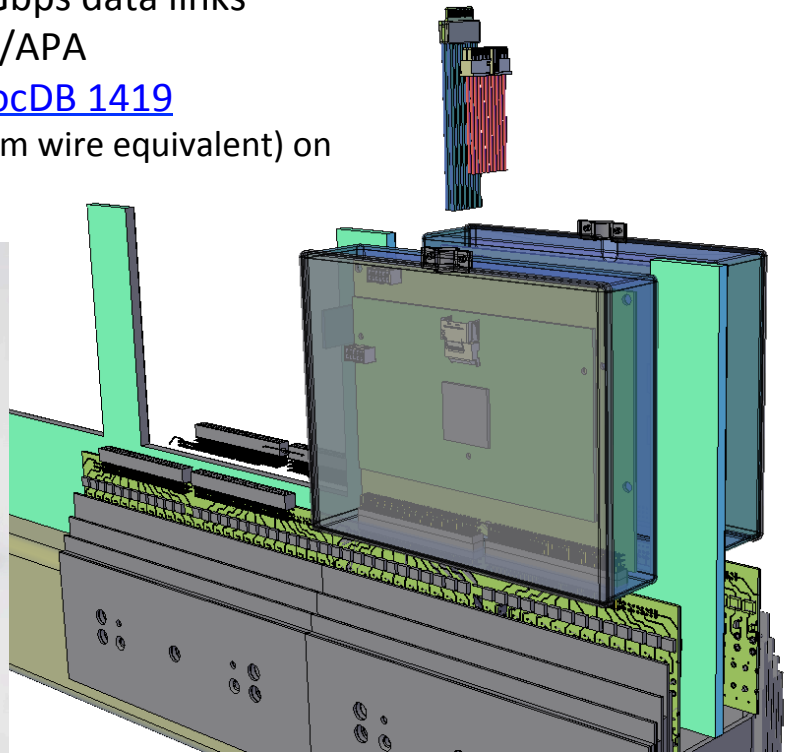
- ADC tests performed on QC teststand
  - Setup and check
    - Synchronize ADC warm and test
    - After ADC is in LN2, take external ramp data prior to resynchronizing chip
- Full test in LN2
  - Power cycle and synchronize
  - External ramp data
  - Internal and external clocks at both 1 and 2 MHz, all channels
    - DNL and INL
    - Stuck code fraction
    - Minimum and maximum ADC codes
    - Vin at min and max codes
  - Enable and check input pins
- Already selected 80 ADCs for 10 FEMBs from production chips
- Have enough ADCs tested with good performance to select remainder for enough FEMB for APA2



FEMB

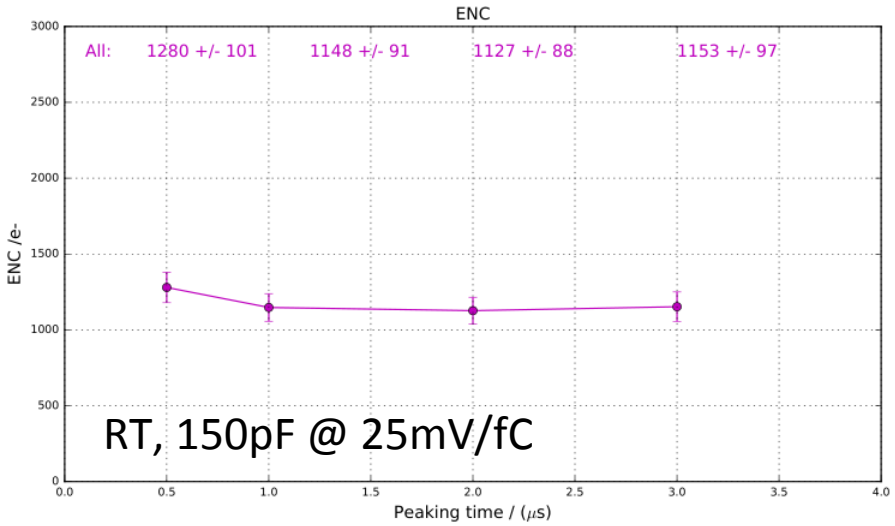
- 128 channels of digitized wire readout on 4x1 Gbps data links
- FEMB individually enclosed in CE Box: 20 FEMB/APA
- FEMB schematics, layout, and BOM in DUNE DocDB 1419
  - Includes toy TPC which enables 150 pF load (~7m wire equivalent) on all 128 FE channels

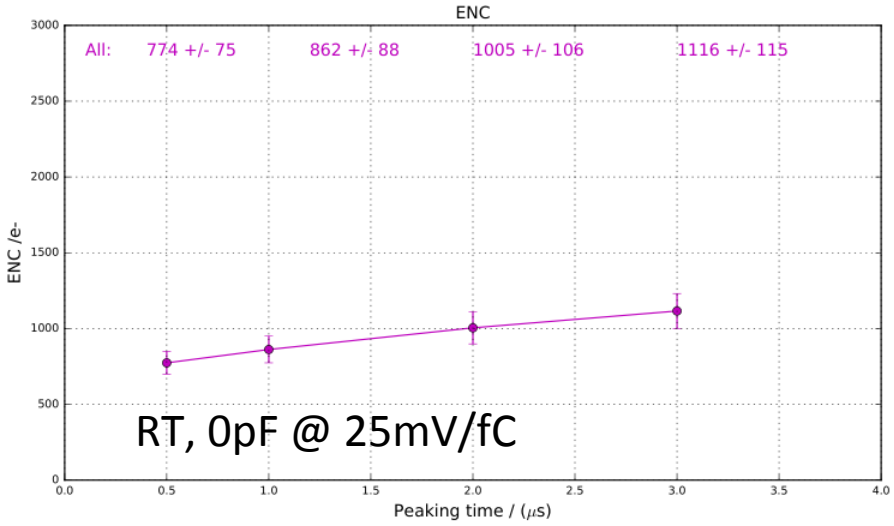


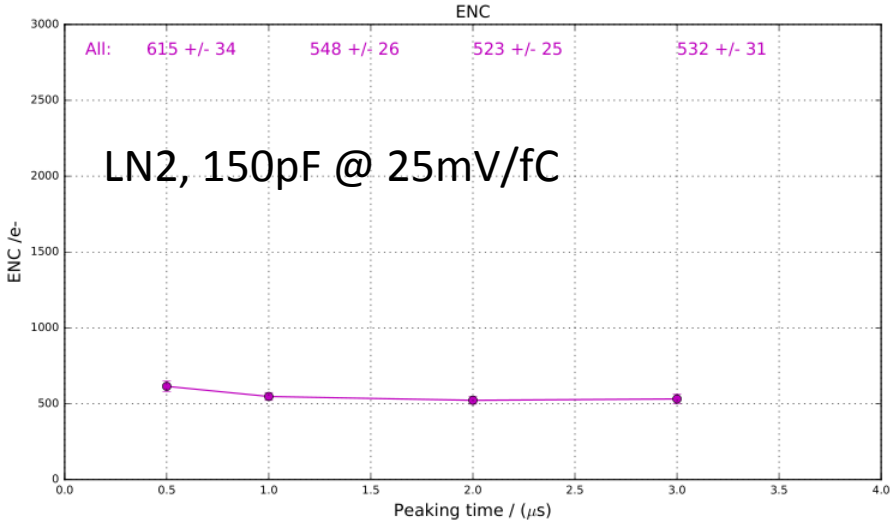


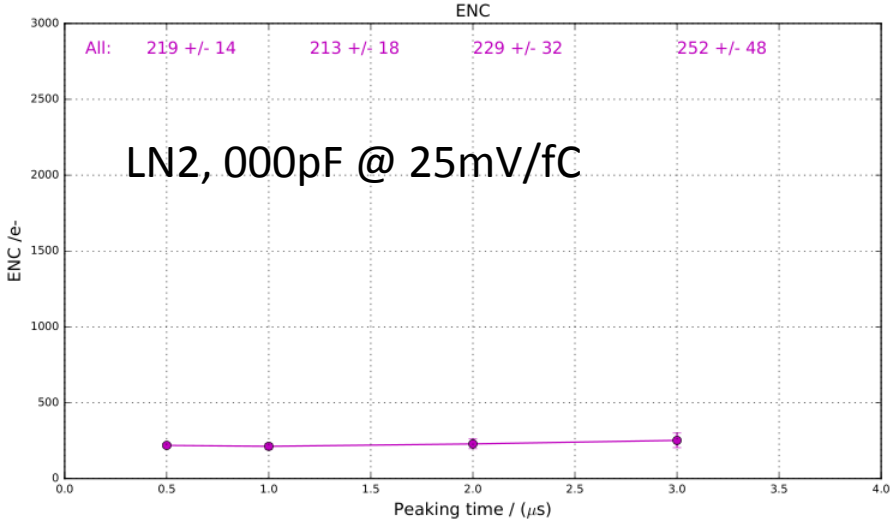
- Extensive testing with P1 FEMB (P1 FE/V* ADC) aka “SBND prototype”
- 25 P2 FEMB assembled for APA1 and tested in August
  - Includes flash memory and oscillator pre-screening
  - 23 selected to ship to CERN for APA1: all results stored in QC database

protoDUNE FEMB ENC Performance









FEMB QC Plan

4.1 Functionality

To validate the functionality requires testing the following features of the FEMB both at room temperature and under multiple thermal cycles in LN2:

- successful loading of the FPGA programming from the onboard EEPROM;
- ability to program the FPGA and EEPROM over the backup JTAG links in the cold data cable bundle;
- ability to set the control registers on the FPGA via the I^2C control IO links;
- confirmation that the backup onboard oscillators can generate the clock for the FPGA state machine in case the clock from the system is lost;
- confirmation that the FPGA can configure all 16 ASICs on the analog motherboard via SPI interface and synchronize the data from all serial links from the ADCs (either 16:1 or 8:1 multiplexing on each ADC ASIC);
- verify that in the state with all ASICs configured, the current drawn by the CLR for all LV power inputs are nominal, indicating the FPGA is programmed and ASICs operational;
- confirmation that all channels observe both the FPGA internal pulser and an external pulser with the FE test capacitor enabled;
- confirmation that all channels observe the FE ASCI internal pulser;
- successful transmission of all digitized waveform data over all 4 ~1.2 Gbps links at sufficiently low Bit Error Rate (BER).

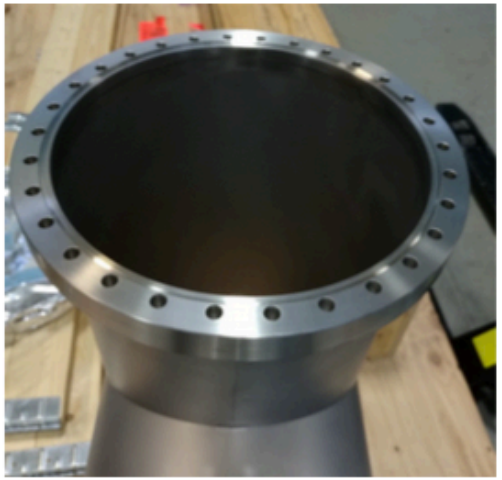
- FEMB are delivered to BNL from vendor
  - Visually inspected and cleaned upon reception
- All FEMB will be pre-tested in LN2 to reject/replace bad components
  - Functionality tests + repeat ASIC QC testing
- Selected FEMB will be “dressed”
  - Installed in CE Box with mounting hardware
  - Mechanical procedure in DUNE DocDB 2611
- FEMB + cable + adapter are final unit and each one will be individually retested in LN2
  - Connection from adapter socket to FEMB input checked with toy TPC
  - Criteria to pass QC:
    - Full suite of FEMB QC passed: functionality, noise characterization, ADC response (DUNE DocDB 1809)
    - No visible stress damage or loose hardware after return to room temperature
  - Results stored in QC database
- Warm reception tests done at CERN
  - Prior to APA installation
    - Identical femb_python analysis as during QC tests at BNL
  - Results to be stored in QC database

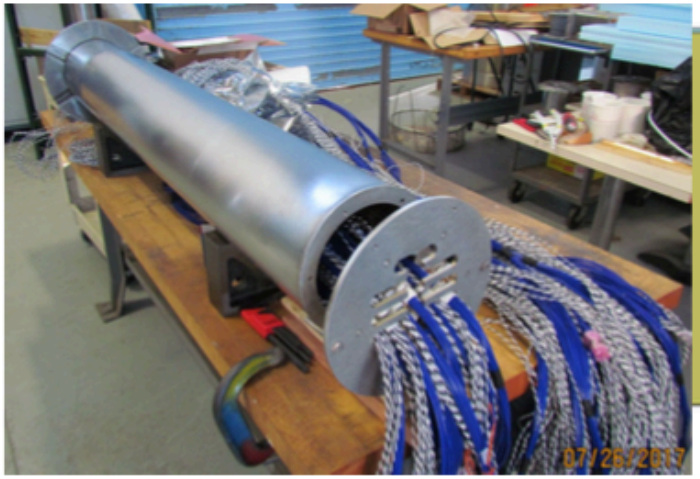
MSU Cryogenic Test Systems

- Cryogenic Test System (CTS) developed by MSU
  - Developed to protect electronics test boards and ASICs/FEMB
  - Increase ease of operation and safety for shifters over dunking in open-top dewars
  - First prototype delivered to BNL in June
- Many safety upgrades required by BNL safety after preliminary review
  - Implemented by MSU in July/Aug
- Safety walkthrough at BNL on August 10th
  - Review of complete documentation and operation procedure
    - Manual available in BNL lab
  - Further list of safety features required by BNL safety
- Expect delivery to BNL of first approved CTS by end of September

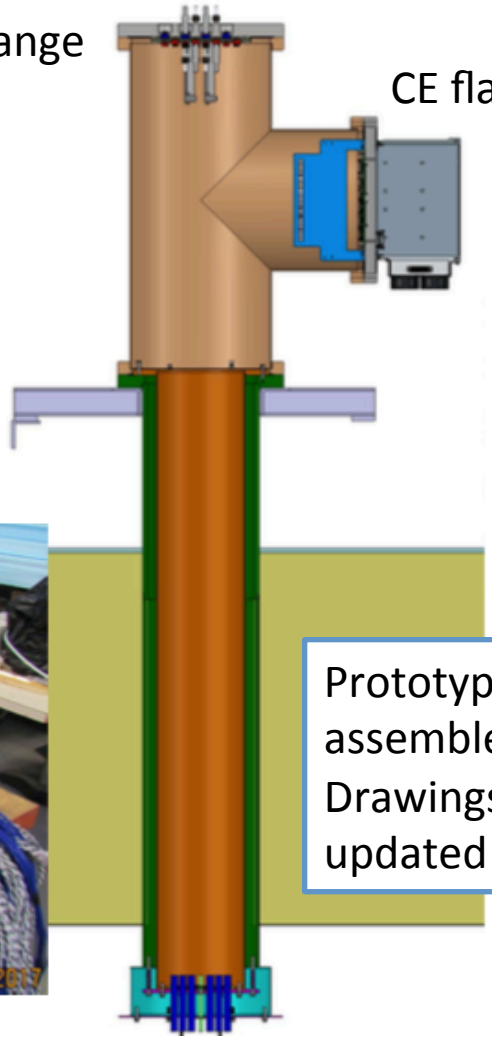
Signal Feed-through

- 2 major mechanical components:
  - Tee pipe
    - 14” Conflat flanges to attach PD and CE feed-through flanges
  - Crossing Tube Cable (CTC) support
    - Inner tube controls GAr flow through feed-through
    - Provides cable strain relief at lower end of cryostat crossing tube without touching tube



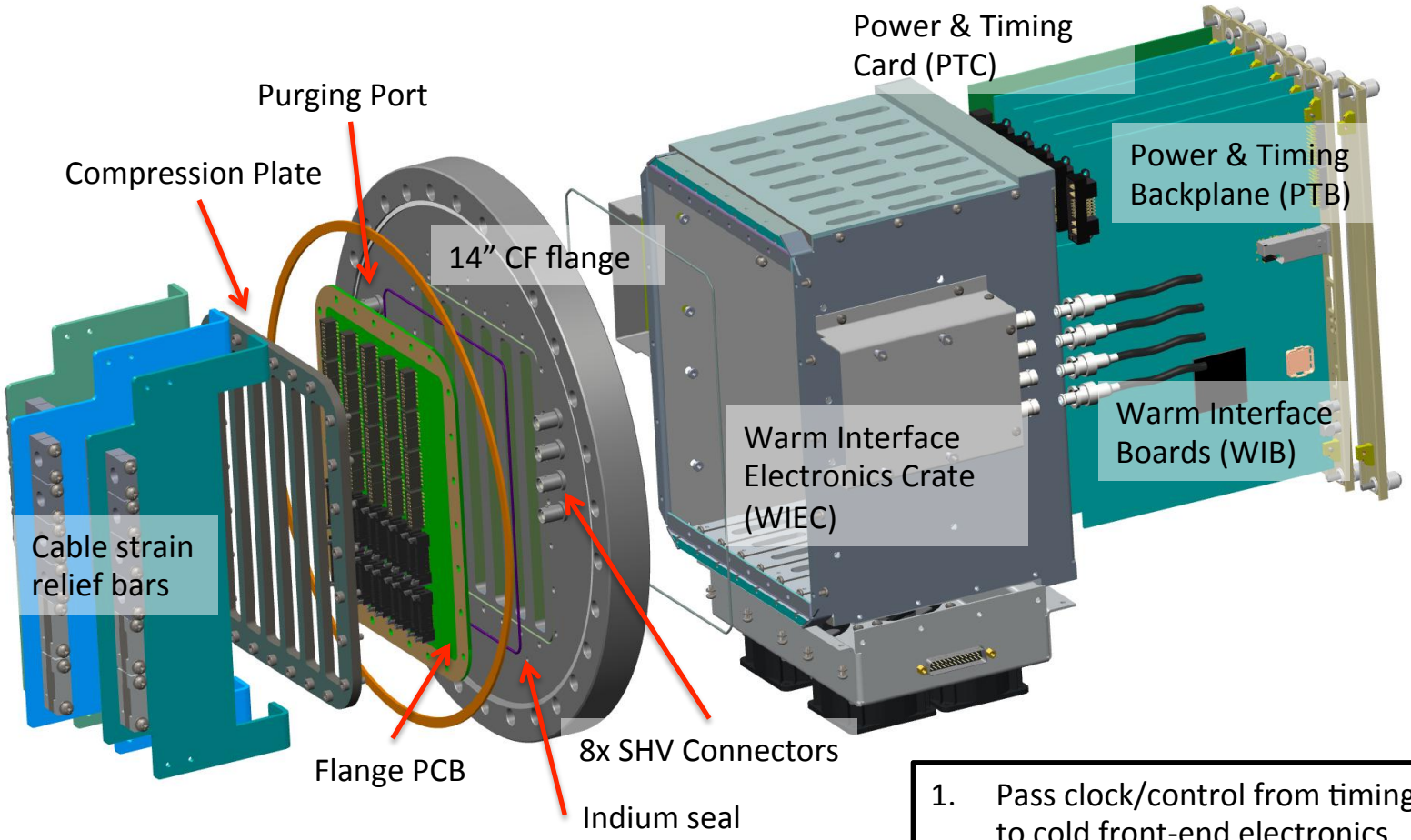


7 Tee pipes at BNL, 1 installed at CERN



Prototype CTC assembled at BNL
Drawings being updated

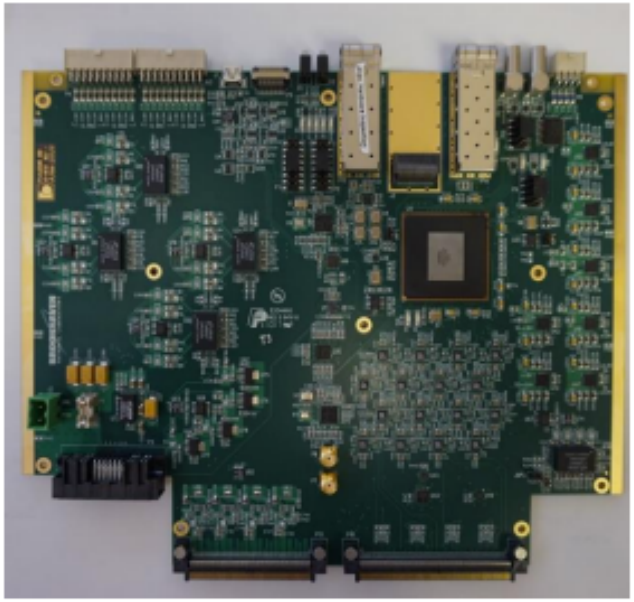
CE Warm Components



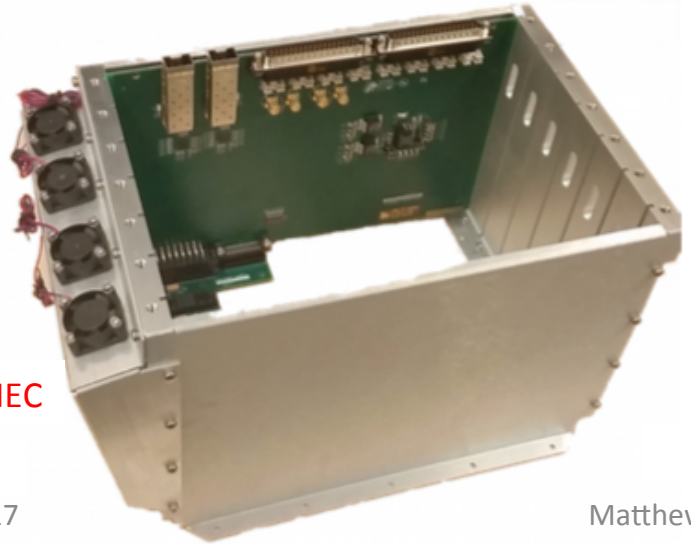
1. Pass clock/control from timing system to cold front-end electronics
2. Deliver high-speed TPC wire data from cryostat to DAQ

3. Connection to detector ground at CE flange
4. Pass wire-bias and FC HV to cryostat

WIB/PTC



V1 WIB

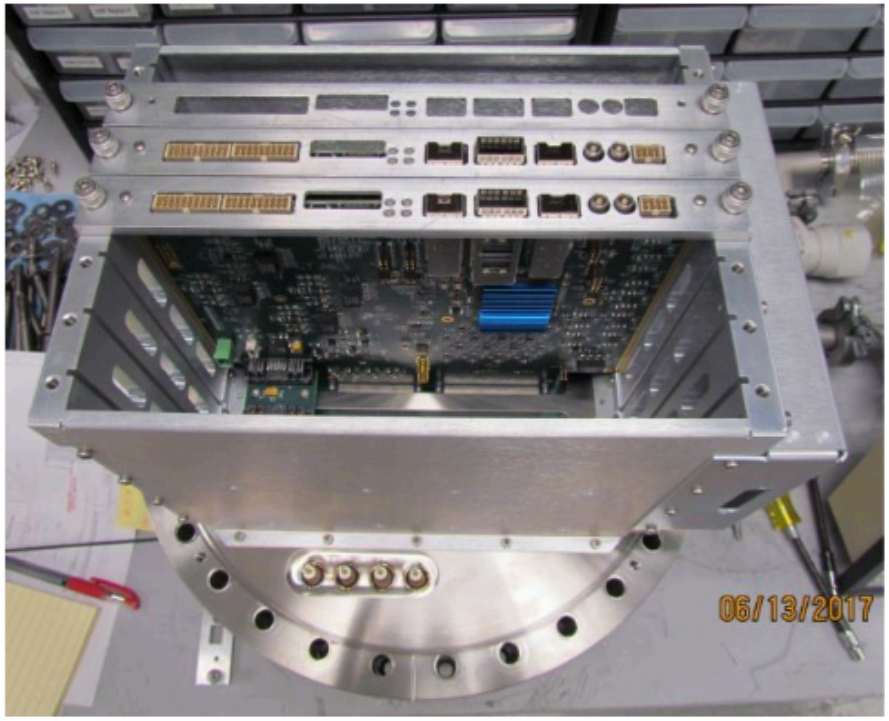


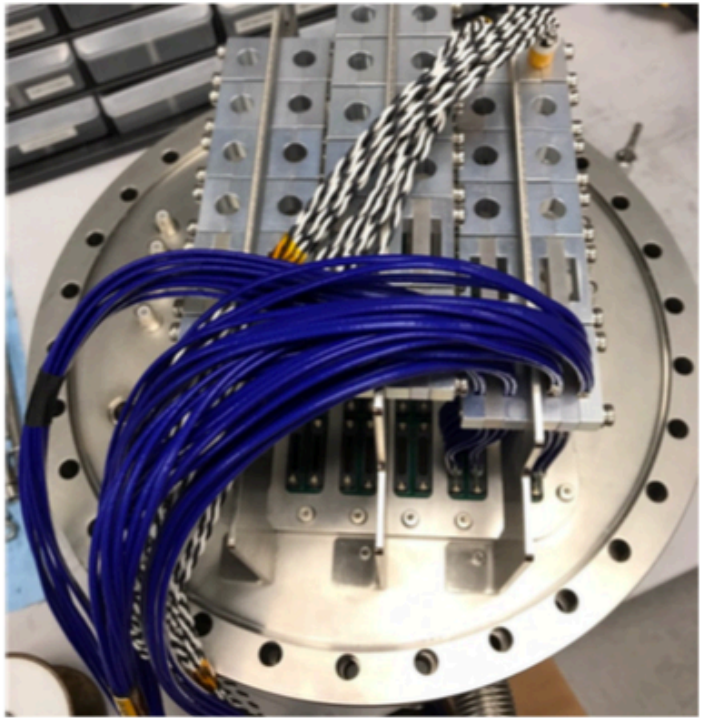
V1 PTC in WIEC

- protoDUNE V2 WIBs being tested at BNL
  - Arria V GT variant FPGA
  - ProtoDUNE clock/data separator
- Testing with V1 WIB
  - Boston University
    - WIB-RCE links working via optical fiber
    - Firmware works with Bristol timing system
  - BNL
    - Hardware and 10 Gbps link checks done
  - CERN
    - WIB-FELIX links almost working
- P2 version PTC layout complete and posted to DUNE Doc 2988 (UC Davis)
  - 2 variants for 2 options for 48/12V DC converter
    - V2-A: with Vicor "Cool Power" Pi3546
    - V2-B: with Linear Tech. LTM8064
  - 1 of each at BNL and 1 of each at CERN

CE Flange and WIEC

- CE flange: provides electrical connection from cold cable to warm electronics and cable strain relief
- Warm Interface Electronics Crate: RF shielding for warm electronics, only connections outside of crate via optical fiber





Complete flange and WIEC assembly built at BNL and installed at CERN

Prototype Milestones

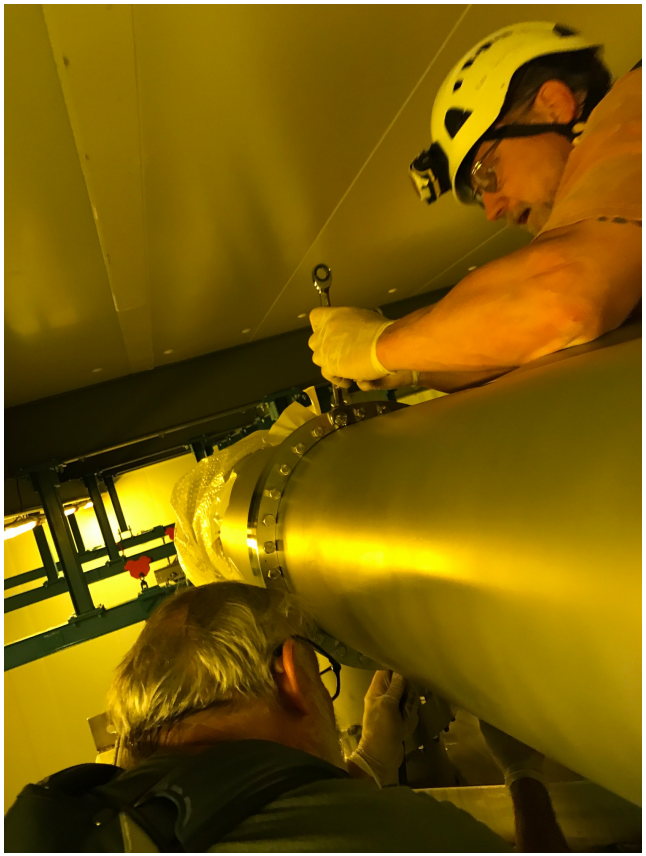
✔ = complete since last update

Prototype Development		Design	Fabrication	Test
Cold Electronics	FE ASIC	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ✔
	ADC ASIC	P1 ✔	P1 ✔	P1 ✔
	FEMB AM	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ✔
	FEMB FM	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ✔
Cold Cable	Data	✔	✔	✔
	Power	✔	✔	✔
Signal Feed-through	Flange	✔	✔	✔
	Flange PCB	✔	✔	✔
	WIEC	✔	✔	✔
Warm Electronics	WIB	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ongoing
	PTB	✔	✔	✔
	PTC	P1 ✔ P2 ✔	P1 ✔ P2 ✔	P1 ✔ P2 ongoing

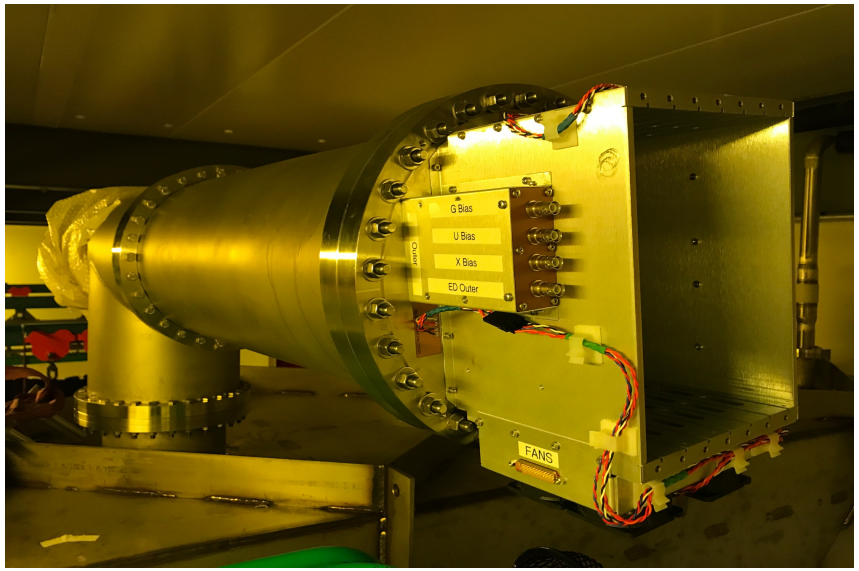
APA1 Installation

- CE Team at CERN:
  - BNL: Hucheng Chen, Jack Fried, Shanshan Gao, Augie Hoffman, Ken Sexton, Elizabeth Worcester, Matt Worcester, Manhong Zhao
  - Collaborators: Jake Calcutt (MSU), Casandra Morris (Houston), Justin Hugon (LSU), Martin Tzanov (LSU), Kevin Wood (SBU)
- Received, re-assembled, and tested 23 CE boxes
- Installed and tested 20 CE boxes on APA1
- Installed Tee, flange, and hardware on cold box
- Other:
  - Incorporated WIB into vertical slice test and interfaced with DAQ and timing experts
  - Assisted with APA and PD installation tasks
  - Tested LV and wire-bias HV mainframes and modules

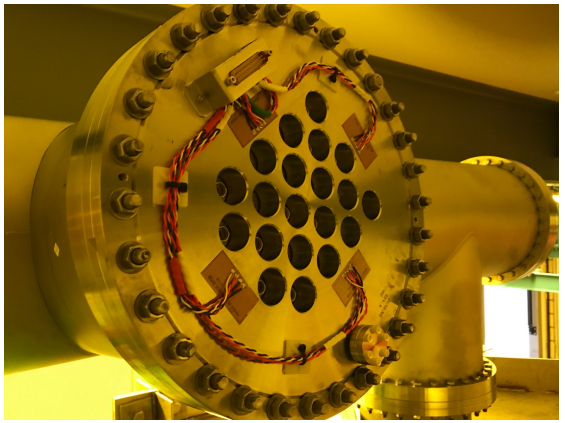
Installation on Cold Box



Tee pipe

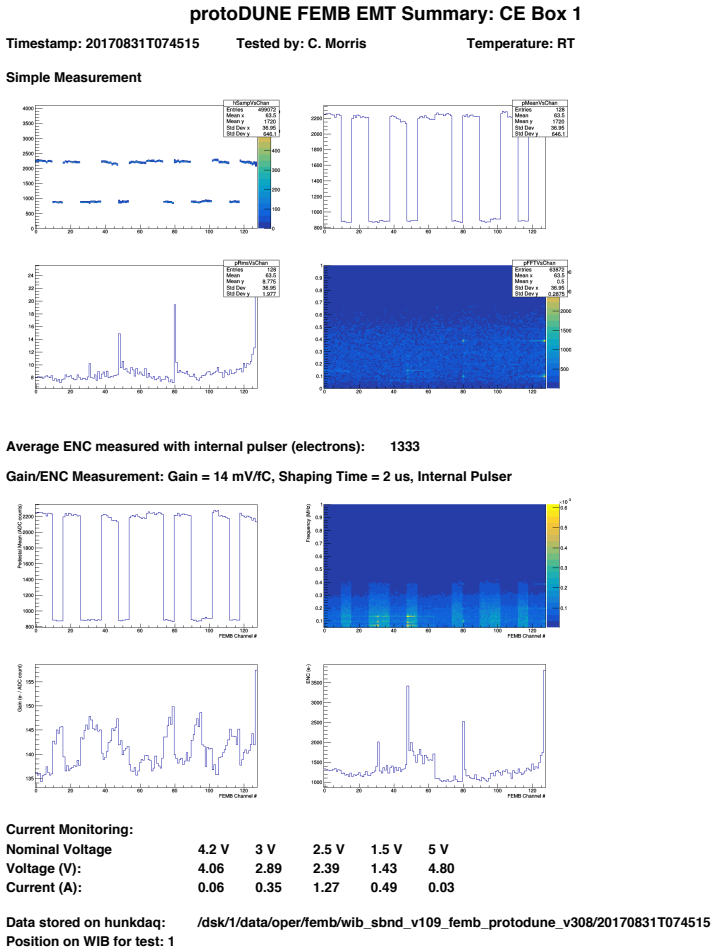


Flanges



Warm Test Results on Bench

- Boxes are fully tested at BNL, then cables are disconnected and shorting caps attached for shipping. Upon arrival at CERN, BNL techs reassembled all the boxes
- Casandra Morris adapted our testing software for a "quick check" baseline and gain measurement using the mobile test stand
  - Boxes and cables unshielded – don't expect identical performance to BNL test results – see pickup in noise plots
  - Purpose is verify no new bad channels (warm) after shipping/reassembly or installation
- Observed no damage to boxes/cables from shipping/reassembly – only one "bad" channel in the warm is ok in the cold and was observed both at BNL and CERN



“Bad” Channel

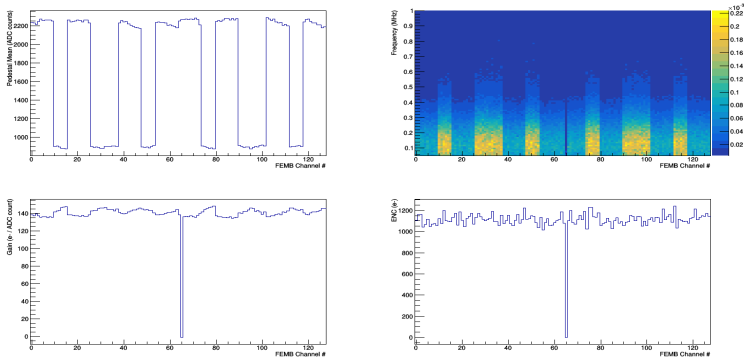
protoDUNE FEMB QC Summary: CE Box 9

Timestamp: 20170816T160403 **Tested by: Brian Kirby** **Temperature: RT**
Analog MB ID: 3 **FPGA Mezz ID: 32**
FE ASICS: 147,163,154,159,141,173,190,198
ADC ASICS: 373,206,96,95,334,64,1,3

Average ENC measured with internal pulser (electrons)

	0.5 us	1 us	2 us	3 us
14 mV/fC	1740	1254	1106	1128
25 mV/fC	1983	1558	1426	1452

Gain/ENC Measurement: Gain = 14 mV/fC, Shaping Time = 1 us, Internal Pulser



FEMB power cycled 5 times at beginning of data collection with no failure.

Current Monitoring:

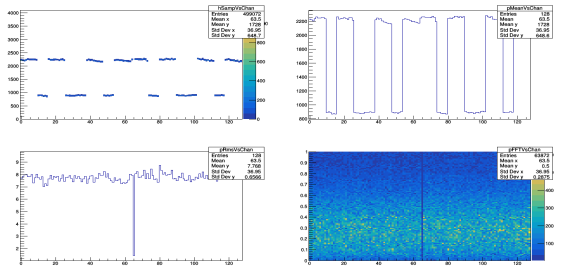
Nominal Voltage	4.2 V	3 V	2.5 V	1.5 V	5 V
Voltage (V):	4.06	2.89	2.40	1.44	4.80
Current (A):	0.06	0.35	1.28	0.49	0.03

Data stored on hothdaq1:
/dsk/1/data/oper/femb/wib_sbnd_v109_femb_protodune_v308/20170816T160403
Position on WIB for test: 1

protoDUNE FEMB EMT Summary: CE Box 9

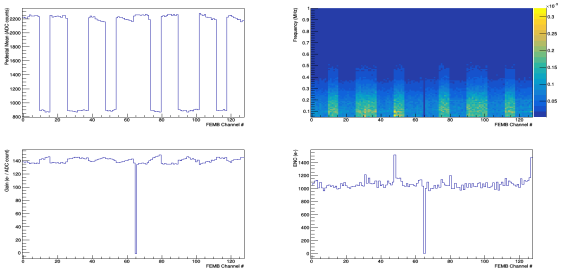
Timestamp: 20170831T092647 **Tested by: E. Worcester** **Temperature: RT**

Simple Measurement



Average ENC measured with internal pulser (electrons): 1059

Gain/ENC Measurement: Gain = 14 mV/fC, Shaping Time = 2 us, Internal Pulser



Current Monitoring:

Nominal Voltage	4.2 V	3 V	2.5 V	1.5 V	5 V
Voltage (V):	4.06	2.89	2.39	1.43	4.80
Current (A):	0.06	0.35	1.26	0.48	0.03

Data stored on hunkdaq: **/dsk/1/data/oper/femb/wib_sbnd_v109_femb_protodune_v308/20170831T092647**
Position on WIB for test: 1

BNL

CERN

Installing on APA1

The first Box

Manhong

APA1 CE Performance

- Out of 2560 channels:
  - One previously known bad channel in warm (ok in cryo at BNL)
  - One open channel – determined to be upstream of CE
  - One box with three bad FE channels – was replaced, replacement all channels ok
- Cold box operation expected late September / early October

Date	APA # [1-6]	APA Side [A, B]	APA Slot # [1-10]	WIB Slot # [0-3]	FEMB # [1-25]	Channel # [0-127]	ASIC # [1-8]	Note	Entered in Hardware DB
9/1/17	1	B	1	0	10			All channels OK	Y
9/5/17	1	B	2	3	25			replace FEMB24 with FEMB25,. All channels OK	Y
9/1/17	1	B	3	2	9	65	5	1 bad channels at RT, which is known to be good at LN2	Y
9/4/17	1	B	4	1	11			All channels OK	Y
9/4/17	1	B	5	0	3			All channels OK	Y
9/4/17	1	B	6	2	12			All channels OK	Y
9/4/17	1	B	7	3	16			All channels OK	Y
9/4/17	1	B	8	1	21			All channels OK	Y
9/4/17	1	B	9	3	7			All channels OK	Y
9/4/17	1	B	10	2	4			All channels OK	Y
9/5/17	1	A	11	2	1	123	8	bad channel: the connection between FE input and wire is open	Y
9/4/17	1	A	12	1	17			All channels OK	Y
9/4/17	1	A	13	2	20			All channels OK	Y
9/4/17	1	A	14	3	13			All channels OK	Y
9/5/17	1	A	15	0	8			All channels OK	Y
9/5/17	1	A	16	1	2			All channels OK	Y
9/5/17	1	A	17	2	15			All channels OK	Y
9/5/17	1	A	18	3	23			All channels OK	Y
9/5/17	1	A	19	0	5			All channels OK	Y
9/5/17	1	A	20	1	14			All channels OK	Y

CE Milestones

- APA
  - FEMB for APA1 (installed Sept 1 – 5)
    - Tested ~400 and selected 200+ ADCs from first lot by late July (LN2 testing June 15 - July 29)
    - Assembled and tested 25 FEMB in August (tested from Aug 4 - 23)
    - 20+ FEMB shipped to CERN by the end of August (received on Aug 30 and 31)
  - FEMB for APA2-3 (projected to install in early December)
    - Test 1000+ and select 400 ADCs from production lot by end of September (started testing July 31: 2 months)
    - Assemble and test 50 FEMB by mid-November (1.5 months)
    - 40+ FEMB ship to CERN by the end of November
  - FEMB for remaining APA
    - Depends on APA4-6 schedule
    - Test enough ADCs for next FEMB selection by end of November (2 months)
    - Assemble and test next FEMB by end of January (2 months)
    - Ready to ship FEMB to CERN by mid-February

CE Milestones

- Cryostat
  - Received Tee pipes at BNL and checked
  - Receive and test CE flanges and WIEC at BNL in early October
  - Install feed-throughs (Tee + CTC) on cryostat in late November
  - Move APA1 inside cryostat in late November
  - CE flange + WIEC assembly install on Tees in early December
  - Production WIB/PTC install in WIEC in early December
  - Move APA2 inside cryostat in late December
- Cold Box
  - Delivered V1 WIB to CERN for vertical slice in late June
  - Components shipped to CERN in late July (arrived Aug 15)
  - Full prototype Flange + WIEC assembly install in late August (work done on Sept 1 and 4)
  - Deliver V2 WIB/PTC for installation in WIEC by end of September

Summary

- protoDUNE-SP requires ~10x more ASICs and FEMB than previous prototypes
- QC testing for production FE, ADC, and FEMB ongoing
  - 20 good FEMB plus spares delivered for APA1
- We are in good shape for APA2-3
  - ADC testing should have enough good chips by end of September
  - Warm electronics for cold box will ship this month
  - Mechanicals for cryostat will be ready before APAs need to be cabled