DAQ Hardware and Interfaces Working Group

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DAQ Consortium Meeting

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Scope

- Define and Document interfaces to SP and DP sub detectors
  - Where no currently agreed interface exists, work to define one — e.g. TPC readout
- Research and document unit costs for hardware components
  - FPGAs, links, memory, boards / crates / power / cooling, network equipment
  - Lead to the initial system costing in Technical Proposal (early) 2018
- Explore suitable modularity of DAQ hardware
  - How many boards, where, how much power, how many links → informed by architecture options

Interaction with other WG

- Interacts both ways with Architecture working group
  - Technical feasibility informs architecture choices
  - Limited number of “sensible” architectures informs search region for hardware

- Interacts both ways with SP TPC, SP Photons, DP TPC, SP Photons
  - Need to understand their technical constraints
  - Need to communicate our technical constraints once we know them.
  - Many will not be hard constraints but rather cost/performance choice
  - Need to avoid being handed a “fait accompli” that leads to global misoptimization by pushing difficultly away from front end towards DAQ
    - Need the material for an informed discussion.

Interfaces – SP TPC

- Optimum interface depends on architecture
- Needs urgent work – interface to cold ASIC
- Different schemes:
  - "Passive WIB" - electrical→optical conversion only. FPGAs that aggregate onto 10/40 Gbit/s links are elsewhere
  - "Multiplexing/Aggregating WIB" receives multiple links from cold electronics and aggregates onto 10/40 GBit/s links
  - "DAQ on WIB"
    - FPGA receives data
    - Buffers
    - Sends "trigger primatives" to data selection system
    - Performs data compression

Interfaces – SP Photon Detectors

- ADCs in the warm
- Sample rate much higher than for TPC
- Information much more compressable
  - Possible, in principle, to reduce to a list of photon arrival times
- Otherwise similar decisions to the SP TPC
- Possibility of common hardware and hence interface to DP Photon system

Interfaces – DP TPC

- Dual Phase TPC currently has a micro-TCA based system
  - ADCs + FPGAs on AMCs , mounted on cryostat
  - Higher signal to noise than in SP makes this less risky
- Data transmitted from MCH (“crate controller”).
- DP proposes to do some limited compression and send Ethernet packets to the DAQ
  - Everything else is DAQ
  - Is this (globally) the best solution ?

Interfaces – DP Photon Detectors

- Seems to be more flexibility than for DP TPC
- Amount of effort available in front-end team may be limited.
- Common hardware? (… and hence common DAQ interface)

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Interfaces – Data Selection

- Driven by architecture
  - Mainly FPGA / Mainly CPU / Mixed / Entirely CPU?
  - “Trigger” objects
  - Links
  - Latency

Hardware

- Tightly linked with architecture (and via them to DAQ simulations)
- Xilinx / Altera-Intel ?
- FPGA / CPU / GPU comparison (processing, I/O , ….)
- Buffering?
  - Probably driven by supernova trigger
    - e.g. Few seconds of RAM to allow trigger decision to be made followed by few minutes of flash storage?
- Try to benefit from previous experience
  - Micro Boone
  - Icarus
  - Won't have input from protoDUNE in time for technical report. Will have in time for TDR (?)

Summary

- Aiming to provide the evidence to perform some evidence based decisions ….
- We only have a few months to narrow down to a few options
- Leads on to implementation.