A New ADC for DUNE

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Task Force Conclusions (presented in May)

- A new 12-bit 2 MSPS ADC should be developed.
- Excellent integral and differential non-linearity are required
  - ADC should contribute very little to effective noise even at the low gain setting of LArASIC.
- The new ADC should use a proven architecture.
  - Σ–Δ, SAR, or pipeline.

Study Group led by Carl Grace

- Carl Grace, Dan Dwyer (LBL), Hucheng Chen, Emerson Vernon(BNL), Grzegorz Deptuch, David Christian (FNAL)
- 8 meetings held 8/15 – 10/2
- Context:
  - DUNE Executive Committee has decided that the development of a new ADC should be a collaborative effort “to avoid a possible single point of failure.”
  - We have discussed a BNL-FNAL-LBL collaboration with Carl Grace as lead engineer.
  - It is important to DUNE that the first iteration of the new ASIC works well.

IC Technology and ADC Architecture

- Our study confirmed the conclusion that any of the three architectures (Σ–Δ, SAR, or pipeline) could be successful.
- We initially considered both 180nm and 65nm CMOS, but quickly focused on 65nm CMOS because it promises better performance.

Pros & Cons

- Σ–Δ:
  - Does not require calibration or exquisite matching in analog circuits,
  - But these attractive features are balanced by risk associated with the complex logic required to implement a sinc^3 digital decimation filter, the need for a fast settling buffer, and by the need for very careful clock generation and routing to avoid clock overlaps at LAr temperature.
- SAR:
  - Conceptually the simplest of the 3 architectures, also lowest power.
  - But, requires moderately complex calibration logic (example considered includes an iterative least squares fit).

Pros & Cons (continued)

- Pipeline
  - Highly tolerant of comparator offsets and uses lowest clock speeds.
  - Requires calibration, but logic is relatively simple (& can use a bootstrap procedure to calibrate the most significant bits using the least significant bits)

Conclusion

- We will develop a calibrated pipeline ADC using 65nm CMOS.
- Carl Grace will be the lead engineer.
- The design will be done as a BNL-FNAL-LBL collaboration.

- Study Group slides & minutes are available in DUNE-doc-5675