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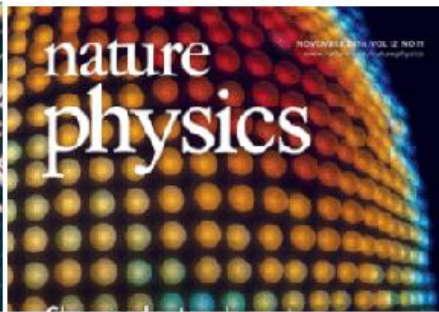
Presentation Title — one line or two lines

Presenter's Name

Meeting Title

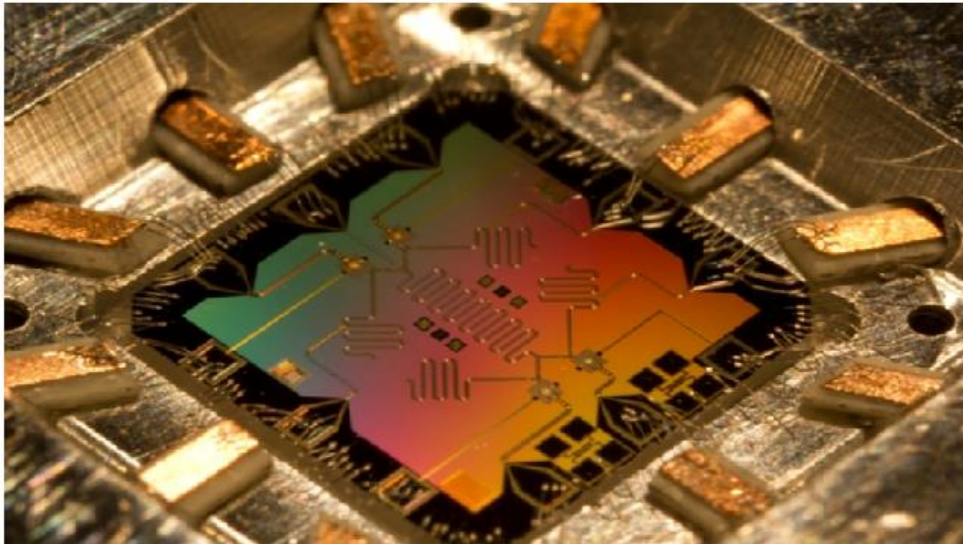
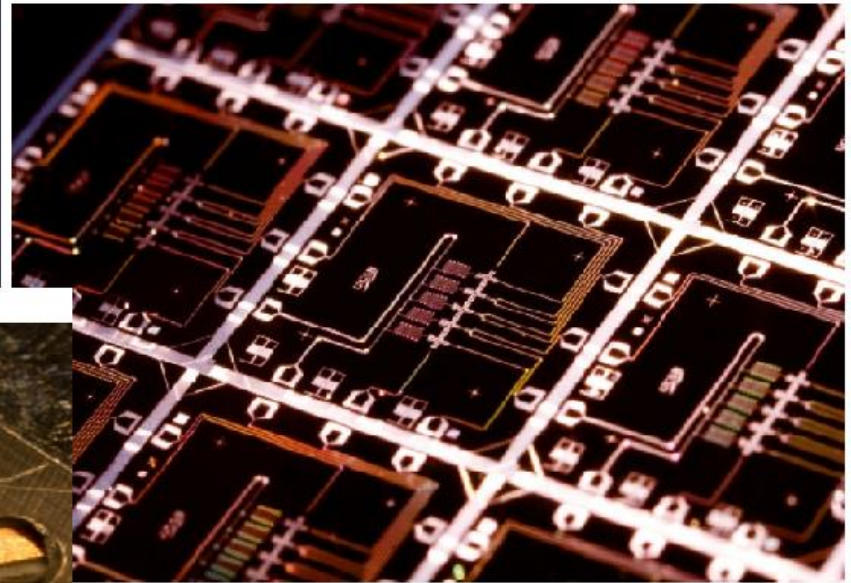
Day Month Year

Superconducting qubits



Superconducting Qubits featured by the BBC

Superconducting circuits at the surface code threshold for fault tolerance



This photo by Erik Lucero illustrates our lab's ReZQu qubit architecture, the focus of a [BBC article](#).

AAAS Science "Breakthrough of the year"

- One of the most promising technologies for quantum computing

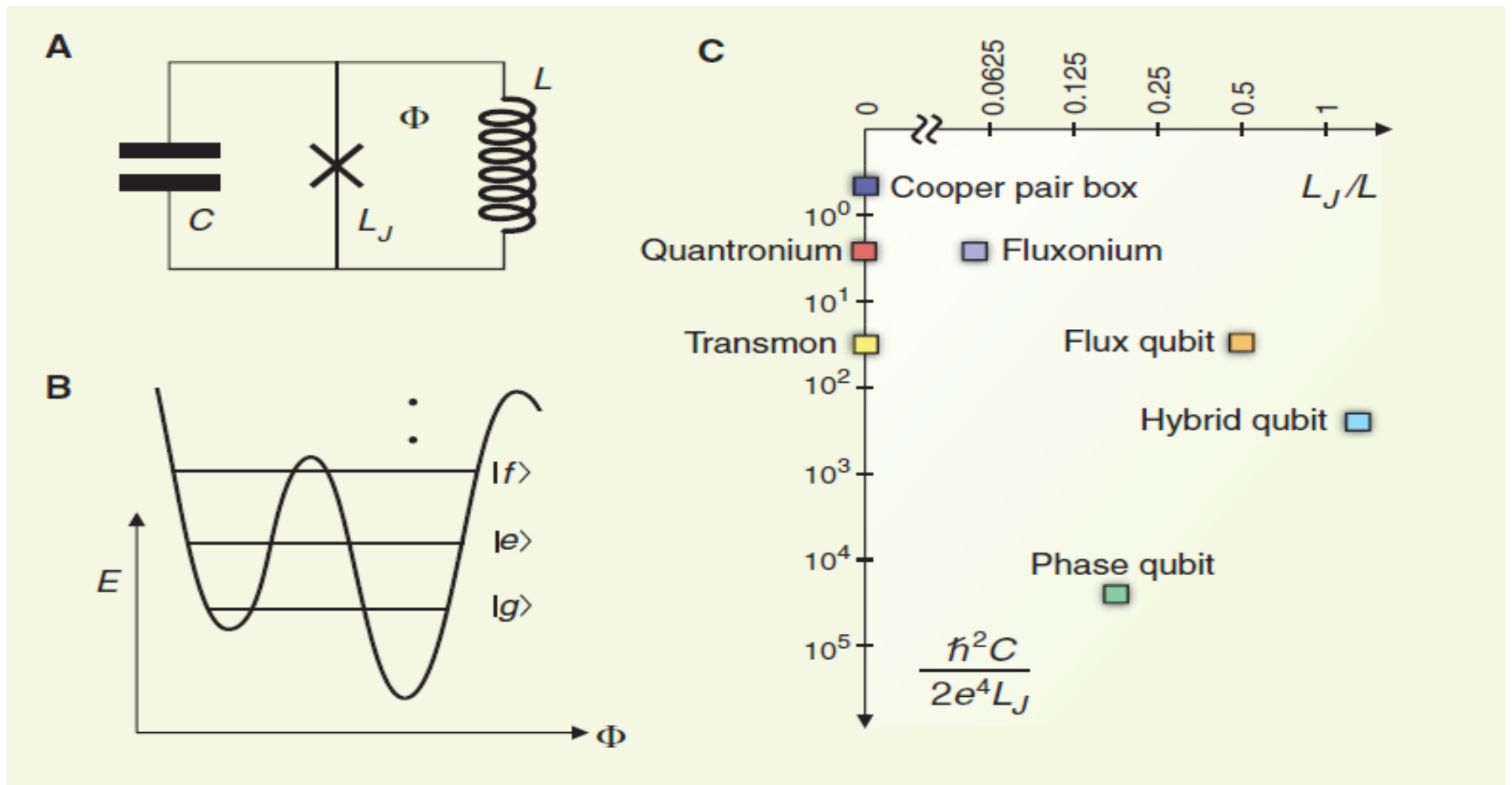


Fig. 2. (A) Superconducting qubits consist of simple circuits that can be described as the parallel combination of a Josephson tunnel element (cross) with inductance L_J , a capacitance C , and an inductance L . The flux Φ threads the loop formed by both inductances. (B) Their quantum energy levels can be sharp and long-lived if the circuit is sufficiently decoupled from its environment. The shape of the potential seen by the flux Φ and the resulting level structure can be varied by changing the values of the electrical elements. This example shows the fluxonium parameters, with an imposed external flux of $1/4$ flux quantum. Only two of three corrugations are shown fully. (C) A Mendelev-like but continuous "table" of artificial atom types: Cooper pair box (29), flux qubit (33), phase qubit (35), quantronium (37), transmon (39), fluxonium (40), and hybrid qubit (41). The horizontal and vertical coordinates correspond to fabrication parameters that determine the inverse of the number of corrugations in the potential and the number of levels per well, respectively.

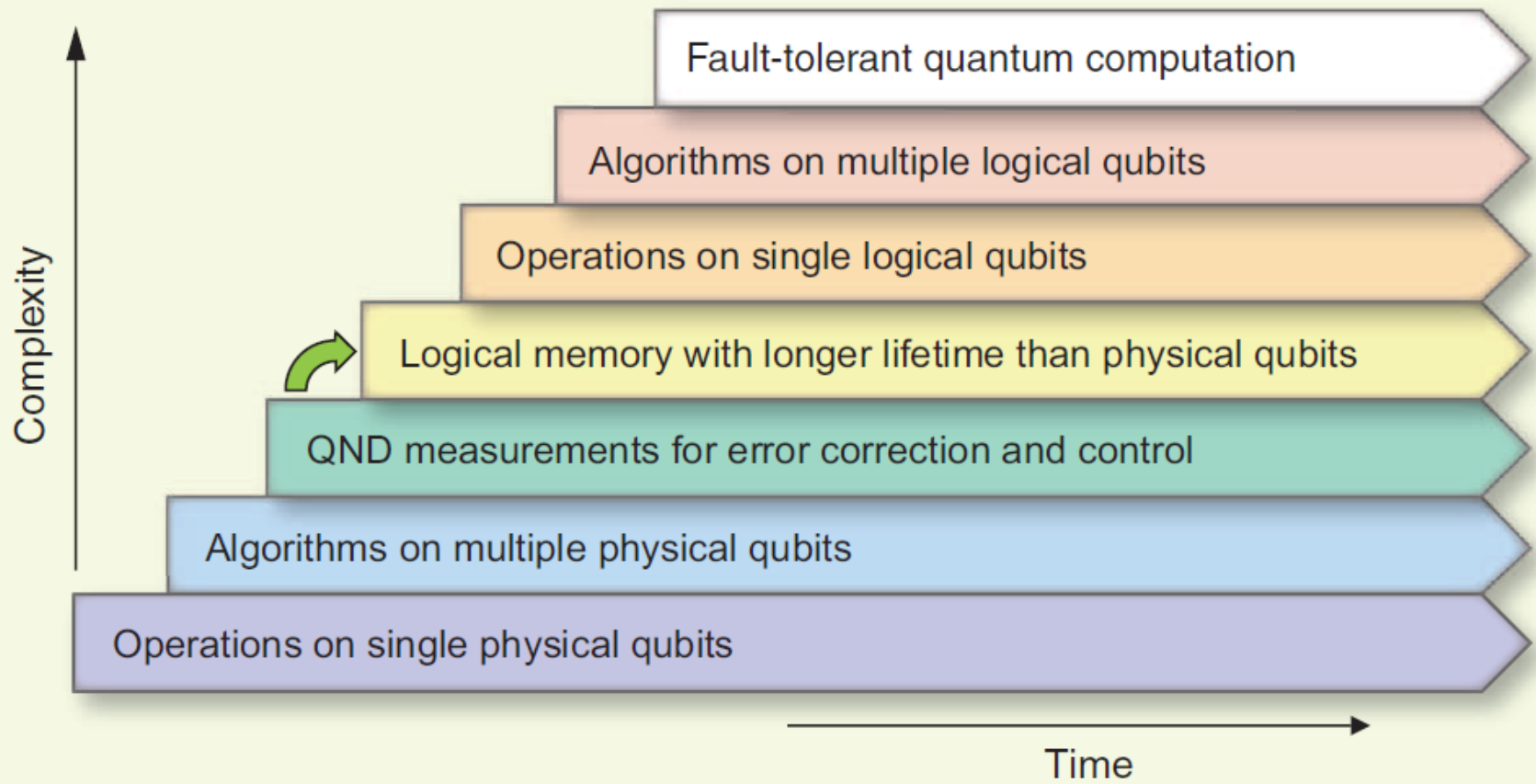
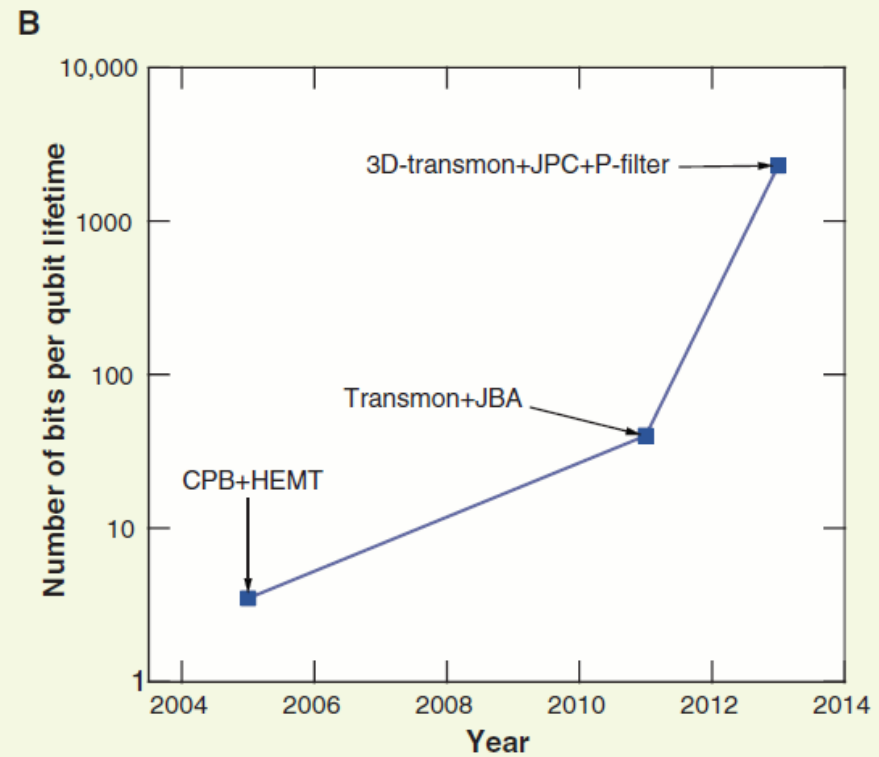
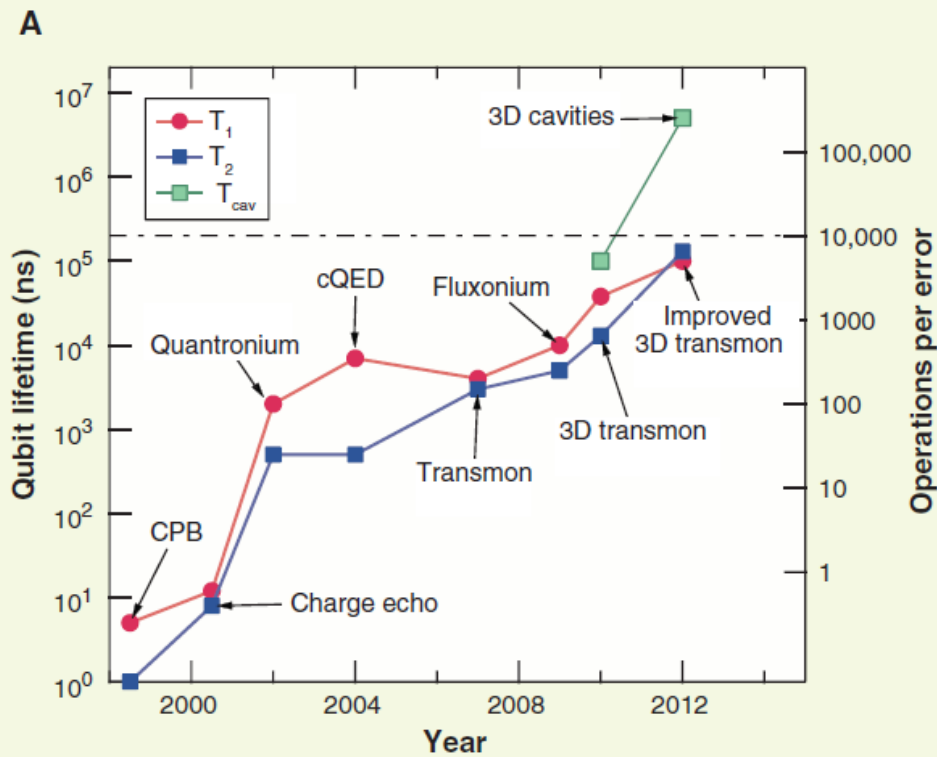
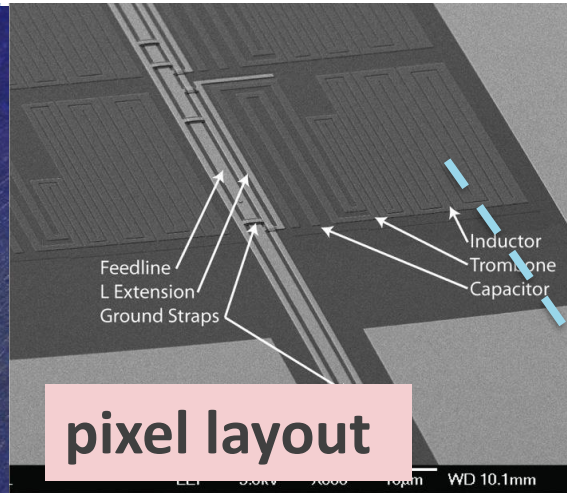


Fig. 1. Seven stages in the development of quantum information processing. Each advancement requires mastery of the preceding stages, but each also represents a continuing task that must be perfected in parallel with the others. Superconducting qubits are the only solid-state implementation at the third stage, and they now aim at reaching the fourth stage (green arrow). In the domain of atomic physics and quantum optics, the third stage had been previously attained by trapped ions and by Rydberg atoms. No implementation has yet reached the fourth stage, where a logical qubit can be stored, via error correction, for a time substantially longer than the decoherence time of its physical qubit components.

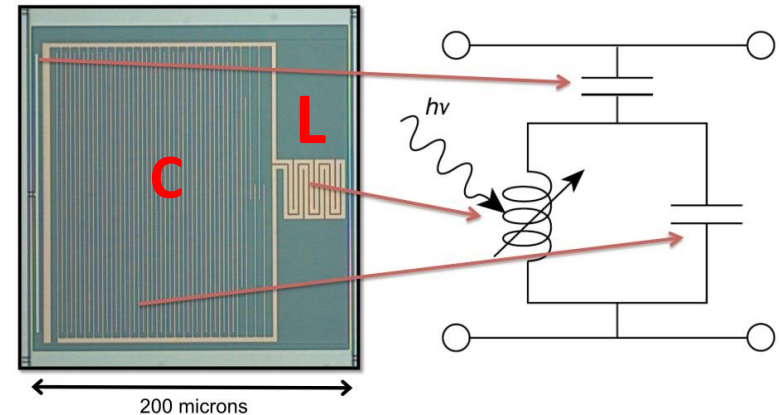
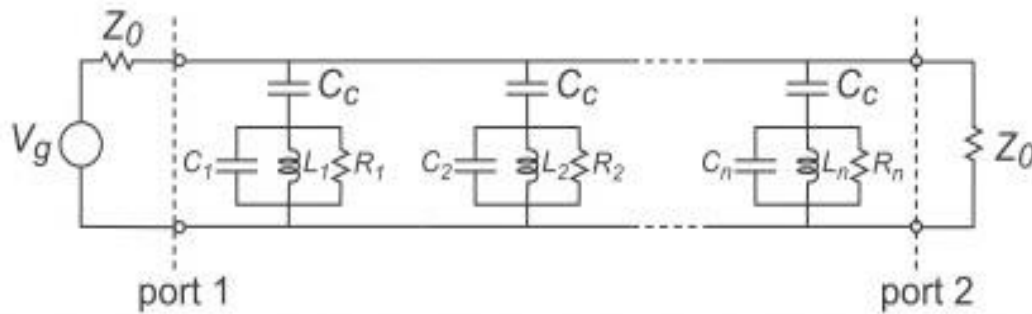


MKID: superconductor detectors for optical-NIR cosmology

10 K MKID pixel array
(B. Mazin, UCSB)



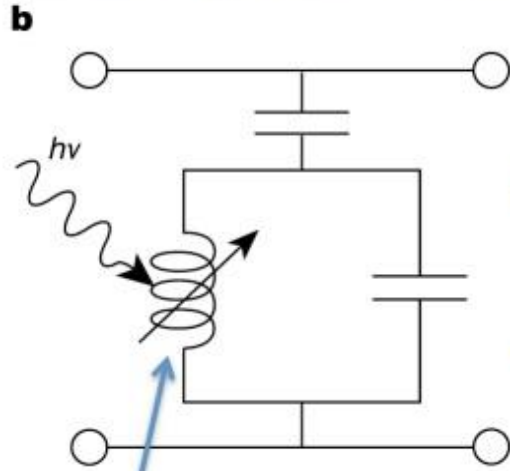
Equivalent
electronic
circuit.



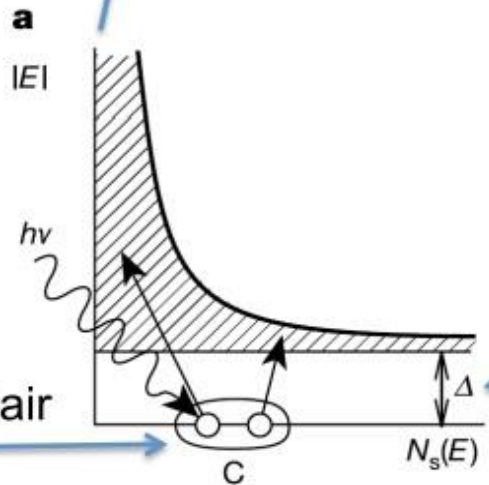
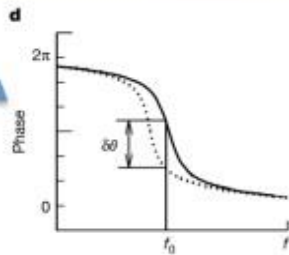
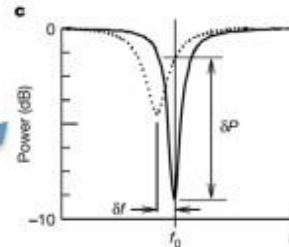
- Pixelated RF resonator array.
 - 2,000 pixels multiplexed in frequency coupled to RF feed/readout-line.

UVOIR MKIDs

MKID Equivalent Circuit



Inductor is a Superconductor!



Cooper Pair

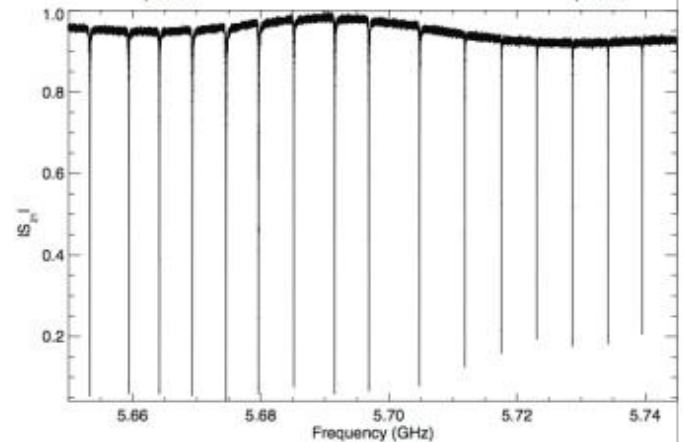
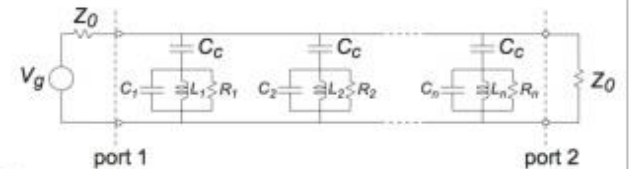
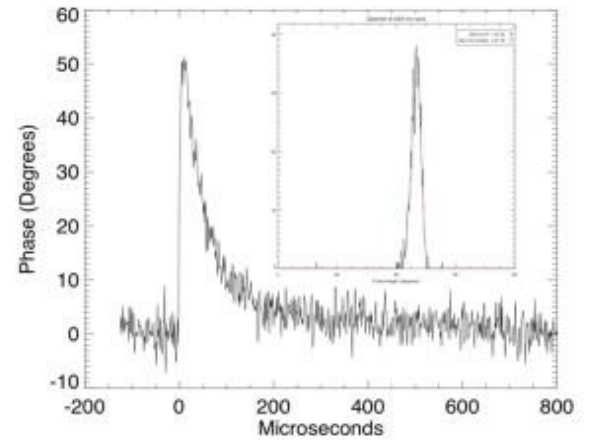
Energy Gap

Silicon – 1.10000 eV
 Aluminum – 0.00018 eV

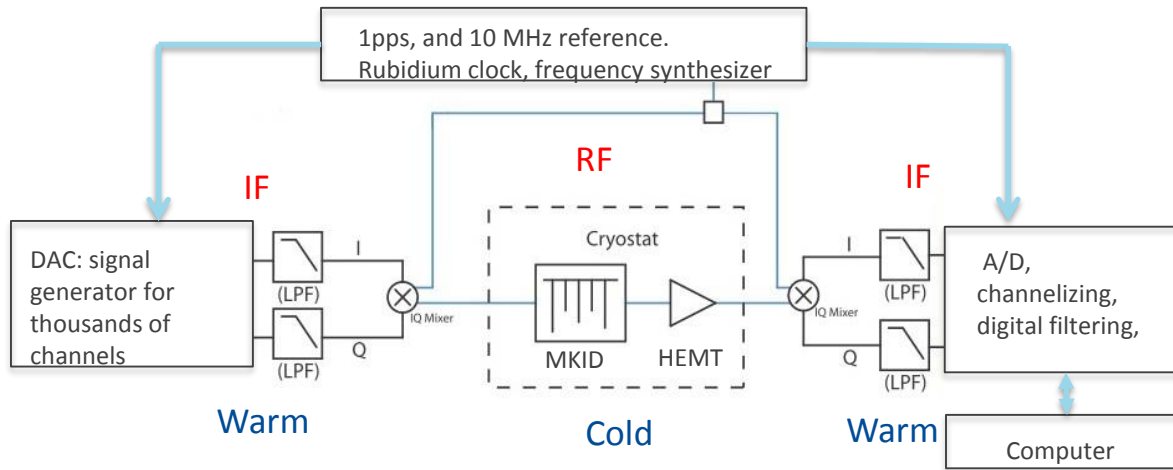
Energy resolution:

$$R = \frac{1}{2.355} \sqrt{\frac{\eta h \nu}{F \Delta}}$$

Typical Single Photon Event



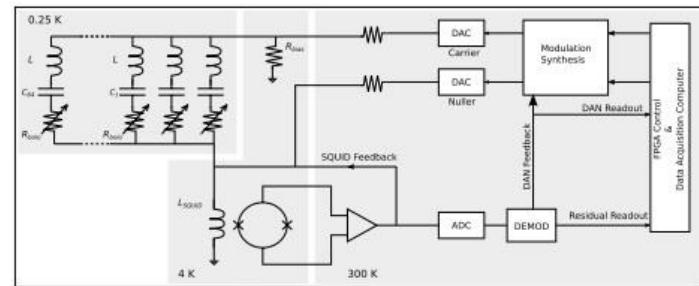
DAQs for Dark energy and the evolution of the universe



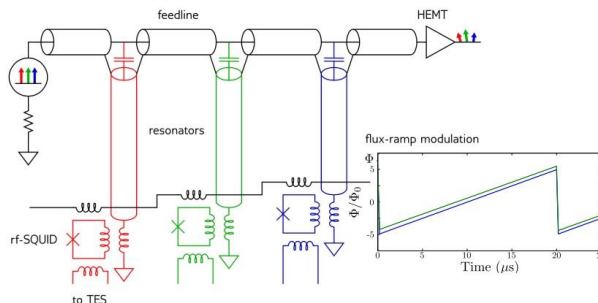
- Superconducting detectors
- Frequency multiplexed.
- RF electronics.
- Almost the same warm electronics.

Challenges:

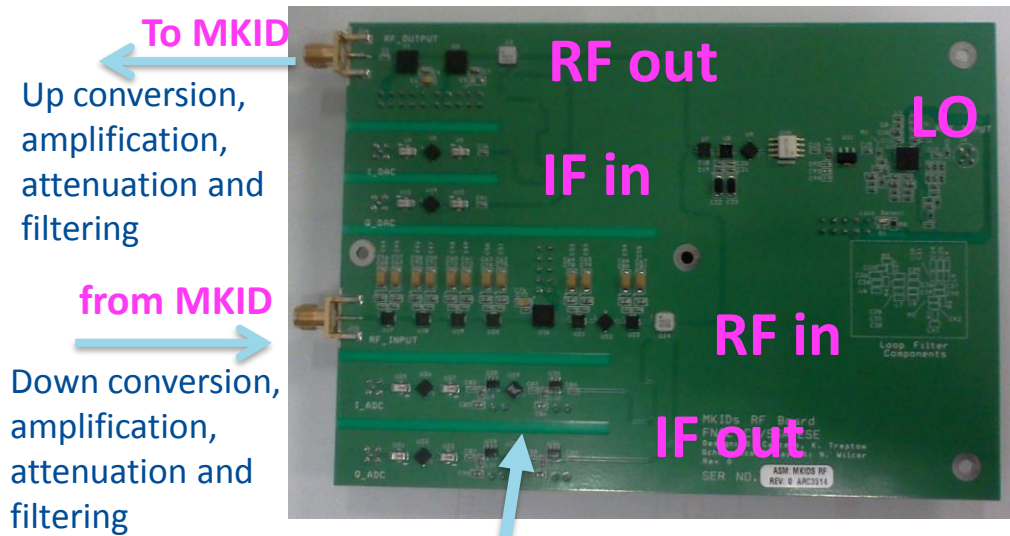
- High number of channels per RF feed to minimize thermal load and detector wiring.
- Low noise in a multi GHz RF environment with noise sources coming from digital electronics.
- Cost: ~1 dollar/channel.
- High input and output bandwidth.



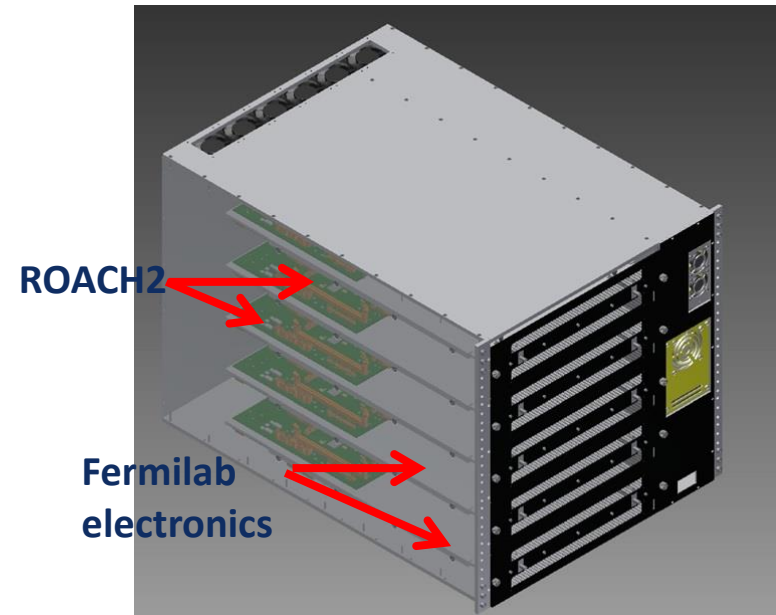
Microwave resonators to multiplex TES bolos (2)



Fermilab DAQ: this is the most advanced electronics today



10 K pixels crate



MKIDs for optical require a detector with a BW of ~ 250 KHz.
CMB ~ 100 Hz. (More channels per ADC and more resolution).

XILINX Zynq UltraScale+ RFSocCs

COMPARE	Reset	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
12-bit, 4GSPS RF-ADC		-	8	8	8	-
12-bit, 2GSPS RF-ADC		-	-	-	-	16
14-bit, 6.4GSPS RF-DAC		-	8	8	8	16
SD-FEC		8	-	-	8	-

Programmable Logic Features

COMPARE	Reset	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
System Logic Cells		930	678	930	930	930
DSP Slices		4,272	3,145	4,272	4,272	4,272
Memory (Mb)		60.5	41.3	60.5	60.5	60.5
33G Transceivers		16	8	16	16	16
Maximum I/O Pins		241	371	371	371	456

- **1 FPGA = ADC/DAC and computing of 10 x fMESSI boards!!**

-
- Where we are?
 - 1000 to 4000 resonators/boards.
 - \$5000/set of boards (ADC/DAC RF/IF).
 - Where we want to be
 - 10K to 50K resonators/board.
 - Factor of 4 reduction in cost per set of boards.
 - Major reduction in cost of a system.