CRYO: A waveform digitizer/serializer for cryogenic TPC experiments

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ASIC design and development activities at SLAC for future cold TPC applications

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- SLAC is designing a waveform digitizing ASIC (named “CRYO”) for cryogenic operation optimized for the charge readout of the planned nEXO TPC + version for Dune (considered as a risk mitigation potential alternative to main Dune approach)
  - Using a SoC approach (single ASIC with analog and digital functionalities)
  - With minimal number of IO/s
  - Digitally Assisted (highly programmable functionality and operation points across a large range of temperatures)
  - On chip regulated
  - Will allow the same chip to be suitable for both Liquid Argon and Liquid Xenon wire chamber applications
- As a compromise between performance of the front-end section and the speed of the back-end section an ASIC implementation in 130nm technology has been chosen
- Technology characterization at cryogenic temperature is now complete
- The first prototype of the ASIC is targeted for the end of the calendar year, so first generation chips should be available in February time frame.
  - In house testing capability; next iteration (if needed) would require perhaps 6 man months of additional engineering
- The prototype is designed to satisfy the baseline requirements of nEXO keeping in mind that as progress is made with simulations and overall architecture of the detector tweaks might be needed

Low Temperature CMOS pros and cons

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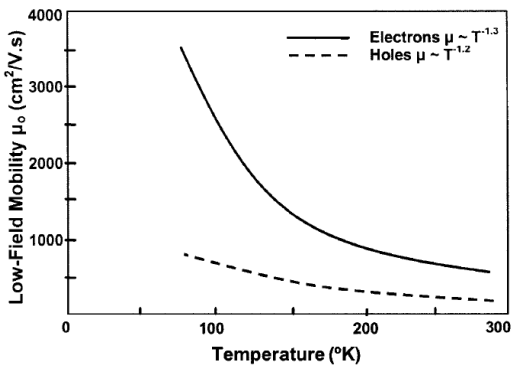
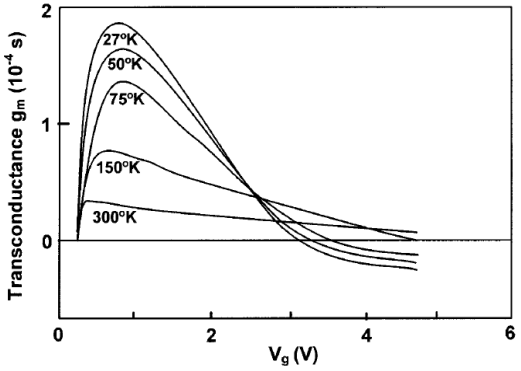
Mobility increase (low field)



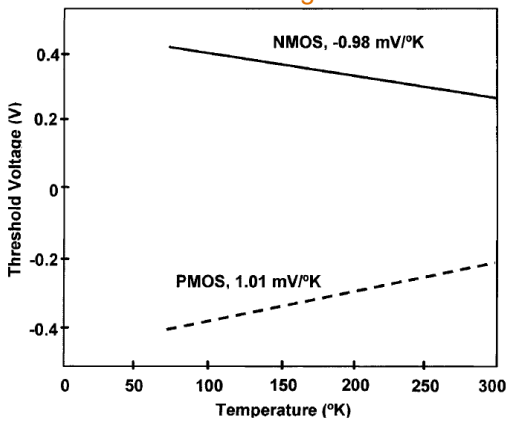
Velocity saturation appears at lower overdrives



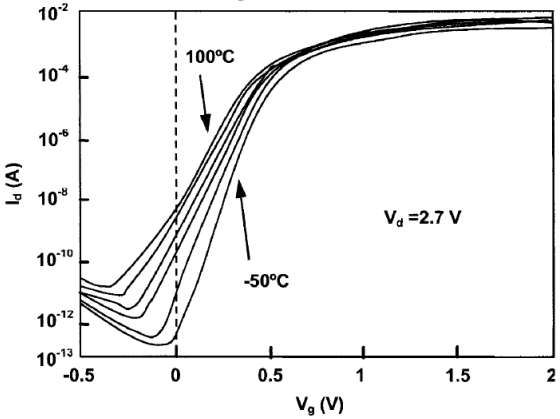
Interconnections Resistance

Resistance	300°K	77°K	4.2°K
N⁺ Diffusion	1	0.76	0.72
Polysilicon	1	0.89	0.88
Aluminum	1	0.14	0.05
P-well	1	0.30	< 10^{-5}

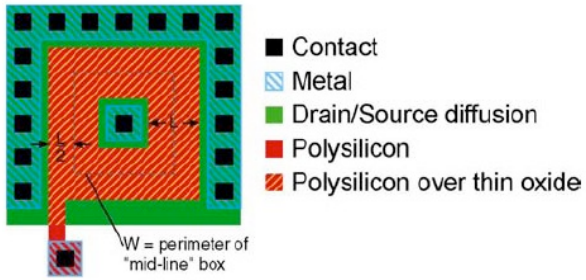
Threshold voltage increase



Leakage currents decrease



Reliability Issues: Hot carriers



Critical:

Foundry models are valid down to 233 °K. Although variations can be predicted, an optimized design requires the extractions of device parameters at cryogenic temperature.

Plots are examples from a 0.5um technology. W. Clark, TNS vol. 15, No. 3, 1992 pg. 397

Cryogenic setup for characterizing transistors at both LAr and LXe temperatures

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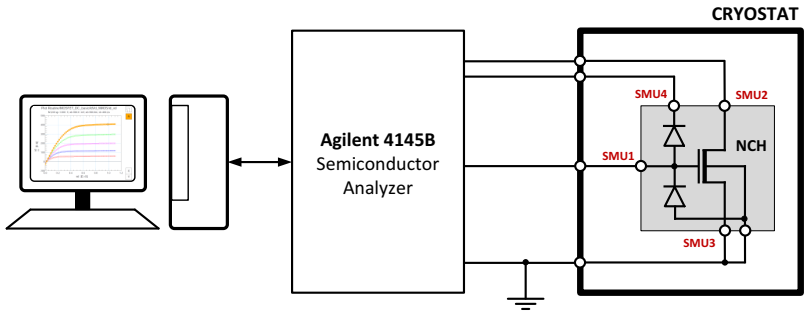
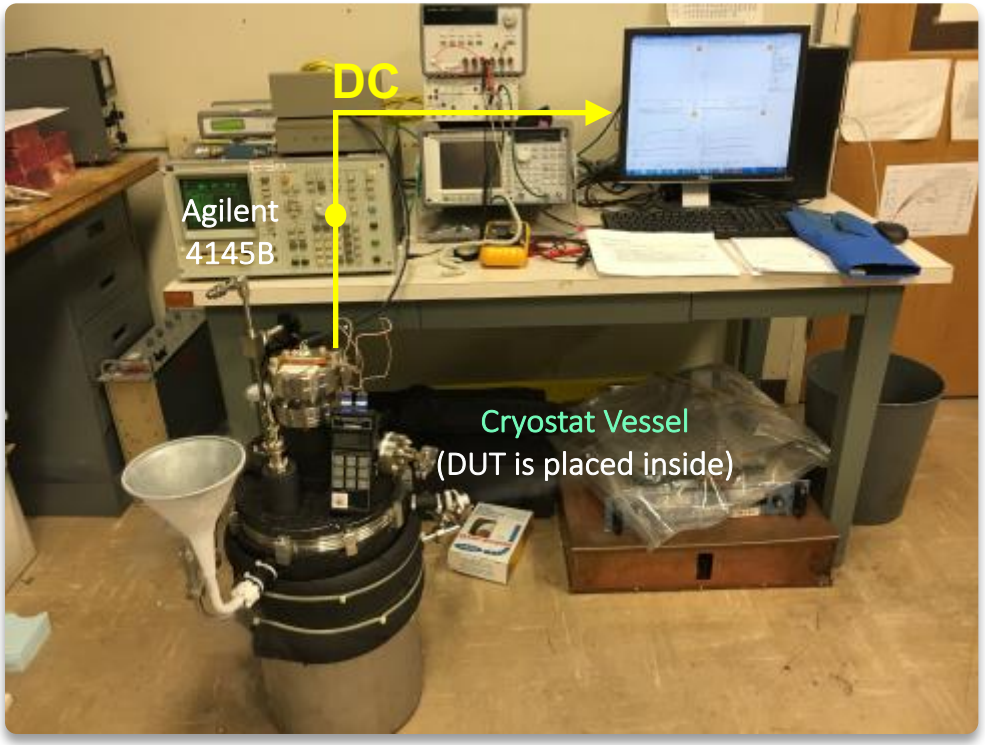
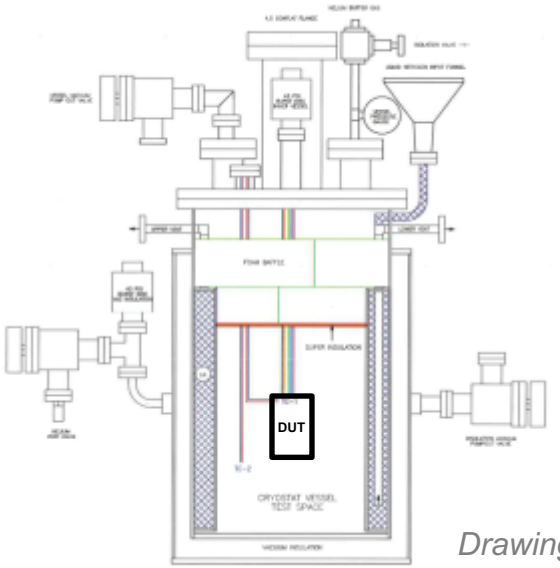
Test Bench Setup – Quick Overview

DC Measurement Setup





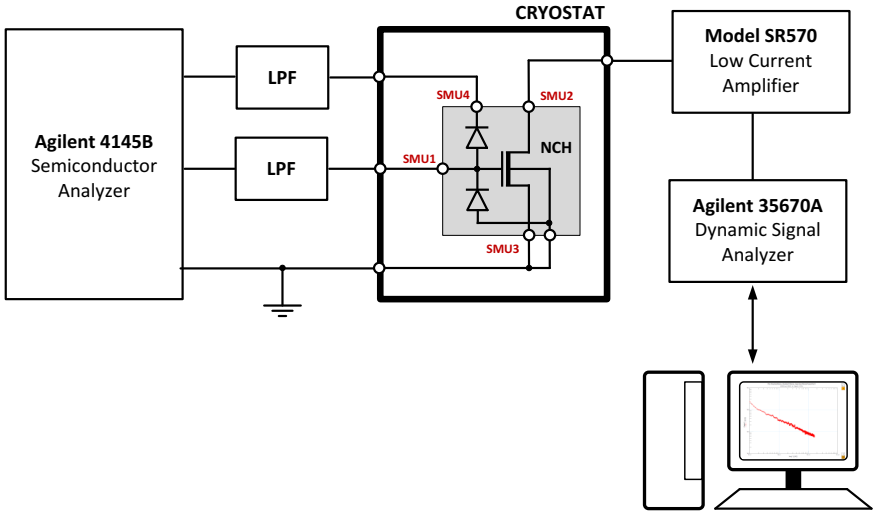


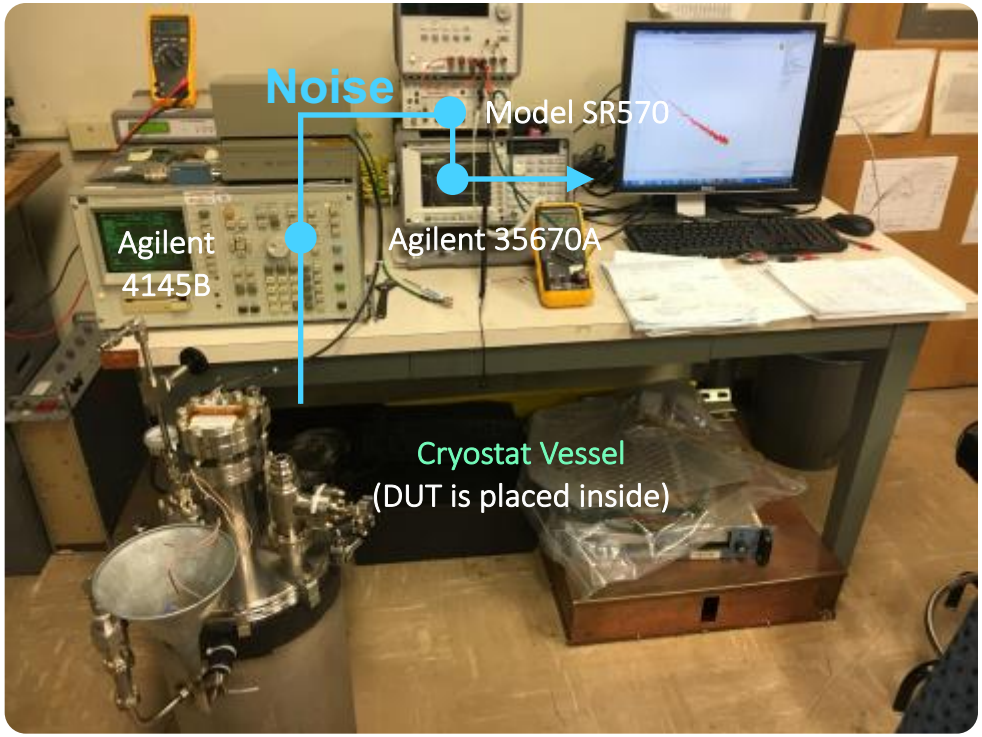
Drawing: Courtesy of Bob Conley

Cryogenic setup for characterizing transistors at both LAr and LXe temperatures

Test Bench Setup – Quick Overview

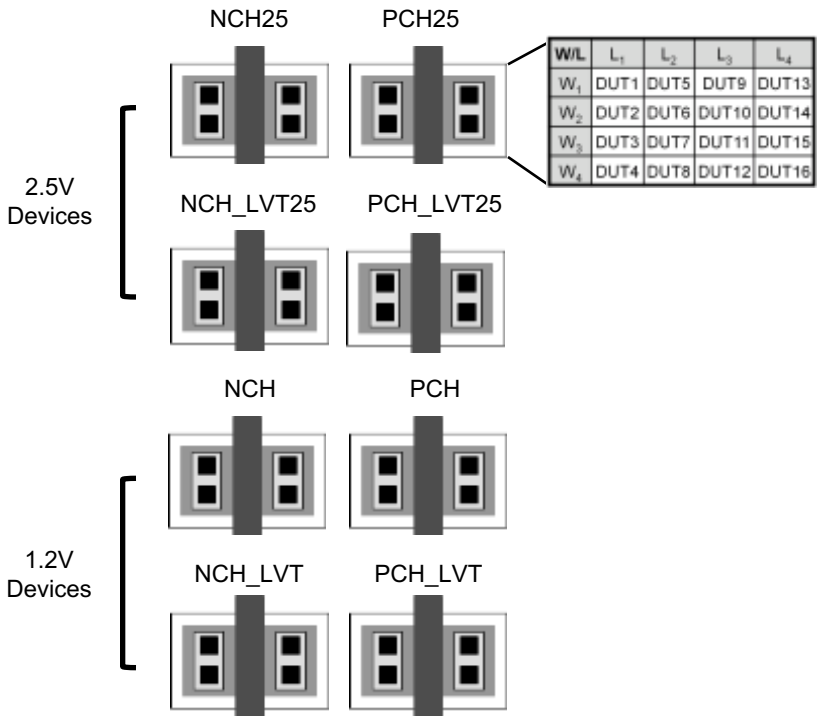
Noise Measurement Setup





Device Characterization

- 8 different types of transistors are targeted for cryo characterization (DC and Noise)
  - Each type is conformed by a subgroup of 16 devices with different W/L
  - The array is used to generate a binned DC model
  - 2.5V devices implement the front-end whereas 1.2V devices the digital back-end
- Cryo characterization has been completed
- Fitting/Modelling has been completed

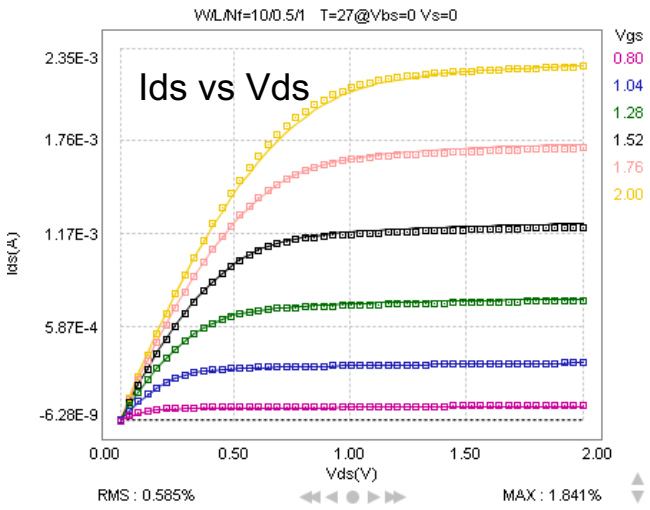


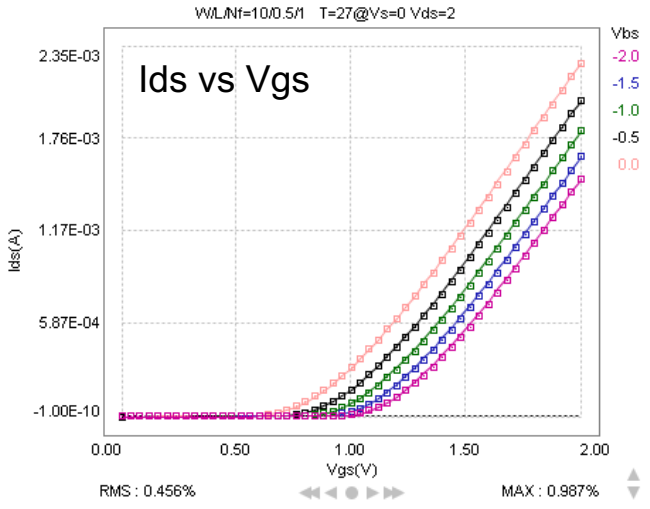
W/L	L_1	L_2	L_3	L_4
W_1	DUT1	DUT5	DUT9	DUT13
W_2	DUT2	DUT6	DUT10	DUT14
W_3	DUT3	DUT7	DUT11	DUT15
W_4	DUT4	DUT8	DUT12	DUT16

Device Characterization Across Temperature

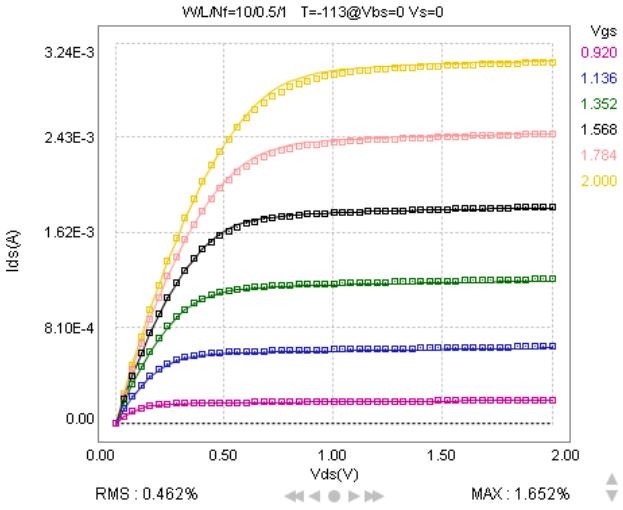
DC Model Vs Real Data (Some Examples) | NCH25 (10u/0.5u)

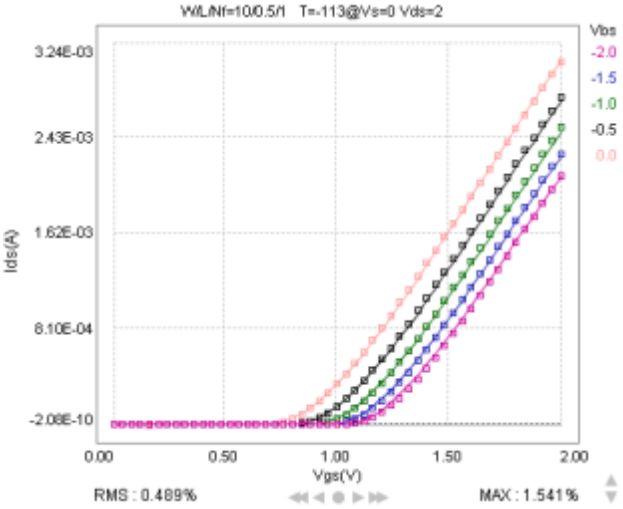
Room Temp



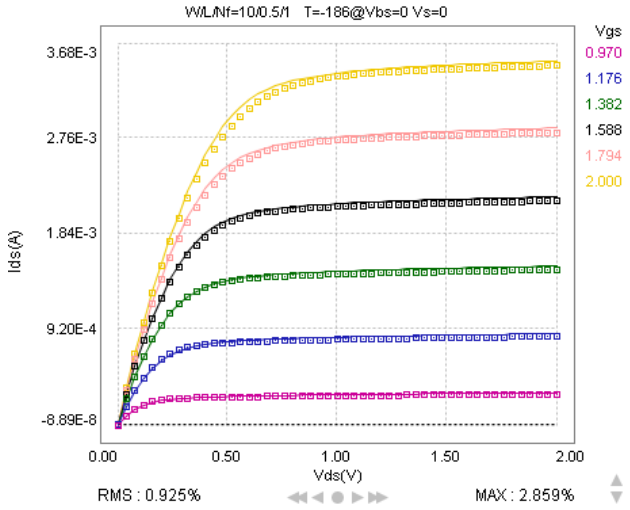


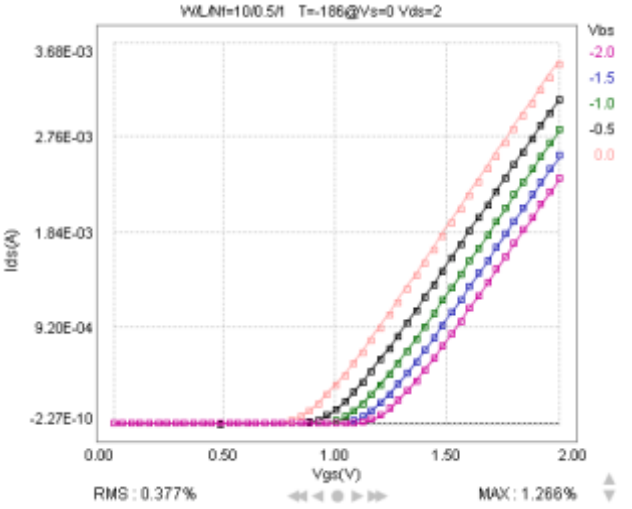
nEXO Temp





DUNE Temp

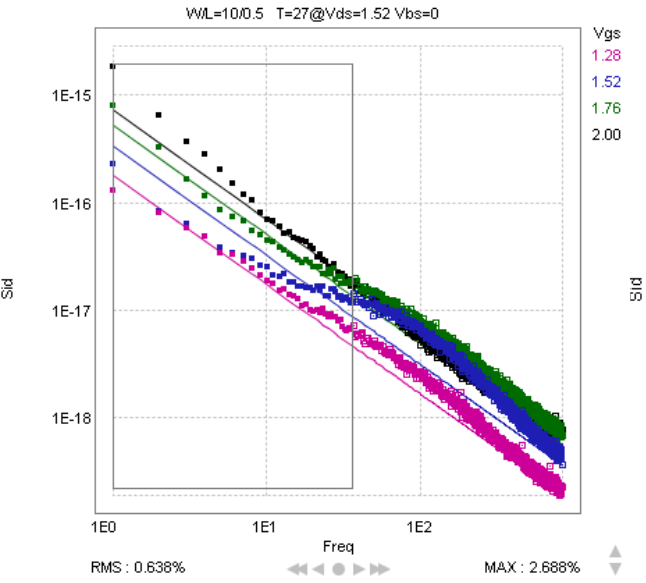




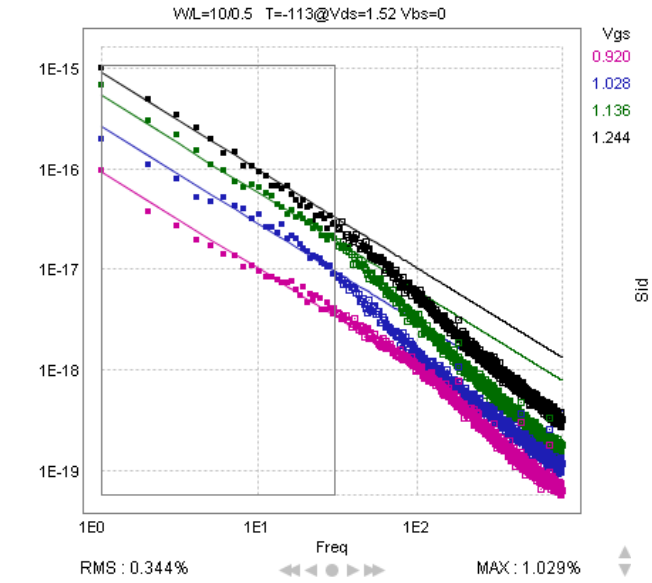
Device Characterization Across Temperature

Noise Model Vs Real Data (Some Examples) | NCH25 (10u/0.5u)

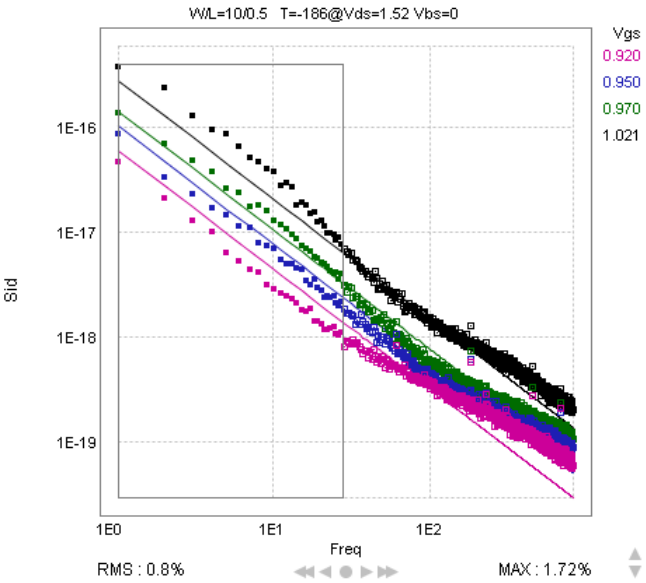
Room Temp



nEXO Temp



DUNE Temp



1/f Noise Coefficient

1/f Noise Exponent

$$S_{id} = \frac{Kf \cdot I_{DS}^{Af}}{Cox \cdot Leff^2 \cdot f^{Ef}}$$

1/f Noise Frequency Exponent (or Slope Correction)

Background – Readout signals from the planned nEXO TPC anode plane, now in development

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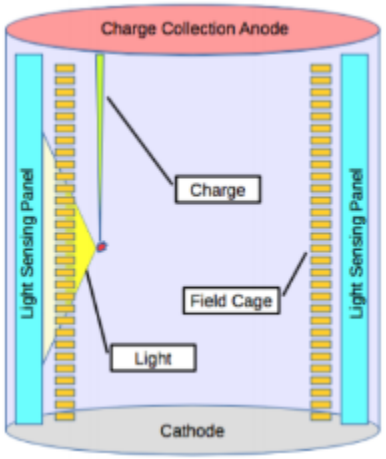
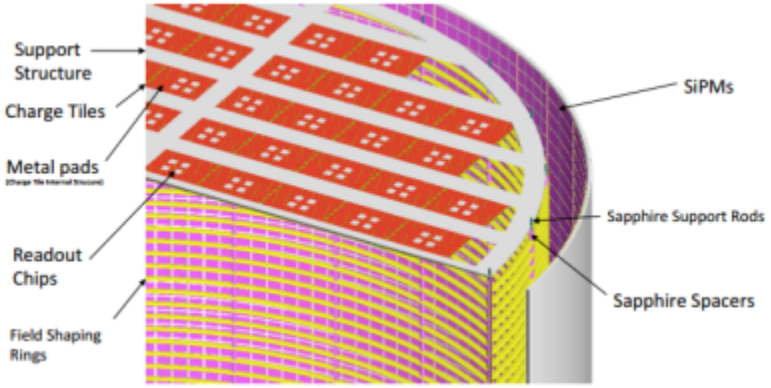
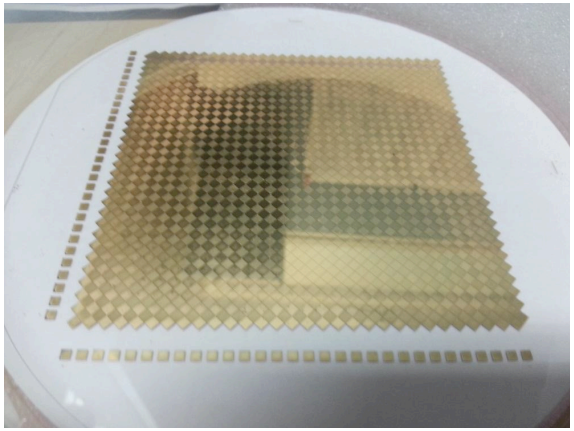
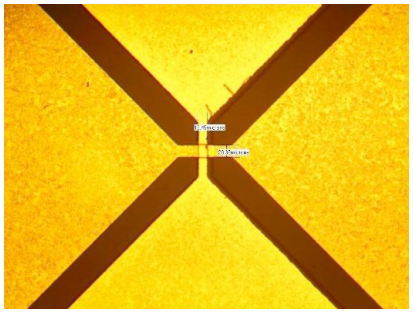
nEXO Detector components





Baseline unit sensing element



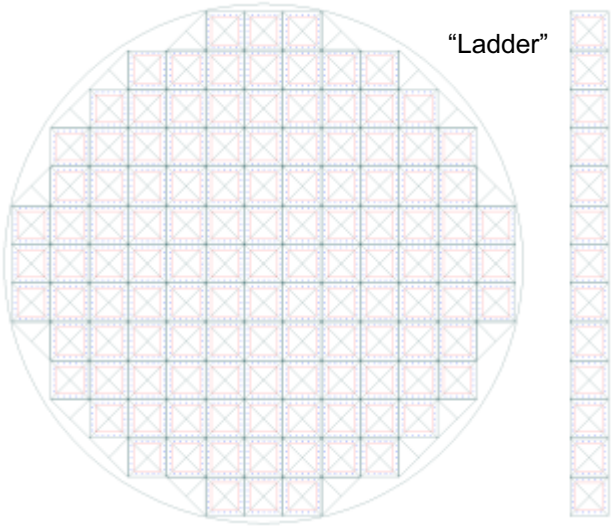


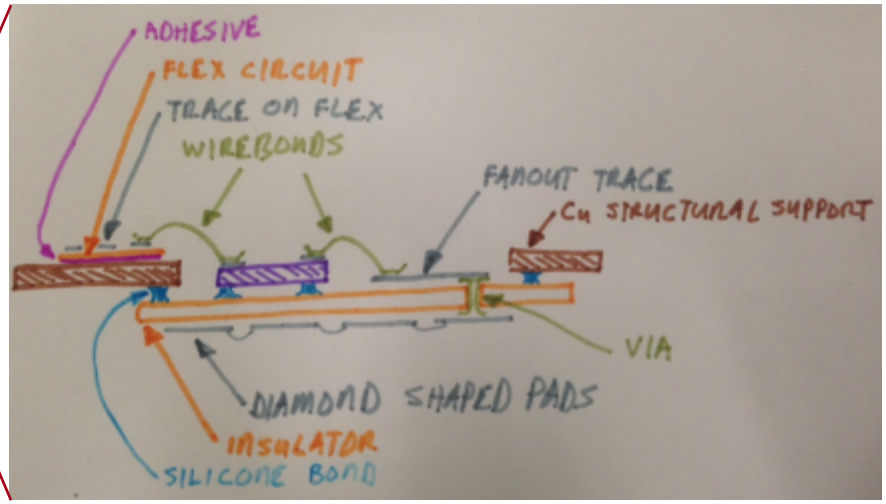
- Quartz Tile Size: 10 x 10 cm x 500 um with square pads
- Number of strips: 30 X strips and 30 Y strings
- Size of the strips: length ~ 10 cm diagonals of the square, 3 mm
- Capacitance of each strip to a group plane on the other side of the quartz tile, ~ 8 pF
- Capacitance of each strip to a single neighbor wire: ~ 0.2 pF
- Capacitance of each strip to all neighboring channels: ~ 6 pF

Implications on the readout ASIC:
- Operating temperature 165ºK
- Total input capacitance ~ 14pF
- High capacitance to neighbor channels (6pF) – Prone to crosstalk

nEXO anode plane

Baseline tile arrangement (K. Skarpaas)

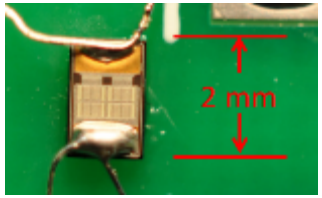




- Tiles are bonded to a metallic Cu strongback with flexible silicone dots to permit thermal contraction.
- The strongback has holes in it to access wirbonding pads on the back of the detectors. Vias through the detectors permit wirebonding from the detector back.
- Signals are carried out with flexible circuits which are bonded to the strongback.
- Negligible radioactivity levels ~ 10^{-12} levels of U, Th, and K40

Implications for the readout ASIC:
- Single Mixed-Signal ASIC 64 channels (130nm)
- Minimum number of I/Os
- On board supply regulation with external Si capacitors

IPDIA Si Cap
0805 100 nF 11V

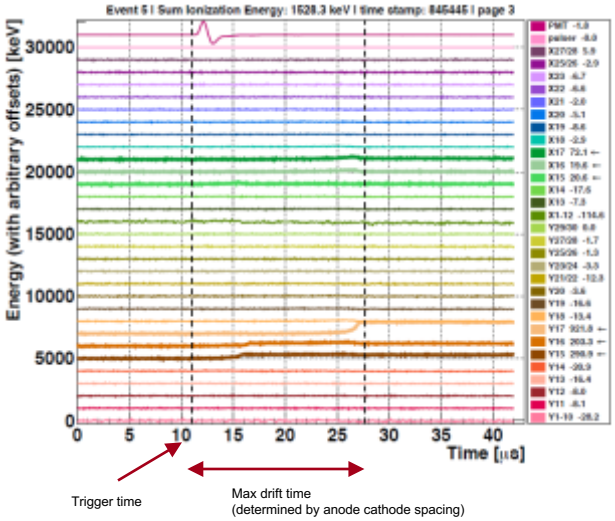


Cryo tested (R. DeVoe)

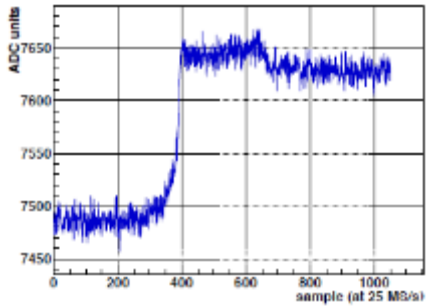
Up to 4.7uF (2016 size)

nEXO anode plane signals

Example of signals (A. Shubert)



Signals acquired at 25 MS/s. 1050 samples, with 275 samples before the PMT trigger. Each preamplifier has a rise time of ~ 50 ns and a decay time of ~ 300 microseconds (charge integration)

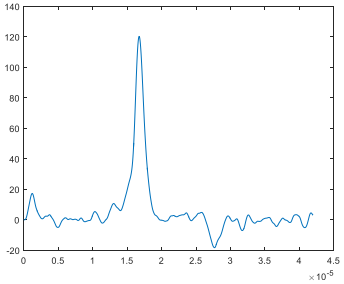


- One cloud of charge arrives at the anode around sample 400, a second cloud of charge arrives at the anode around sample 650

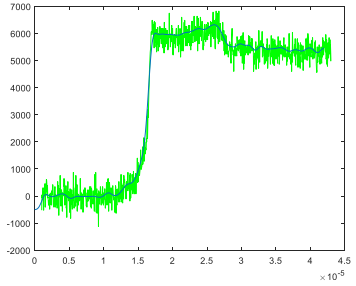
Input signal characteristics:

- Signals can have complex features
- There is information on the rise time of the signal that we want to extract
- Typical signal: 100ke- (0nbb event at 2.5 MeV)
- Max signal: 400ke-
- Noise floor: 200-250e-
- Bandwidth: <250kHz

Current signal cut at 250kHz



Reconstructed Charge



Implications on the readout ASIC:

- Waveform digitize the current signal
- ADC resolution: 12bits
- ADC INL, DNL: < 1 bit
- ADC Sampling freq: 2MSPS (more in the next slides)

Additional requirements

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Power budget:

- To meet the power budget requirements of the full detector the ASIC power consumption is targeted at < 10mW/ch

Calibration:

- On chip calibration with 0.2% of full scale

Reliability:

- Full Digitally Assisted design (all bias points of the analog section are programmable)
- Input protection
- Hot electron effect mitigation (reduced supply)
- Some redundancy in the configuration protocol
- Further redundancy options can be pursued in the context of an overall architecture evaluation

How does this compare to Dune?

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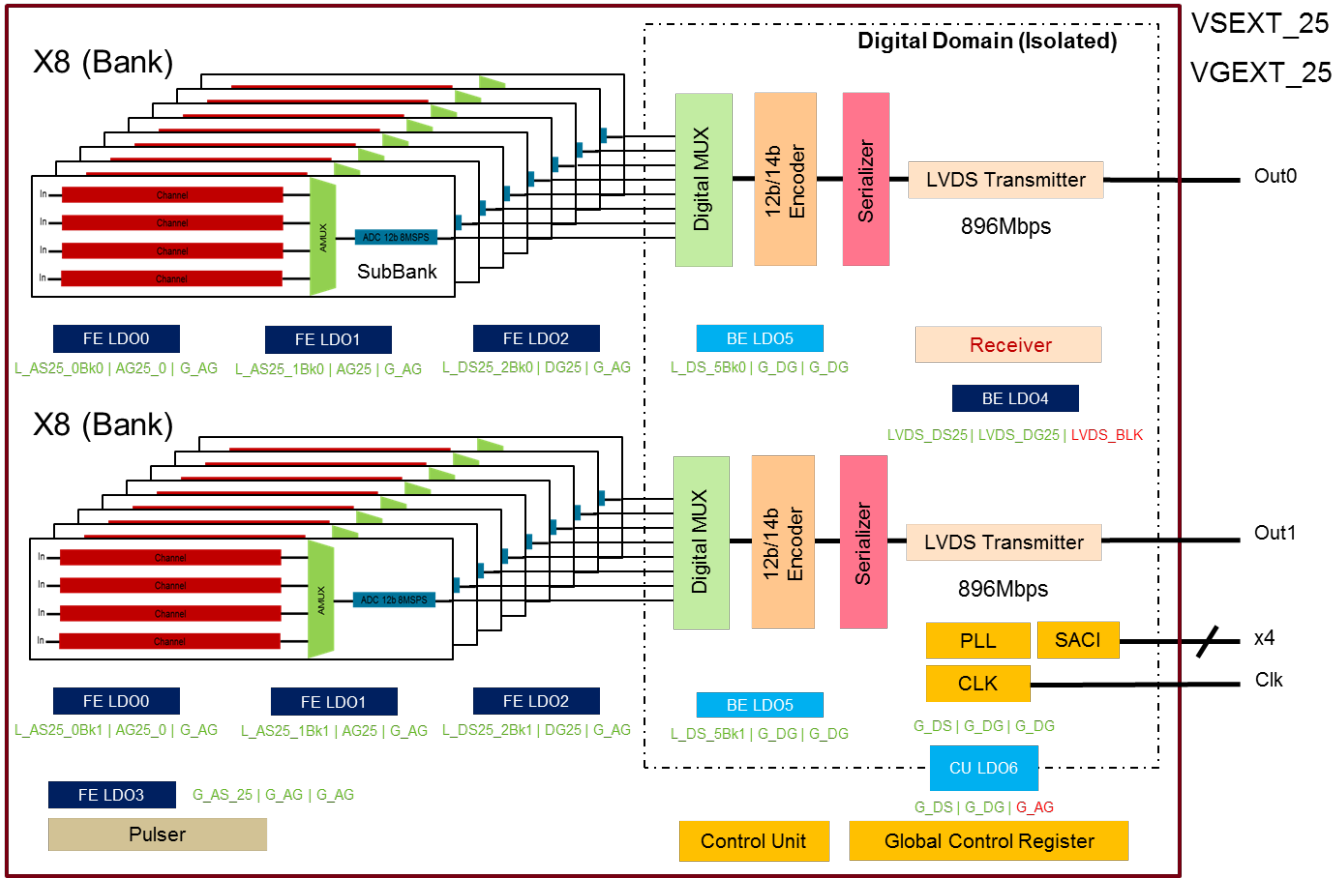
	nEXO	DUNE
Input capacitance	~ 20pF	~ 200pF
Bandwidth	Bessel 5th (P.T. 0.8us, 1.6us, 2.4us, 4.8us)	CPSG 5th (P.T. 0.5us, 1us, 2us, 3us)
Noise	200e-	ALARA (~500e-)
Multiple gains	1X, 0.5X, 0.25X, 0.125X	1X, 0.5X, 0.25X, 0.125X
Dynamic Range	12bit	12bit
Sampling Freq.	2MSPS	2MSPS

CRYO architecture

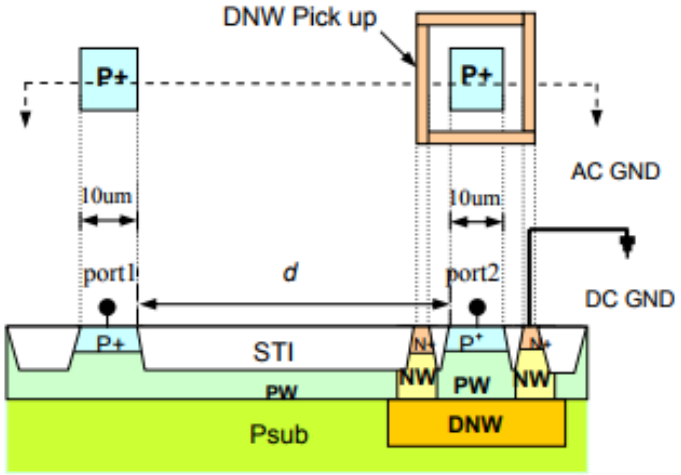


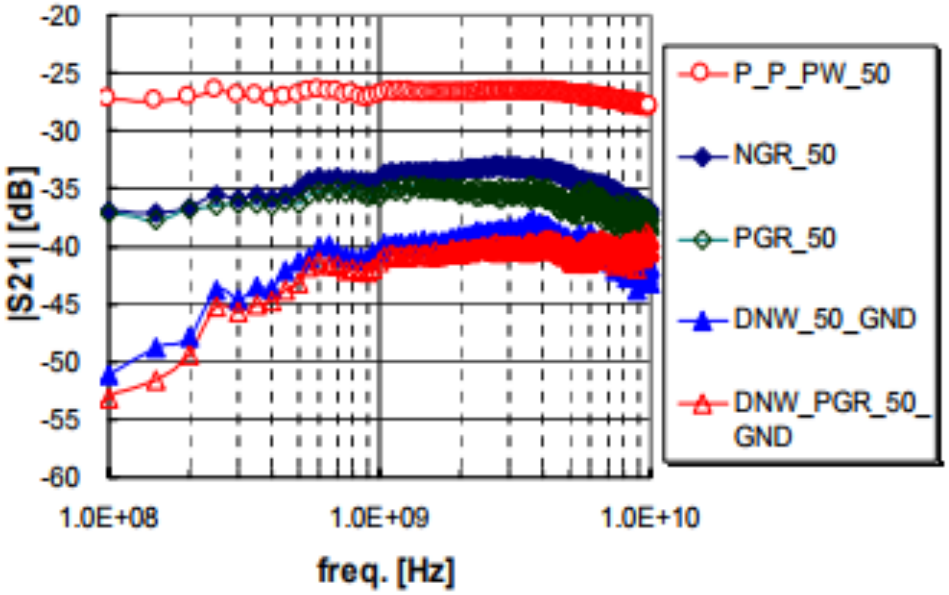
Overall Architecture:

- 64 channels divided in 2 32-channel sections with a single data output
- Distributed supply regulation on-chip
- 4x1 multiplexing of channels into a single ADC with a dedicated LDO
- 8MSPS 12b SAR ADC (2 MSPS/ch)
- 12b/14b custom data encoding
- Serialization and LVDS data transmission at 896Mbps
- Digital domain isolated in DNW
- Dedicated slow control unit (SACI) an global registers to control functions and operative points (digitally assisted operation of analog sections)

Substrate Isolation: Key to combining digital and analog functionality

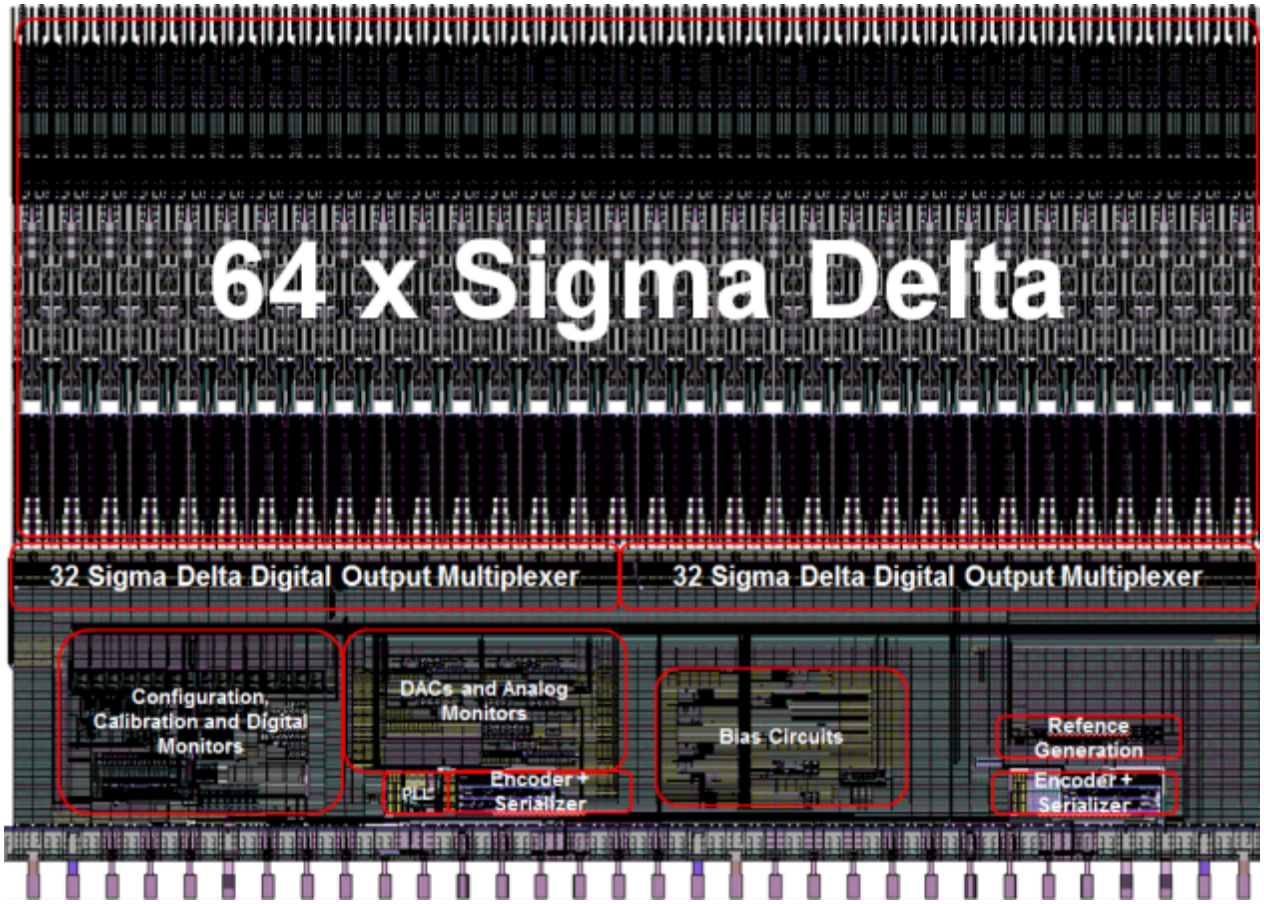
Approach tested in several designs

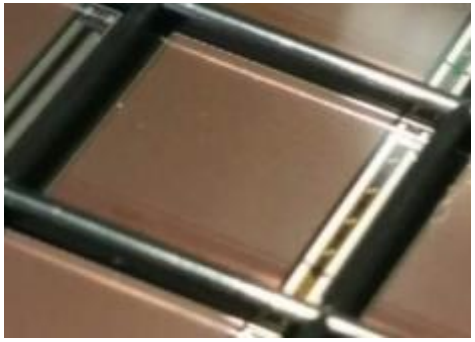




Wen-Kuan Yeh et al. Solid State Devices and Materials, Tokyo, 2003, - 408 - P1-5 pp. 408-409

Serializer/readout architecture is taken from existing chips (tPix, cPix,ePixHR) digital activity is here isolated in deep NWELLs

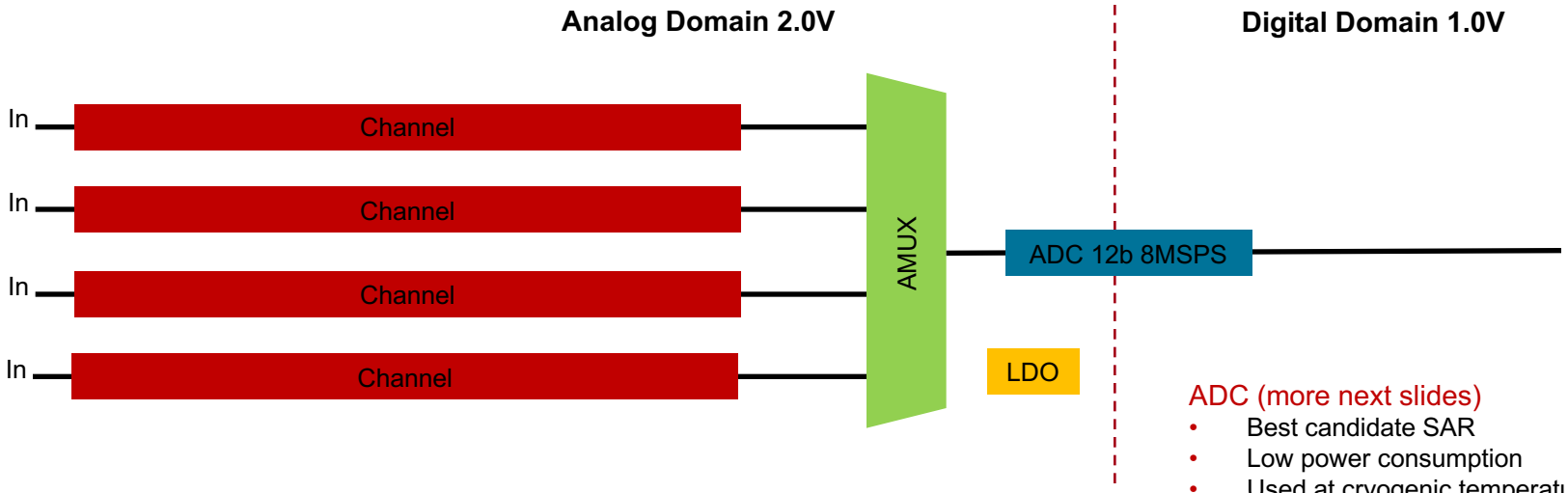




tPix 130nm

SLAC CRYO ASIC architecture

Analog front-end implementation

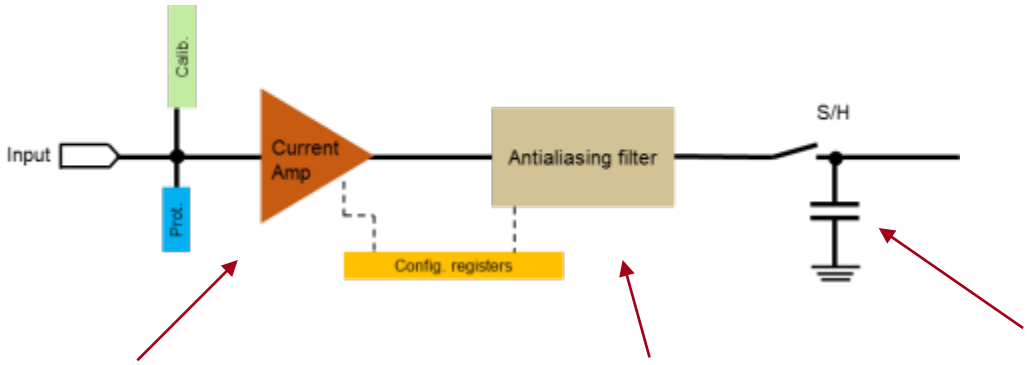


ADC (more next slides)

- Best candidate SAR
- Low power consumption
- Used at cryogenic temperature in several applications
- Requires few analog components

SLAC CRYO ASIC architecture

Channel Architecture:

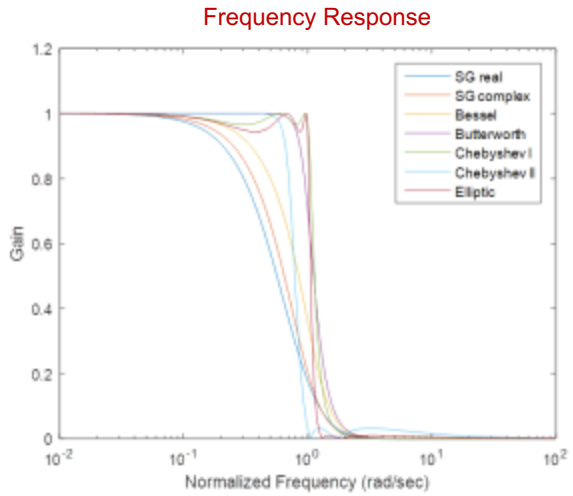


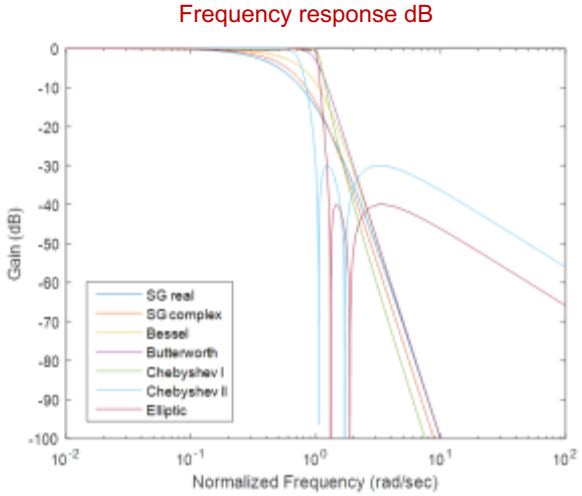
- Preamp with pole zero cancellation (G. De Geronimo approach)
- Highly programmable
- Gain relay on capacitive matching
- Can be easily digitally assisted to tweak operation at different temperatures

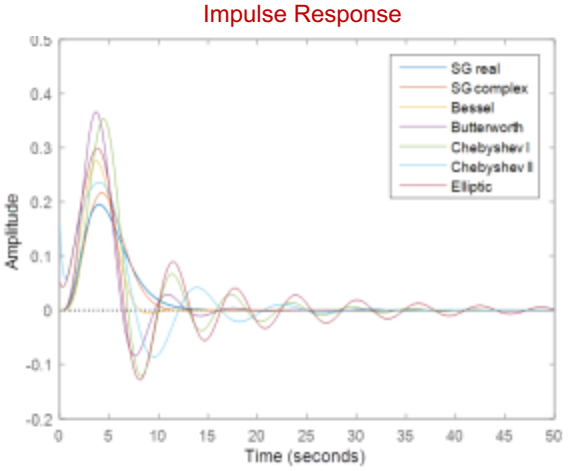
- Bessel architecture:
  - avoid aliasing
  - optimize S/N ratio
  - avoid waveform distortion

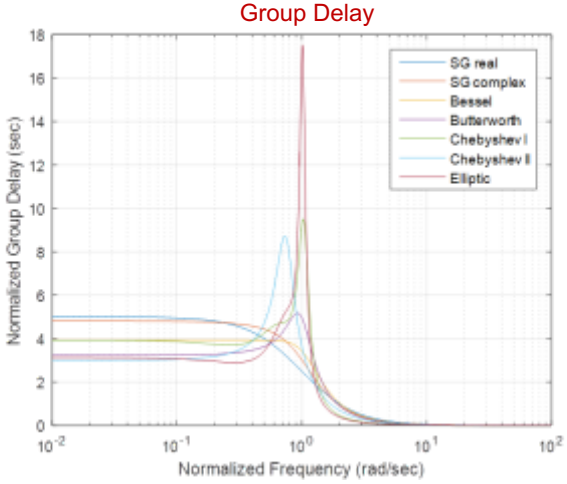
- Concurrent sampling on all channels is required
- A S/H allow as to multiplex more channels on a single ADC

Antialias filter, Sampling frequency, and distortion







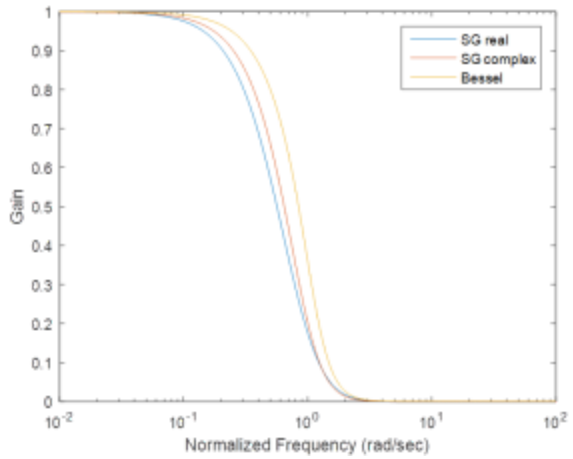


Antialias Filter

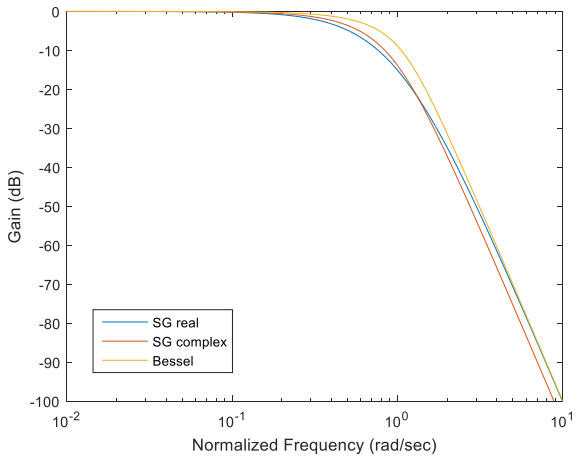
- Prevents spectral replicas due to sampling overlap
- Bandwidth needs to accommodate the signal content
- Its characteristics affects:
  - sampling frequency
  - duration of the response
  - waveform distortion
- Nyquist-Shannon limit “really” says:
  - $f_s > 2f_{-40dB}$
- Group Delay is a measure of the distortion. The more constant the delay the less the filter introduces distortion

Antialias filter, Sampling frequency, and distortion

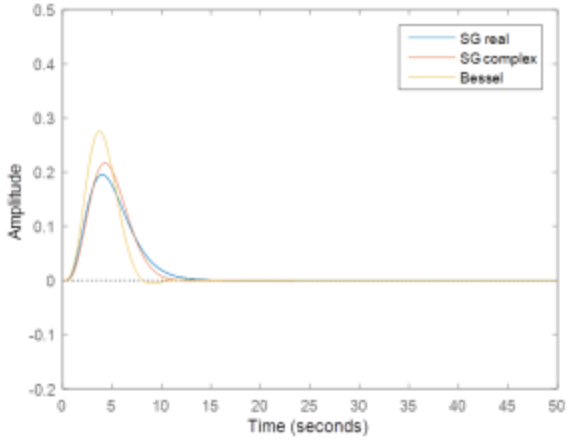
Frequency Response



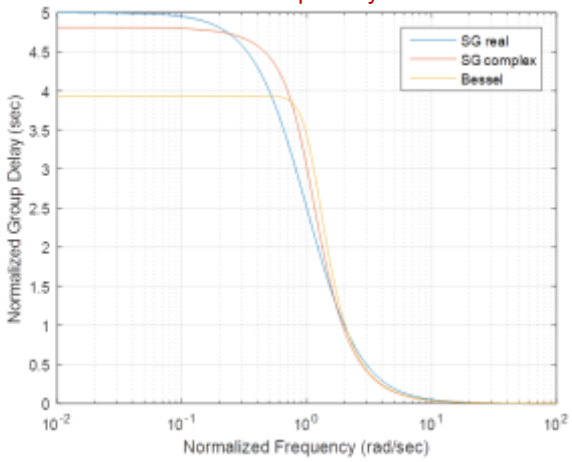
Frequency response dB



Impulse Response



Group Delay



Antialias Filter

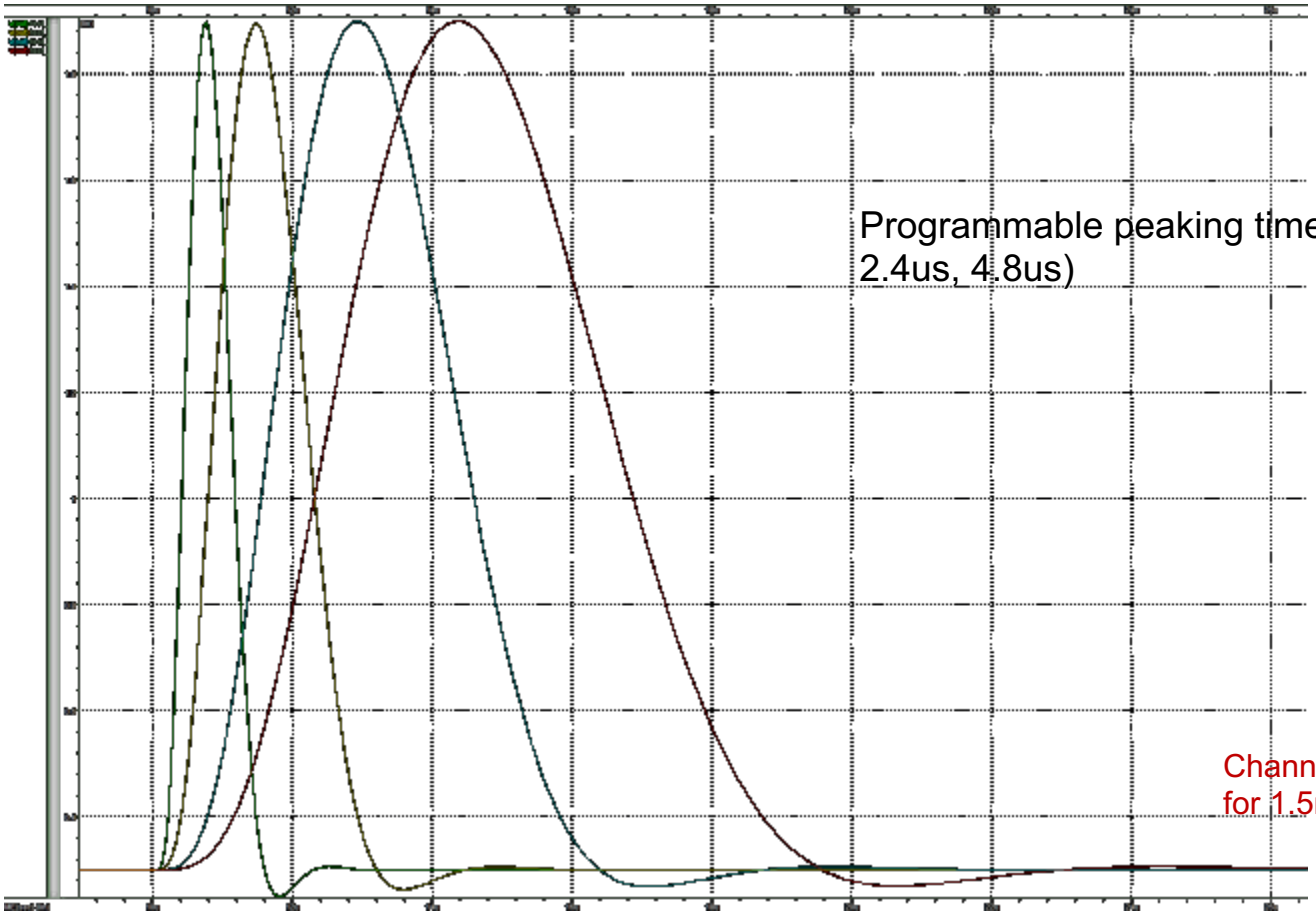
- Classic semi-gaussian shaper together with the Bessel filter have the best behavior for our application
- Short impulse response with no ripples
- Flat group delay (Bessel win)

	f_{-40dB} /f_{BW}	ADC fs (250kHz signal)	Signal Bw (ADC fs 2MSPS)
SG real	6	3MSPS	160kHz
SG complex	4.7	2.4MSPS	212kHz
Bessel	4	2MSPS	250kHz

Simulated Channel Response

SLAC

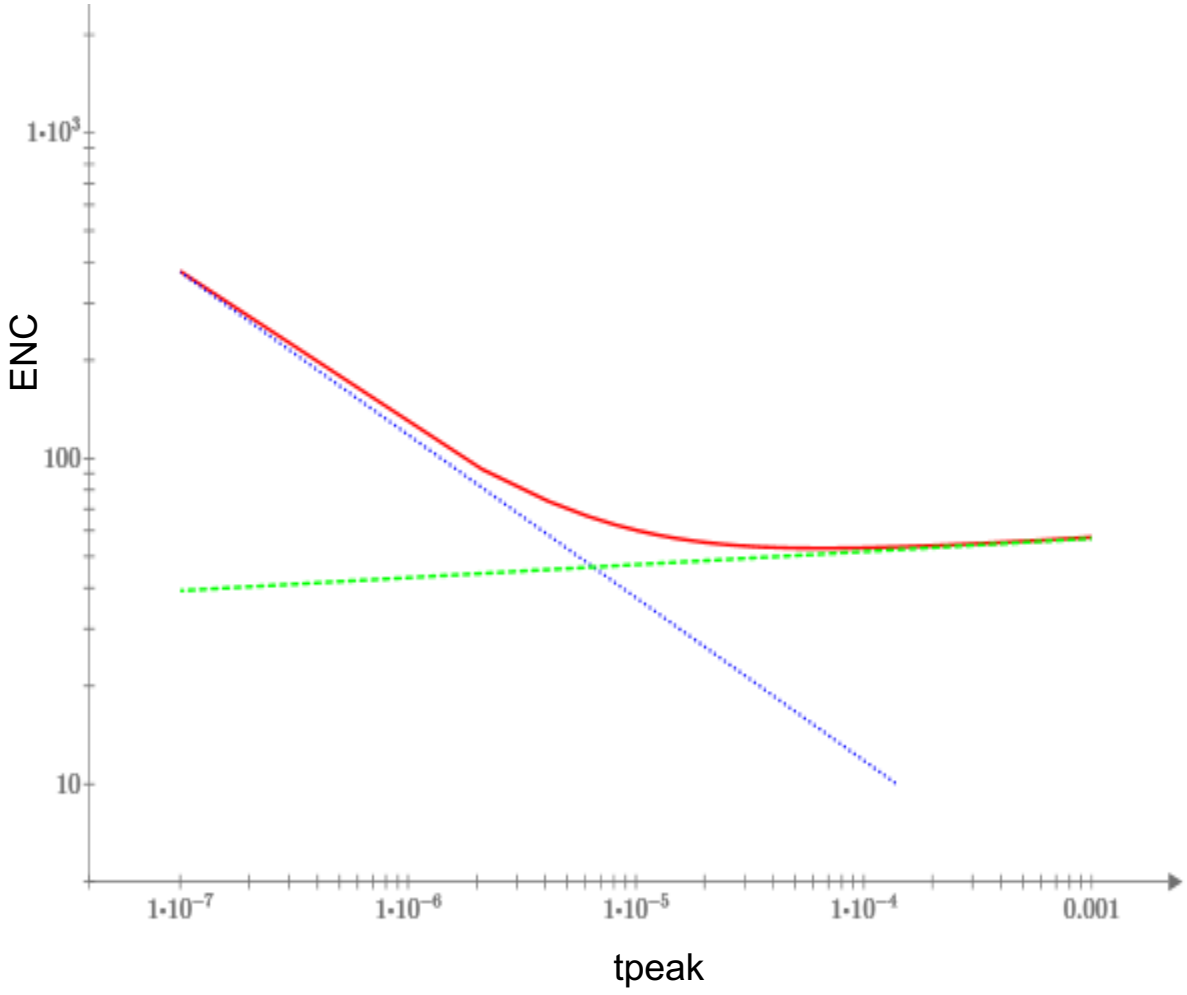
Bessel



Programmable peaking time (0.8us, 1.6us, 2.4us, 4.8us)

Channel Current consumption for 1.5mA

Preliminary noise estimates from cryogenic models (for nEXO optimized circuit)



Temp. 160K
Id = 200uA
Cin = 20pF

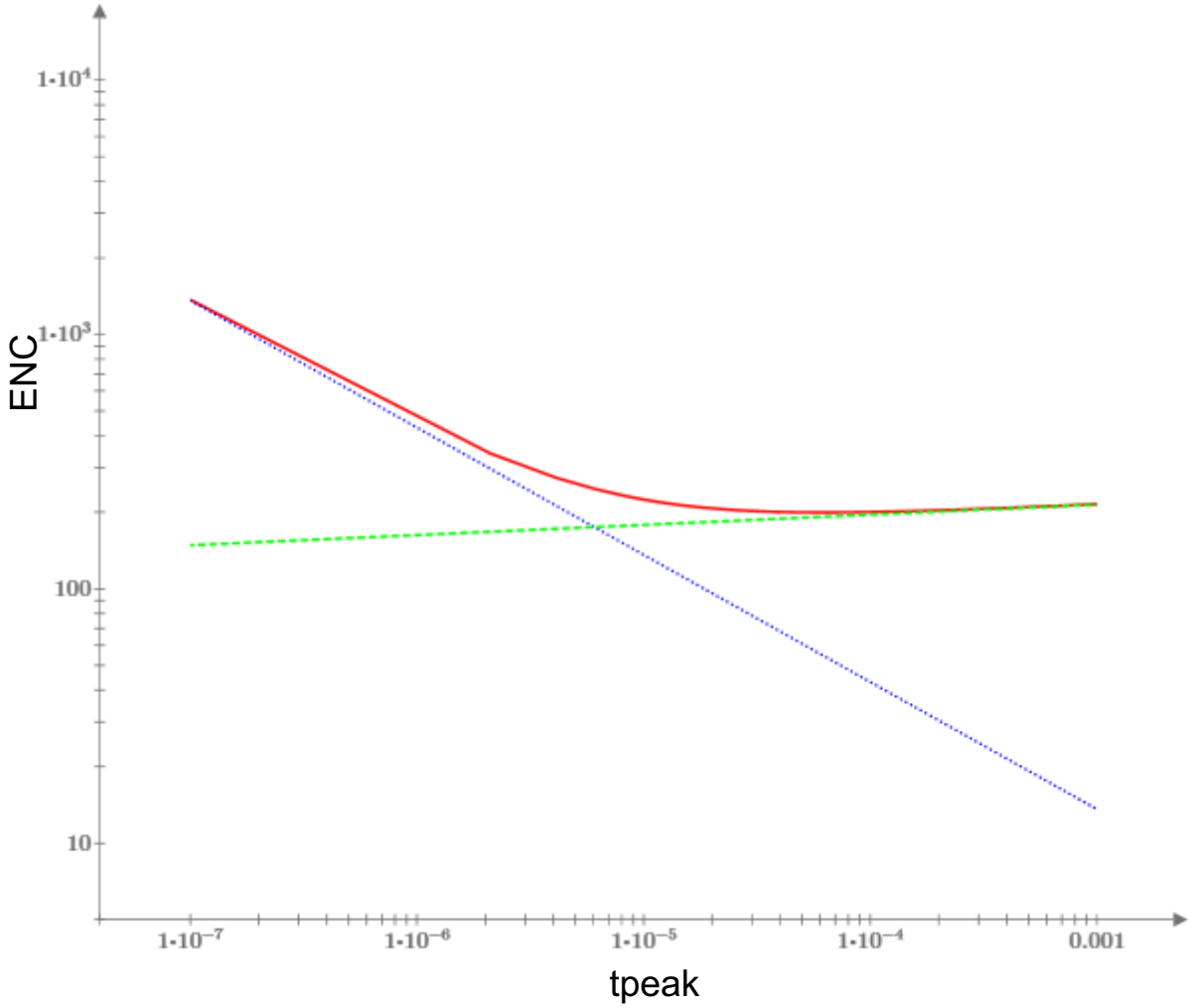
W = 2m
L = 280n

ENC ~140e$^-$ @ 0.8us

Using this front end for Dune would give ~850e$^-$

(this might be satisfactory, but it is not even optimized for DUNE yet, just using nEXO ASIC circuit)

Optimizing for Dune: preliminary noise estimates from cryogenic models



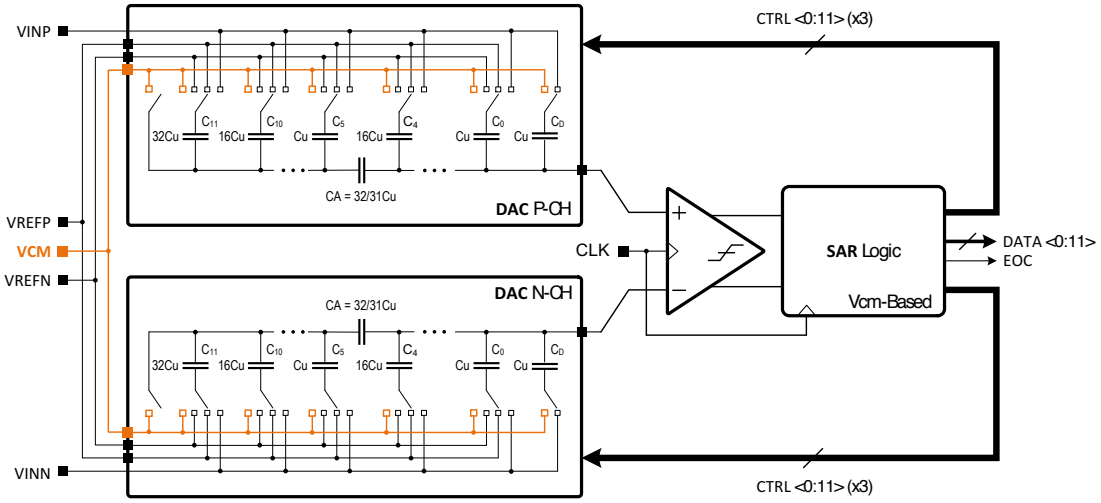
Temp. 80K
Id = 420uA
Cin = 200pF

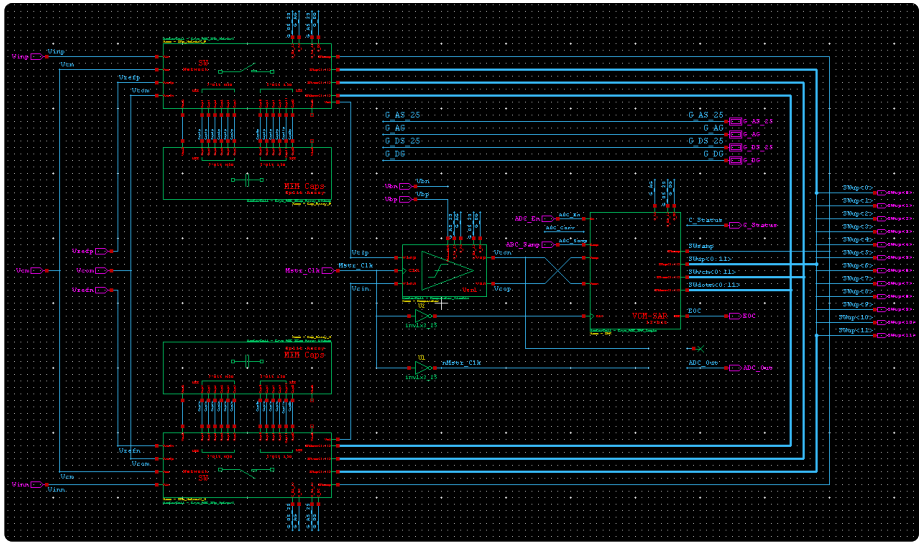
W = 18m
L = 280n

ENC ~500e$^-$ @ 0.8us

So lower noise can be achieved with some circuit optimization for DUNE

SAR ADC





Key ADC Specs

CMOS process	130 nm
Supply Voltage	2.0 V
Type	Nyquist Rate
Architecture	Synchronous SAR
DAC Switching Scheme	Vcm-Based Split Capacitor Array
Mode	Fully-Differential
Resolution	12 bit
Sampling Rate	10 MS/s
INL/DNL	< ±1 LSB
Current Consumption (ADC only)	< 800 uA
Temperature	160°K (-113°C) and 87°K (-186°C)

Main Features

- **Fully differential configuration**
- **Comparator with two-stages preamplifier followed by latch circuit**
  - High gain and low sensitivity to kickback noise
  - Digitally assisted to adjust operation at cold temperatures
  - Internal offset cancellation
- **Split capacitor DAC based on VCM switching scheme [Y. Zhu, JSSC2010]**
  - Obviates the need of the MSB capacitor
  - Improves area and DNL by x2 times wrt conv. split configuration
  - Reduces switching energy by ~80% wrt conv. binary weighted
  - Cu = 62fF (MIM capacitor) meets noise and linearity requirements (DNL and INL < ± 1 LSB)
  - Does not require calibration (but we are adding offset calibration)

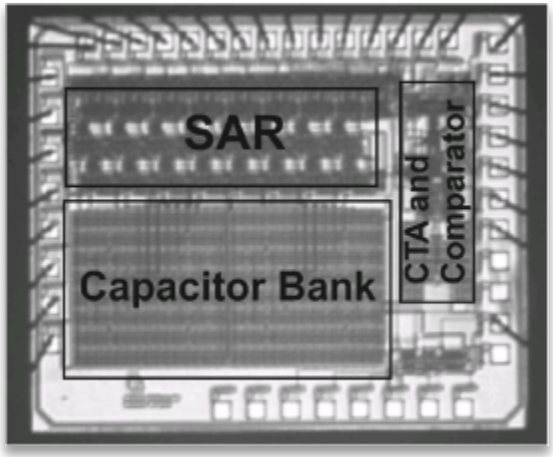
SAR ADC

Why SAR?

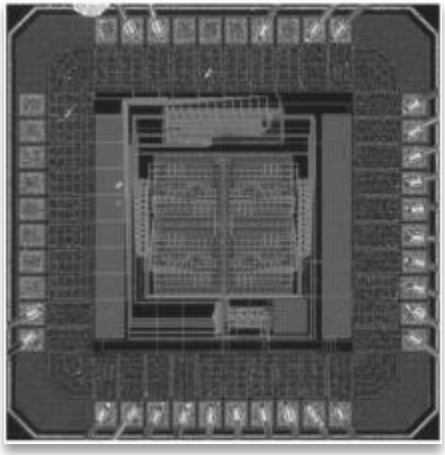
State-of-the-Art Solutions

@ Cryo Temp

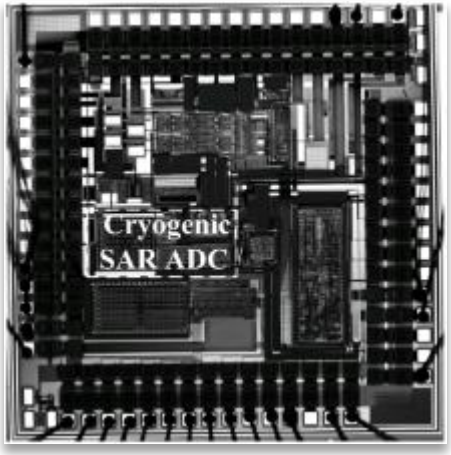
ISSCC 2007 [1]
Down to 4K



AIP 2010 [2]
Down to 4K



J. Semicond. 2011 [3]
Down to 77K



J. Shangai-Springer 2013 [4]
Down to 77K

References:
[1]. Y. Creten, *et al.*, "A cryogenic ADC Operating Down to 4.2K", International Solid State Circuits Conference, 2007.
[2]. B. Okcan, *et al.*, "A Cryogenic Analog to Digital Converter Operating from 300K down to 4.4k", Review of Scientific Instruments, 2010.
[3]. H. L. Zhao, *et al.*, "A Cryogenic SAR ADC for Infrared Readout Circuits", Journal of Semiconductors, 2011.
[4]. Y. Q. Zhao, *et al.*, "A Cryogenic 10-bit SAR ADC Design with Modified Device Model", J. Shanghai Jiaotong Univ. (Science) - Springer, 2013.

SAR ADC Performance

Simulation Results at -113ºC

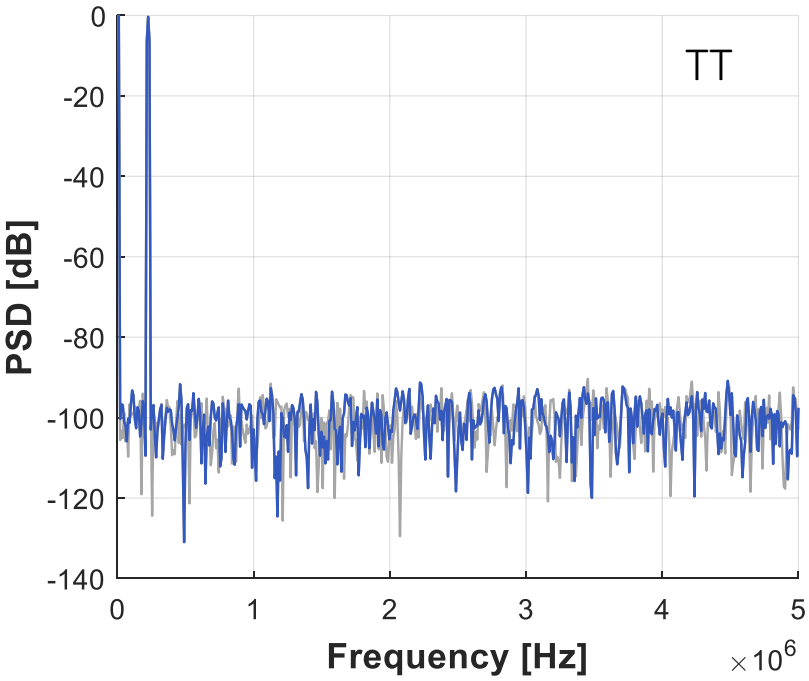
SLAC

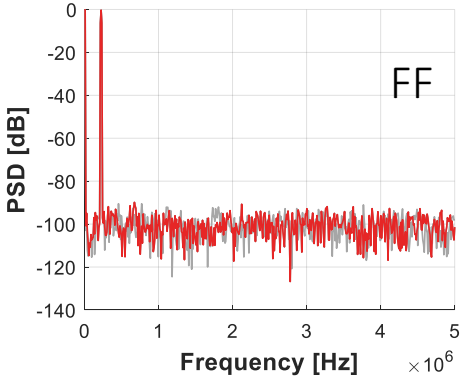
Transient and Transient Noise Across Corners

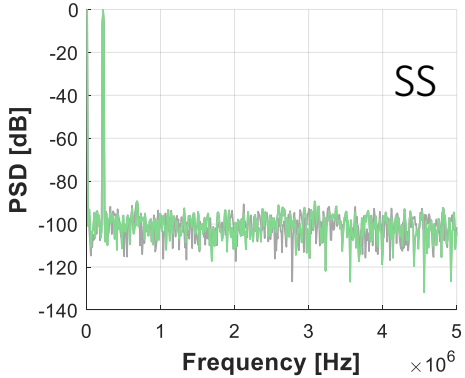
Simulation Conditions:

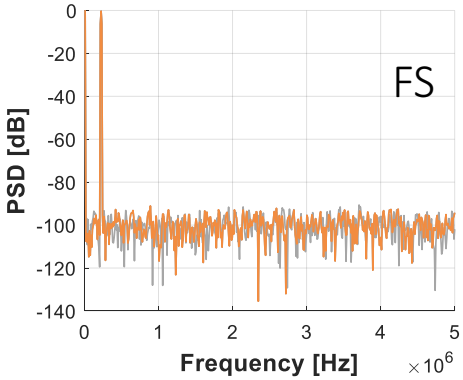
- Cu = 62fF | Base-Band MIM Capacitor Model
- Fin = 224kHz @ -0.3dBFS (1.545 Vp-p)
- FFT = 2^10 = 1024 | **Temperature = -113C**
- Corners: TT, FF, SS, FS, SF
- Fs = 10Ms/sec (140 MHz)
- Ideal Reference and Supply Voltage

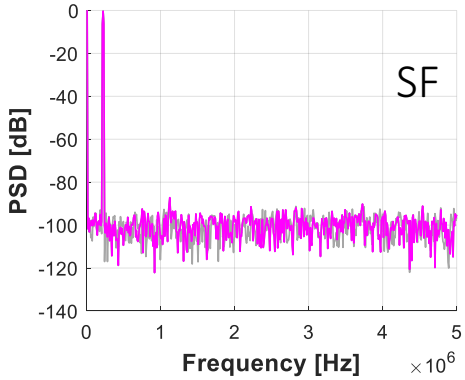
Corner	Transient		Color - Transient Noise Noise Bw: 10kHz-10GHz	
	ENOB	SQNDR	**ENOB**	**SNDR**
TT	11.89 bit	73.36 dB	**11.82 bit**	**72.91 dB**
FF	11.94 bit	73.61 dB	**11.85 bit**	**73.12 dB**
SS	11.90 bit	73.39 dB	**11.81 bit**	**72.84 dB**
FS	11.91 bit	73.45 dB	**11.80 bit**	**72.81 dB**
SF	11.90 bit	73.37 dB	**11.81 bit**	**72.88 dB**











SAR ADC Performance

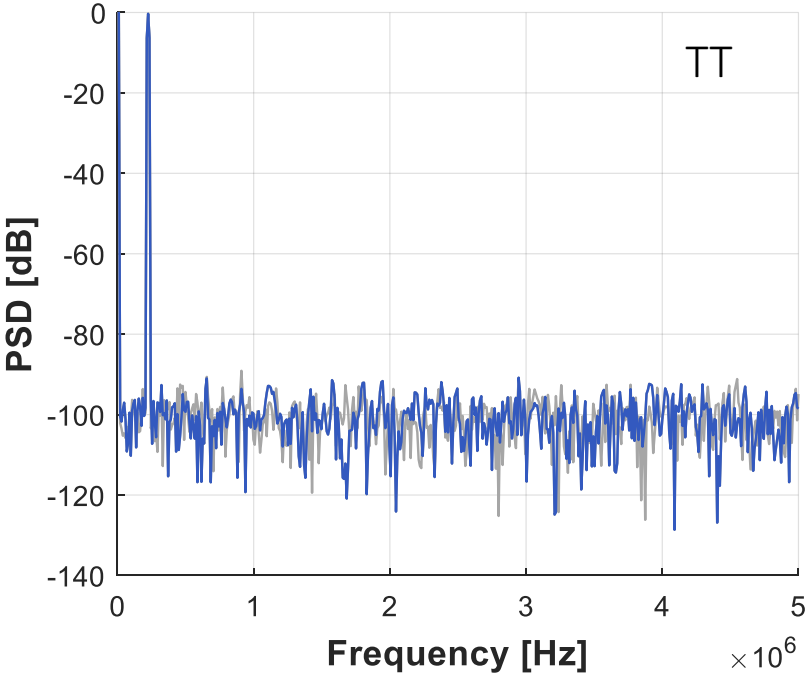
Simulation Results at -186ºC

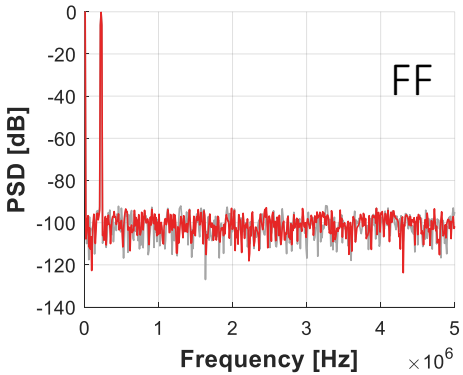
Transient and Transient Noise Across Corners

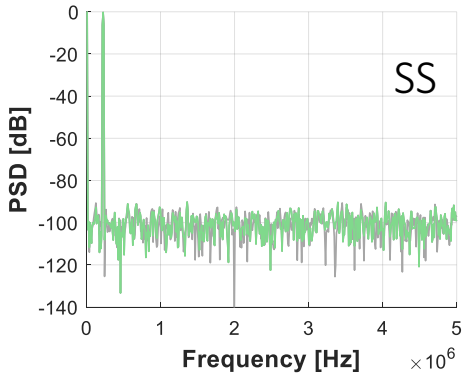
Simulation Conditions:

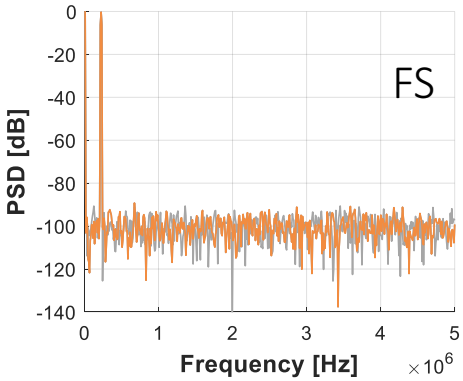
- Cu = 62fF | Base-Band MIM Capacitor Model
- Fin = 224kHz @ -0.3dBFS (1.545 Vp-p)
- FFT = 2^10 = 1024 | **Temperature = -186C**
- Corners: TT, FF, SS, FS, SF
- Fs = 10Ms/sec (140 MHz)
- Ideal Reference and Supply Voltage

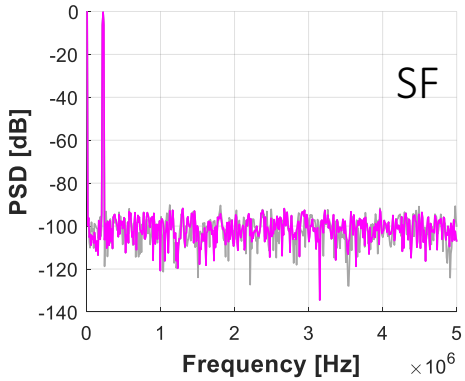
Corner	Transient		Color - Transient Noise Noise Bw: 10kHz-10GHz	
	ENOB	SQNDR	ENOB	SNDR
TT	11.93 bit	73.58 dB	**11.88 bit**	**73.30 dB**
FF	11.99 bit	73.94 dB	**11.95 bit**	**73.71 dB**
SS	11.87 bit	73.20 dB	**11.84 bit**	**73.04 dB**
FS	11.93 bit	73.60 dB	**11.88 bit**	**73.30 dB**
SF	11.92 bit	73.51 dB	**11.90dB**	**73.41 dB**











SAR ADC Performance

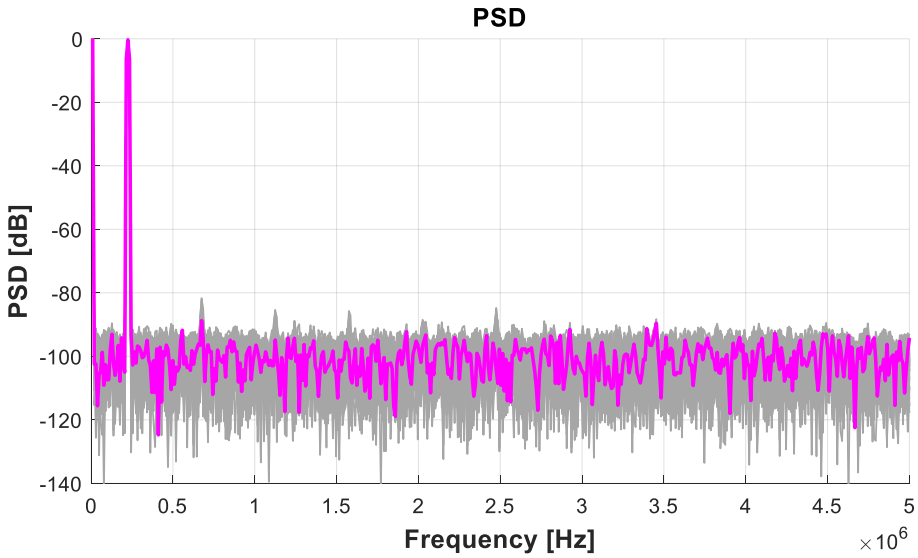
Monte Carlo Mismatch at -40ºC

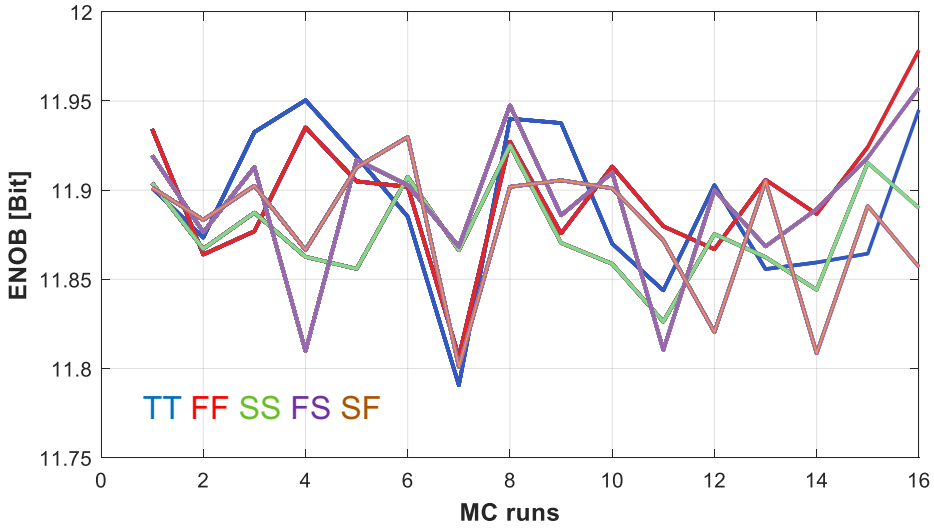
SLAC

Dynamic Test Across Corners

Simulation Conditions:

- *Devices Under Mismatch: MIM Caps, SWs and Comparator*
- Cu = 62fF | Base-Band MIM Capacitor Model
  - Kc = 1fF / um2 Capacitor Density
  - Ks = 1.5%um Capacitor Mismatch
- Fin = 224kHz @ -3dBFS (1.545 Vp-p)
- FFT = 2^10 = 1024 | **Temperature = -40C**
- 15 MC runs Across Corners: TT, FF, SS, FS, SF
- Ideal Reference and Supply Voltage





SAR ADC Performance

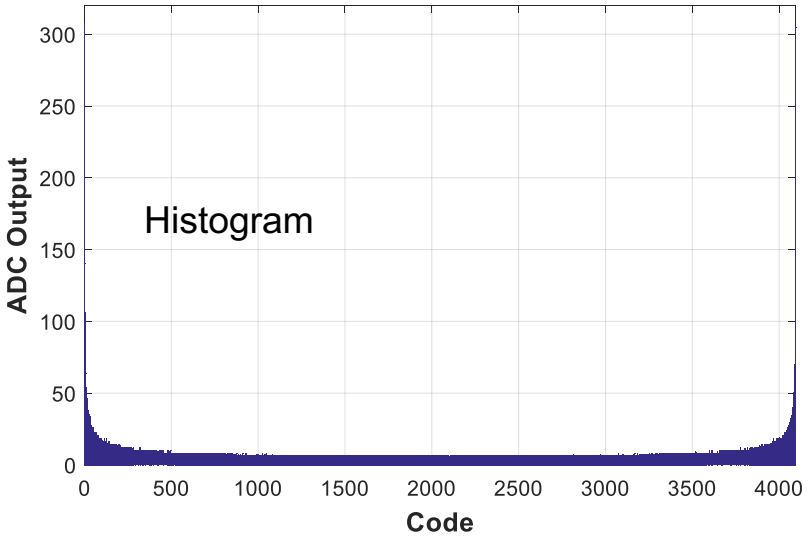
Monte Carlo Mismatch at -40ºC

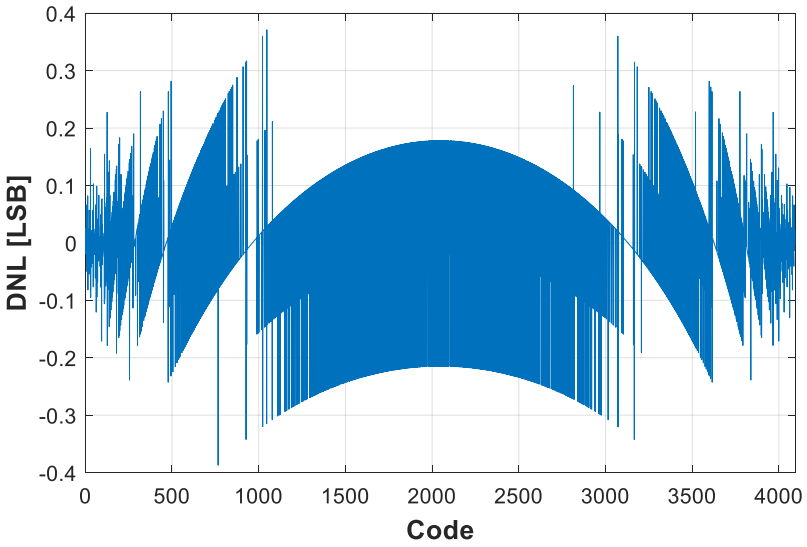
SLAC

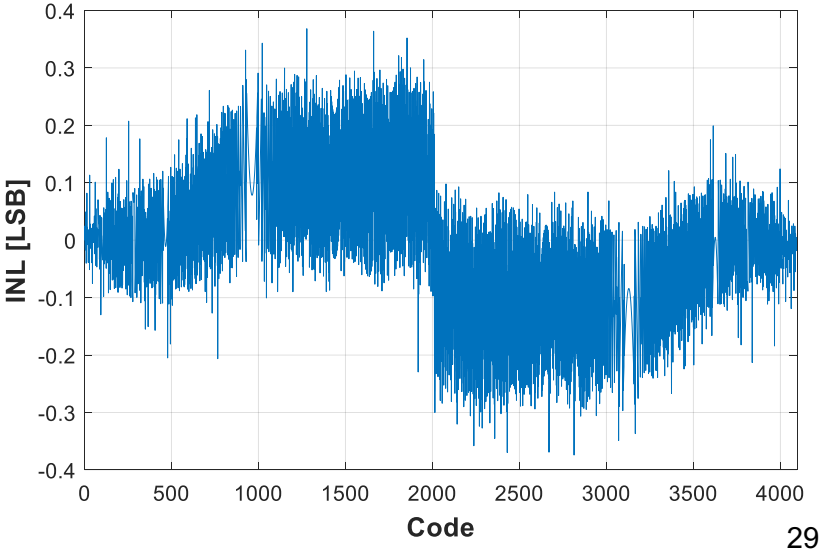
Linearity Test (Sinewave Method)

Simulation Conditions:

- *Devices Under Mismatch: MIM Caps, SWs and Comparator*
- Cu = 62fF | Base-Band MIM Capacitor Model
  - Kc = 1fF / um2 Capacitor Density
  - Ks = 1.5%um Capacitor Mismatch
- Fin = 224kHz @ -3dBFS (1.545 Vp-p)
- **FFT = 2^15 = 32768 | nper = 107 | Temperature = -40C**
- Single MC run at TT
- Ideal Reference and Supply Voltage



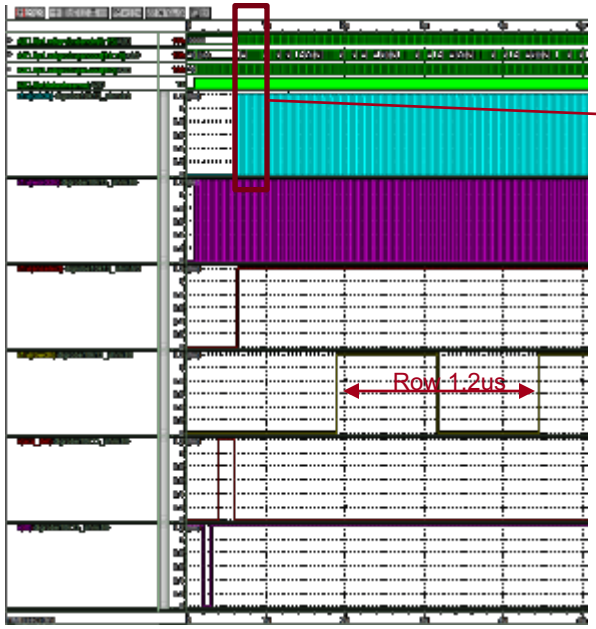


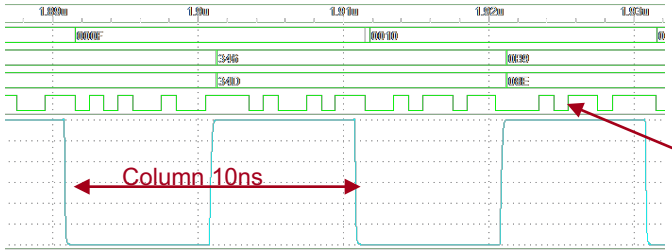


SLAC CRYO ASIC architecture

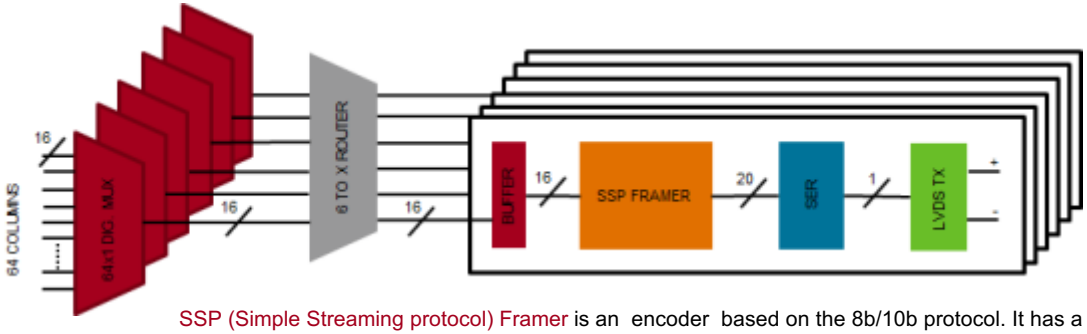
Digital back-end

ePixHR - 6 LVDS digital outputs each one multiplexing 64 columns

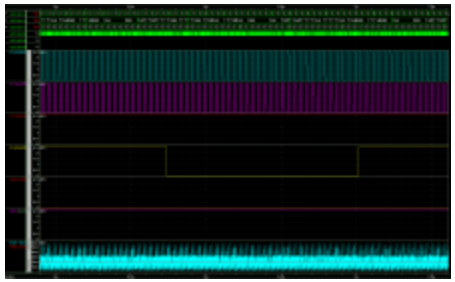




1Gb/s encoded data stream

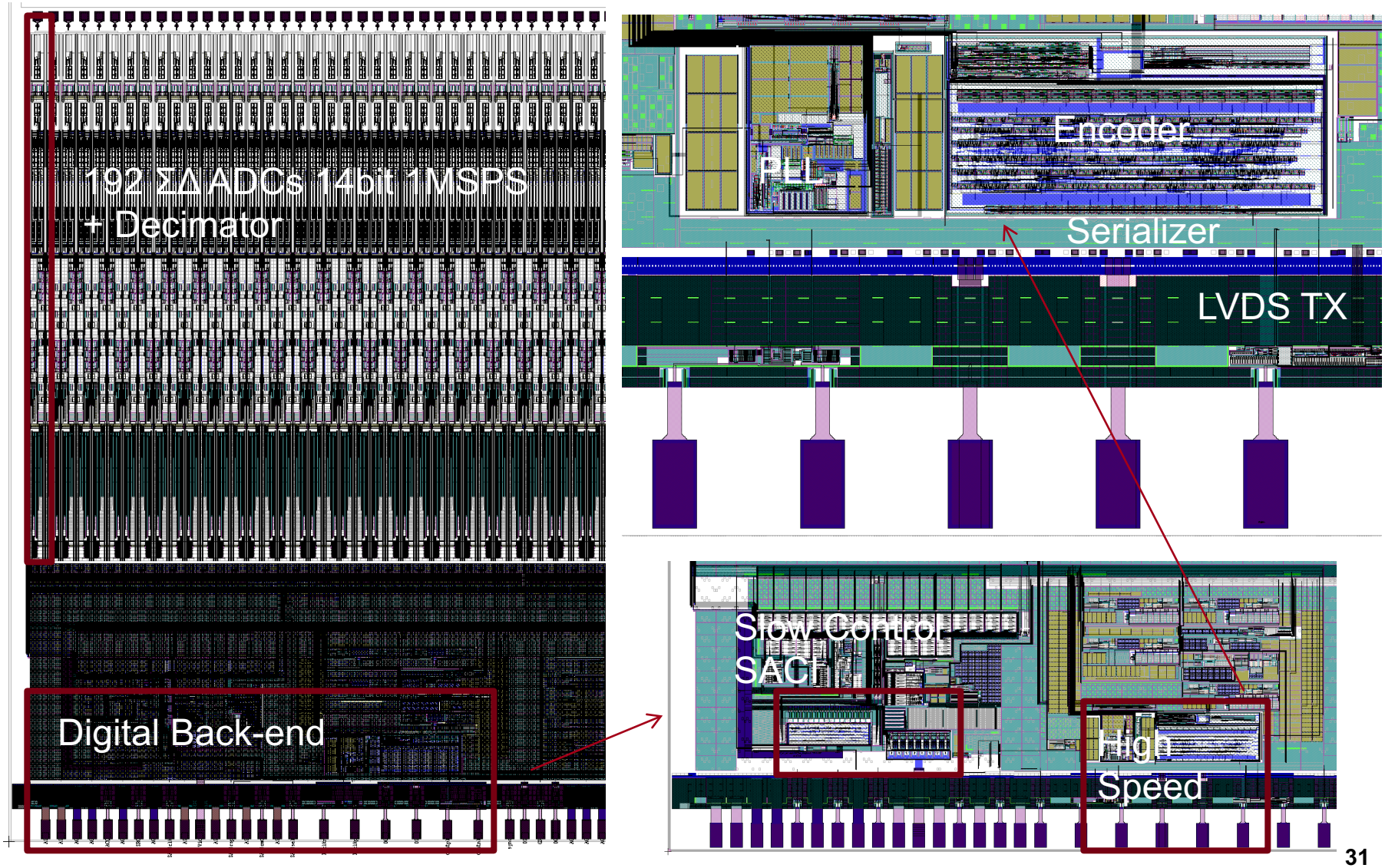


SSP (Simple Streaming protocol) Framer is an encoder based on the 8b/10b protocol. It has a defined idle code and it automatically adds a start and an end of frame code to the data.

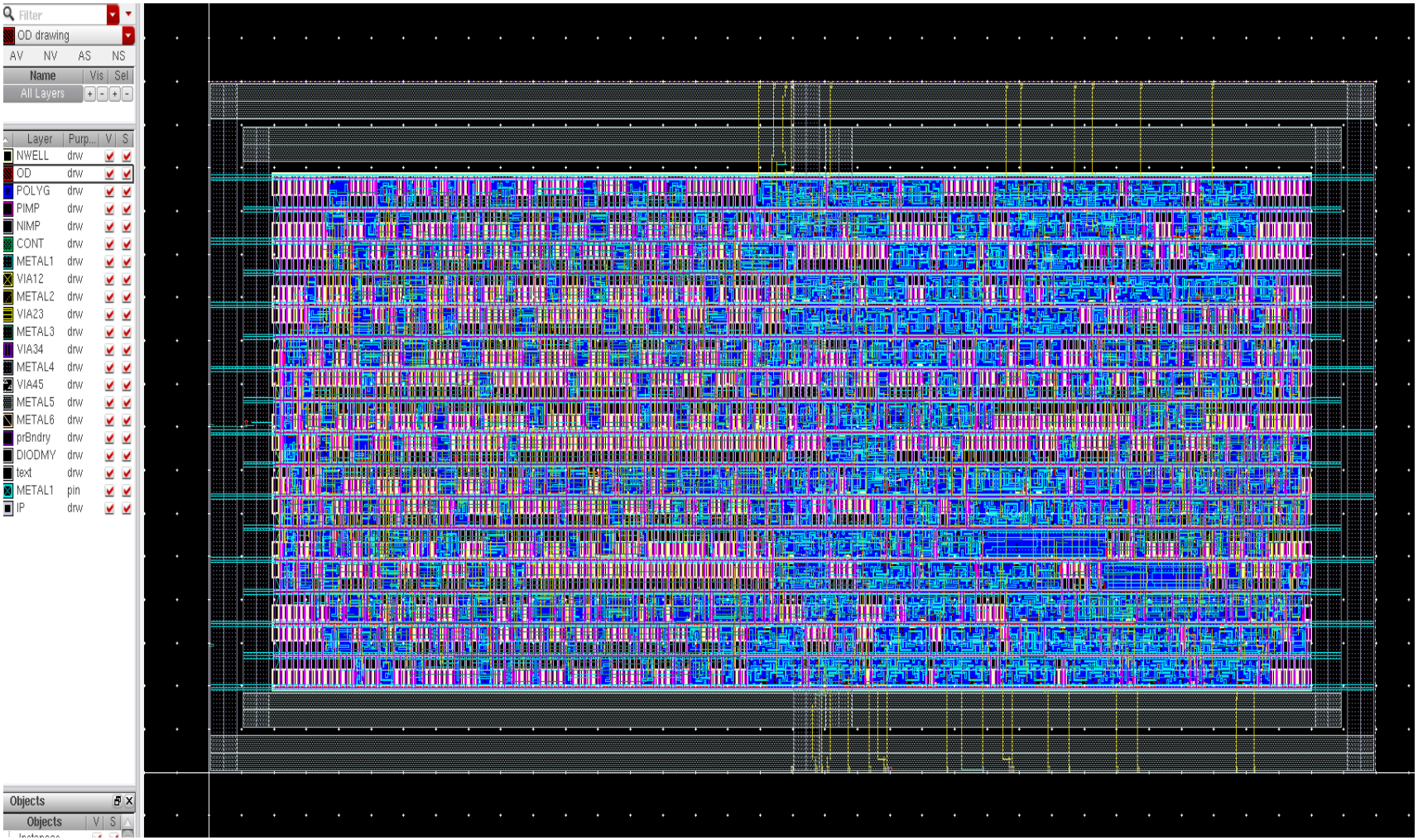


Average current consumption for 64 ch mux, encoder, serializer and transmitter 30mA @ 1Gb/s

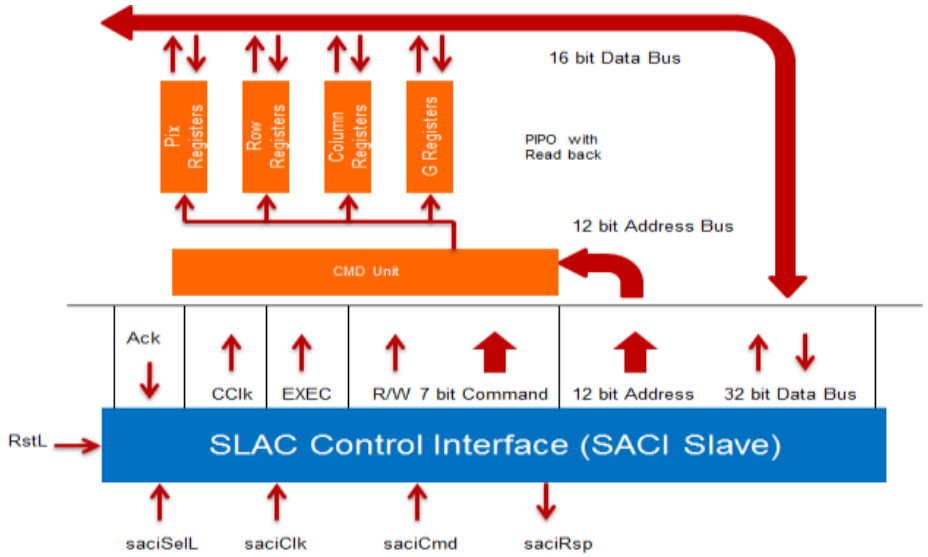
Digital back-end ePixHR



New 12b/14b encoder synthesized



SLAC ASIC Control Interface (SACI)



Master/Slave Serial Interface

4 Signals

- 3 shared: saciClk, saciCmd, saciRsp
- 1 dedicated select line per slave: saciSelL

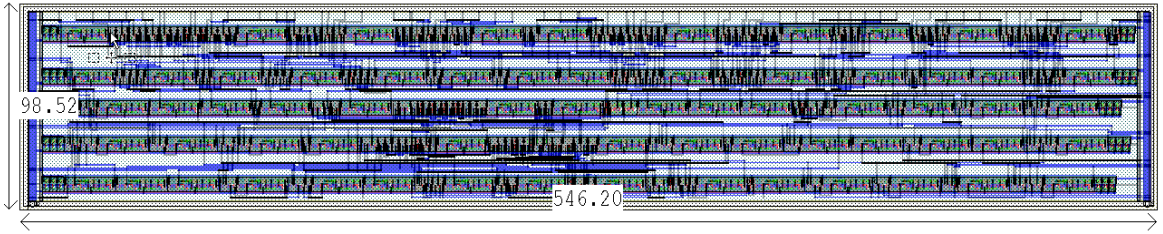
Allows multiple slaves on same SACI bus. (Similar to SPI.)

Motivation

- Need simple serial interface to ASICs for configuring registers and sending commands.

Standard Options Not a Great Fit

- SPI: No backpressure. No way for ASIC to signal that it is done with a command or ready for new data. Requires polling.
- I2C: Backpressure possible through clock stretching, but complex protocol and implementation.



- 320 Standard Cells
- 98.52 µm x 540.20 µm

Power estimate (preliminary)

SLAC

Channel x 64:

- From initial simulation ~ 1.5mA (2V domain)
  (for a potential Dune version this will go up to ~2mA)

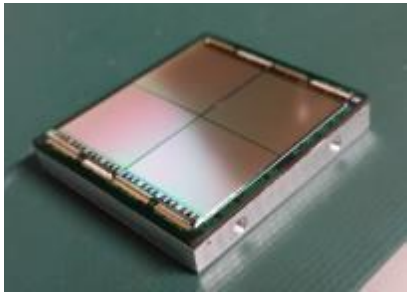
ADC x 16:

- From previous designs ~ 250uA (1.2V domain)

Encoder/Serializer/Transmitter/PLL x 2:

- From previous designs ~ 15mA (1.2V domain)

Example from a previous design



ePix100 and the ePix family:

- 28M transistors
- Analog and Digital on the same chip
- 135k pixels
- Consumption 10uW/pix
- Max signal 220ke-
- Noise 50e-

Total estimate (only listed components):

- (2V x 1.5mA x 64 + 1.2V x 250uA x 16 + 1.2V x 15mA x 2) / 64 ~ 4mW/ch

we still have margin!

(~5mW/ch for Dune version)

Where we are in the development process

- Characterization of TSMC 130nm complete
- Architecture of CRYO defined
- Front-end channel
  - Baseline architectural implementation complete
  - Antialias filter implementation complete
  - Noise studies completed
  - Variants for nEXO and Dune implemented
  - Analog channel optimization in progress
  - Layout started
- ADC
  - Design complete
  - Optimization in progress
  - Layout started
- LDOs
  - Architectural design complete
  - Noise optimization to be completed after full front-end simulation
- Back-end (SACI / PLL / Encoders / Serializers / Transmitters)
  - Reuse from previous design
  - Low temperature optimization in progress
  - 12b/14b encoder designed

Design completion is targeted before the end of the year