DP Photon System Readout - Envisioned System and DAQ Interfaces

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DUNE FD DAQ Design Workshop - Architecture considerations: Interfaces - Columbia University 30-31 October 2017

APC - Astroparticule et Cosmologie

Outline

Context

IN2P3 Collaboration

Joint effort between several In2p3 laboratories in France

Omega Microelectronics Design Center for Physics and Medical Imaging - ASIC development and testing

LAPP Particle and Nuclear Physics - PCB layout, routing and FMC board production

APC Cosmology and Astroparticle Physics - ASIC testing, PCB schematics, Firmware

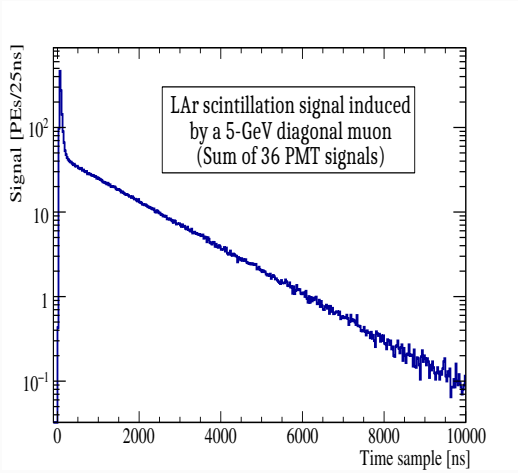
IPNL Nuclear Phycis - General support, advice and firmware

Develop (Micro)electronics front end for PMTs

Scintillating light in LAr : reference numbers (to revisit)

Time properties of light signal

Simulated data



Primary scintillation in LAr

- fast component 7ns (~23% of light)
- slow component 1.6us (~77% of light)

Falling tail constant of 500 ns
Overall signal duration of 5 us
Dynamic Range 1 to 4k PhotoElectrons

Amplitude of light signal

1 GeV neutrino ~ 1.6×10^7 photons @500V/cm

Ref: ArXiv:1408.0848

Ligh collection efficiency 0.1 %

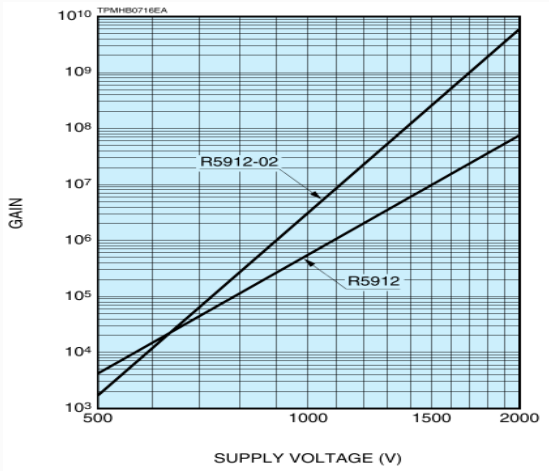
Simulated neutrino / Gev => 20k PE

500 PE/PMT/Gev neutrino (4.10^3 @ 8 Gev)

Pulse Width SPE = 20 ns.

Ip (8 Gev) = $(4.10^3) \times (1.10^6) \times (1,6.10^{-19}) / (2.20^{-9})$

Ip x 50 Ohms ~= 800 mV. ~= 100 pC.



Goals

A. Beyond ASIC functionality

Implement an PMT dedicated, latest generation ASIC

+ integrate with an state of the art Stratix IV FPGA

Advanced, non ASIC features

- Dead timeless monitoring system + digital event tagging
- Online trigger efficiency computing
- Endless (x-bits) time stamping, etc.

B. Digital Pulse Processing

Perform DPP on the samples within FPGA fabric

- Sampling of analog signals
- Computing falling tail, averaging, windowing, etc.
- Event rejection, pile up handling, etc.

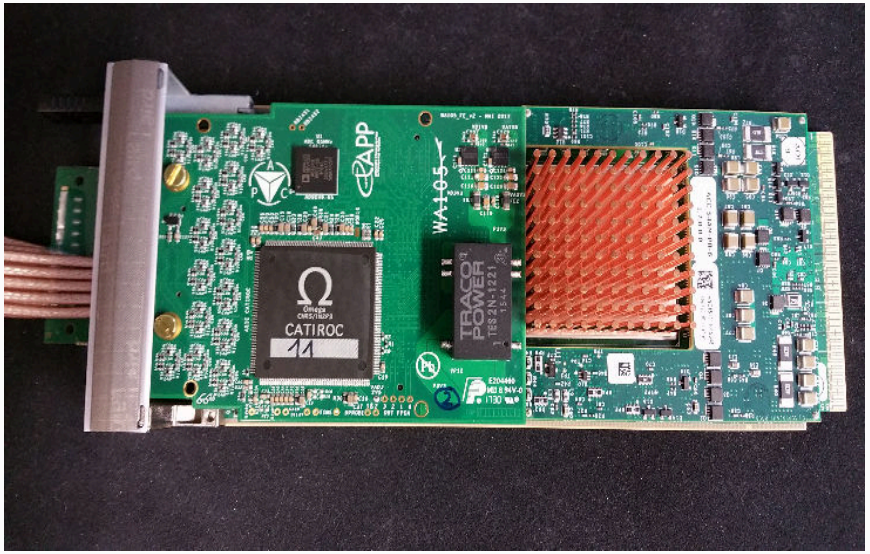
cnrs IN2P3 Les deux infinis

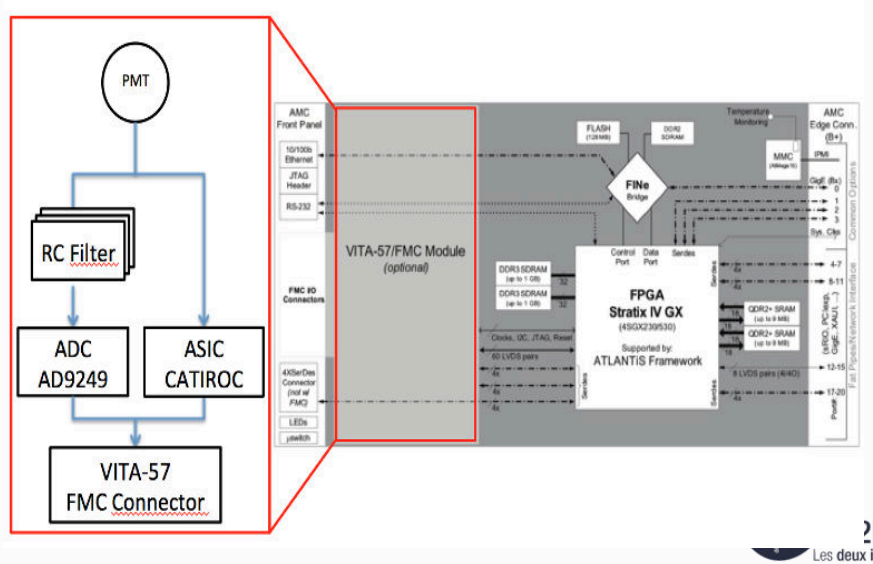
Current prototype architecture - bottom-up

Motherboard + mezzanine + sma cabling

- Splitting of 16 PMT analog inputs
- Anti aliasing, low pass filter
- VITA 57 FMC connector
- Full analog processing in dedicated ASIC
- Provides light trigger to experiment
- Readout from ASIC to FPGA
- ADC-9249, 65 MHz, 14 bits
- ADC improve measurement of charge by correlation
- Samples are merged and processed in FPGA

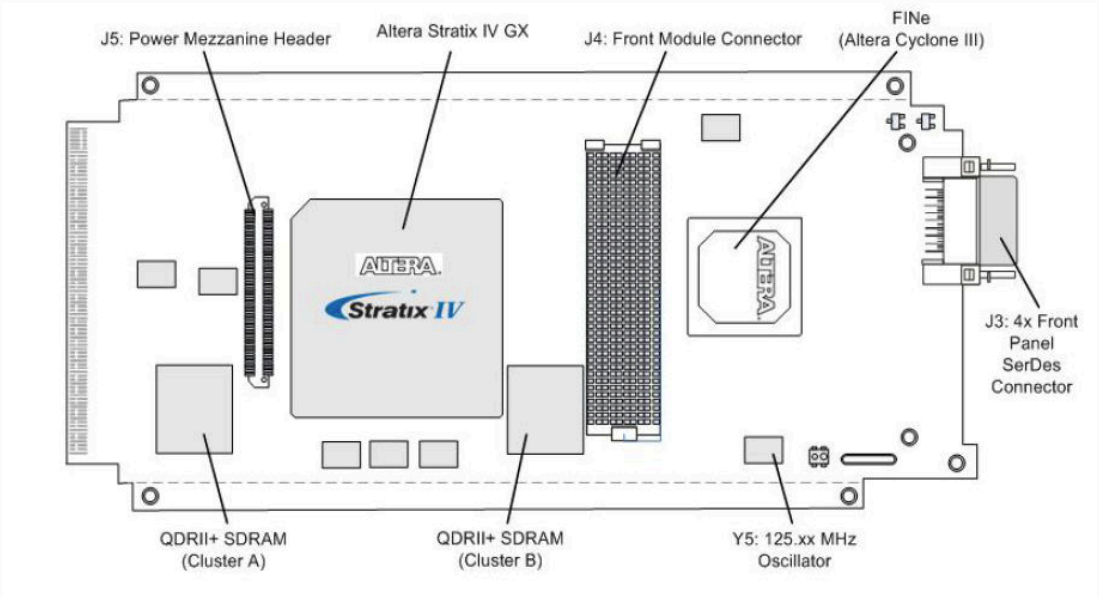
- 1 ASIC, software controlled, calibration signal conditionally replaces all analog inputs
- 4 Spare I/0 signals handle positive/negative polarity signals (-400 mV / 1.5 V, software selectable)

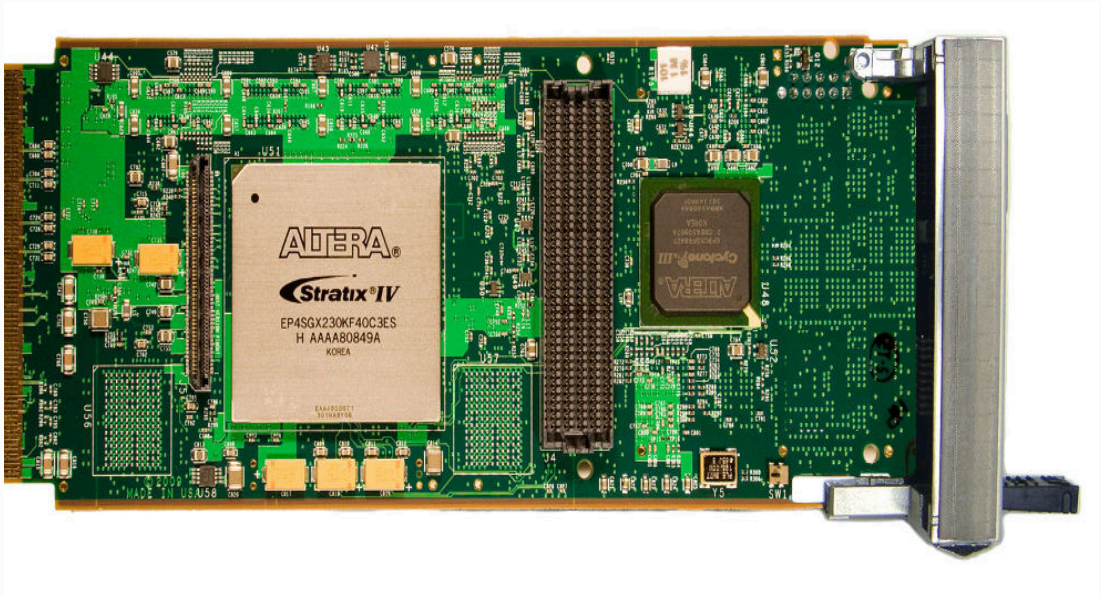




Block diagram

COTS mother board : Bittware S4 AMC

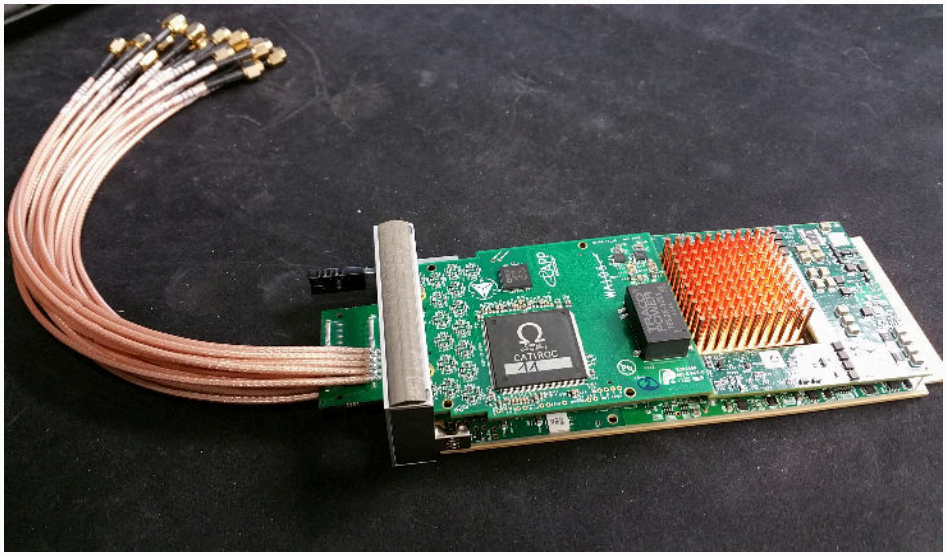




- High performance computing platform
- COTS: Reduced risk of failure
- Stable operating temperature
- Strong power supply stability

- Altera Stratix IV GX FPGA
- l BittWare FINe Host/Control Bridge
- 10/100/1000 Ethernet, SerDes, LVDS, RS-232, and JTAG
- 2 GBytes of memory
- Fully connected to AMC (16 ports SerDes, 4 ports GPIO)
- VITA 57 FMC site for I/O expansion
- Six backplane clocks

Mezzanine card



AMC unit and three mezzanines

Home made, custom design

Three units produced

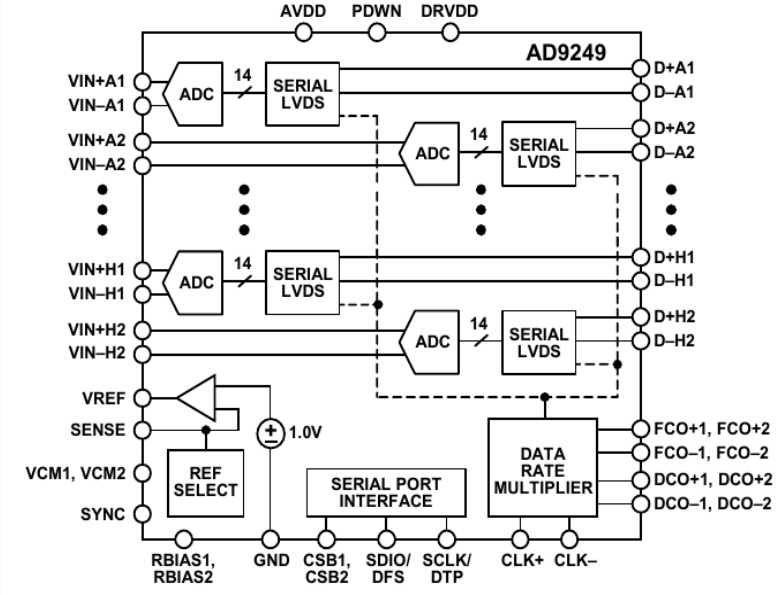
Cabling priority

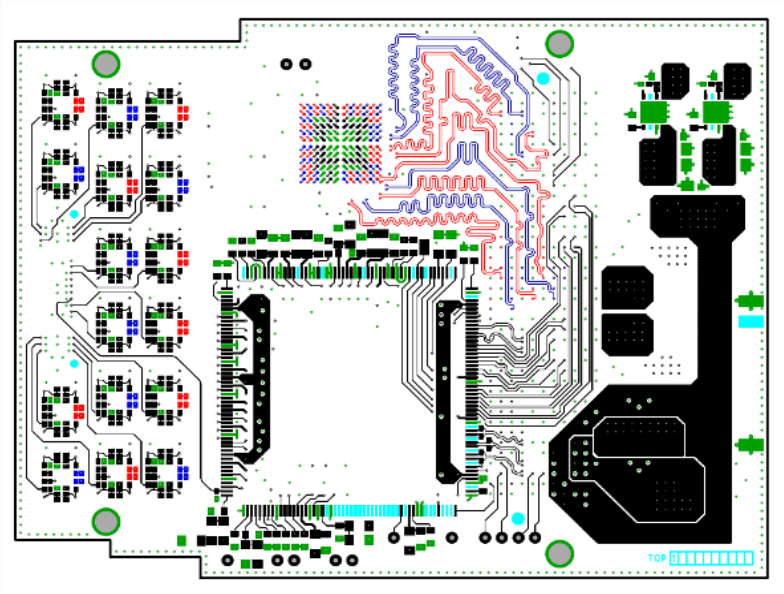
- RG393 (0,6 dB/100 feet @ 400 MHz)
- RG303 (8,6 dB/100 feet @ 400 MHz)
- RG316 (20 dB/100 feet @ 400 MHz)

Main features

- SMA, 20 channels splitter cable (16 analog + 4 spare)
- Analog frontend
- Highly integrated
- 16 channels CatiROC ASIC
- High bandwidth, 400 pins VITA 57
- 65 MHz, 14 bits ADC
- FMC form factor

Sampling ADC





65 MSPS / 650 MHz Bandwidth

16 data out lines, fully differential

Serial LVDS

2 Vp-p - 14 bits - 75 dBFS SNR

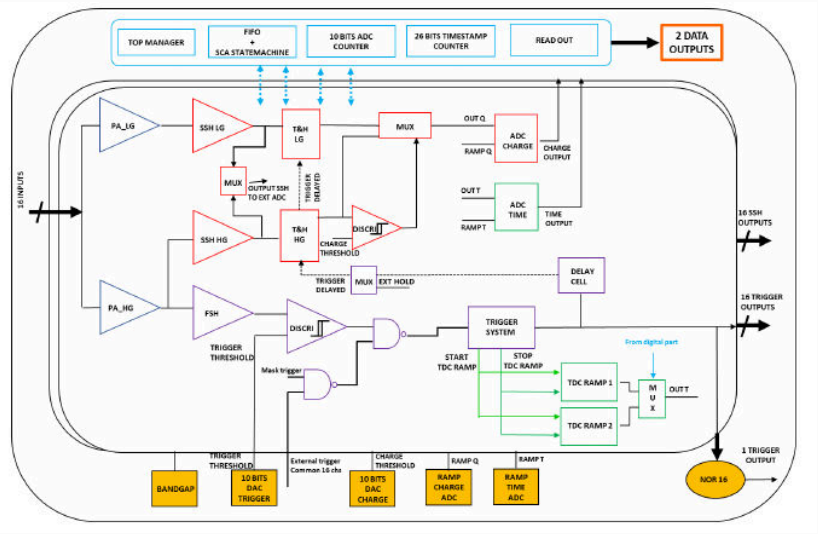
DNL $<$ 0.6 LSB; INL $<$ 0.9 LSB

- AD9249, fully configurable device
- Low voltage & low power
- Small footprint
- Configurable sampling frequency
- Anti aliasing filter necessary
- Capture FCO, DCO and clock available
- SPI Serial port control for slow control

Sophisticated routing

CatiROC ASIC - AMS SiGe 0.35 um - 13.2 mm2

Detailed datasheet available at omega.in2p3.fr



Detector Read-Out	PMTs
Number of Channels	16
Signal Polarity	negative
Sensitivity	voltage
Timing	**Time stamp: 26 bits counter @40 MHz** **Fine time**: resolution < 100 ps (simulation) A TDC ramp for each channel
Charge Dynamic Range	160 fC up to 100pC
Trigger	Triggerless acquisition Noise= 5 fC; Minimum threshold= 25 fC (5σ)
Digital	**Conversion: 10 bits** ADC at **160 MHz** **Two Read out: 80 MHz** Read out frame: **50 bits** 2 frames of (29+21) bits 1st frame/8chs: Ch nb= 3; coarse time= 26 2nd frame/8chs: Gain used= 1; Charge converted= 10, Fine time converted= 10
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm
Power Consumption	30 mW/channel
Outputs	16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurement over 10 bits
Main Internal Programmable Features	Variable preamplifier gain Shaping time of the charge shaper (variable shaping and gain) Common trigger threshold adjustment Common gain threshold adjustment

- 328 bits, slow control 1-bit shift register
- Fast channel for trigger and time measurement
- Slow channel for charge measurement
- Two capacitors for dead time reduction
- Ch. discriminator output / analog probe

- Ch. dynamic range 160 fC / 70 pC PA Gain of 20
- Measured timing around 200 ps.
- Low gain / high gain modes.

CatiROC facts

16 channels readout chip for PMTs with fully independent charge and time measurements

16 negative inputs: each voltage input is sent to high/low noise amplifiers for small and large signals to ensure a good charge precision (30 fC)

Variable 8 bit gain / amplifier / channel

Charge: preamp followed by 2 variable slow shapers sent to analog memories to measure up to 50pC

Time: coarse + fine timing

10 bits Wilkinson ADC to convert charge and fine time @ 160 MHz

Dead time ~ 5 us.

2 x 16 effective channels (two capacitors)

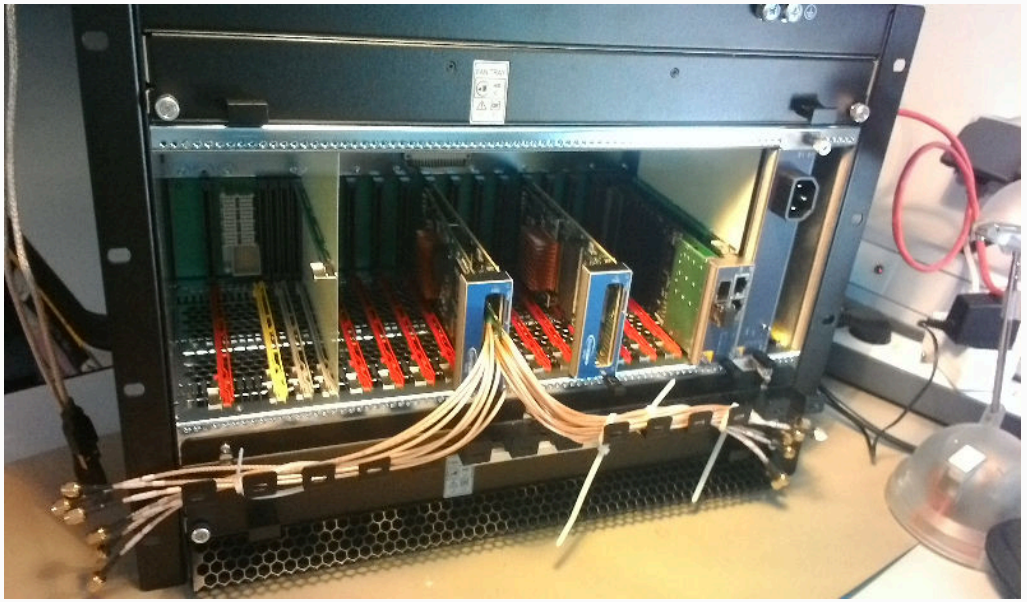
A fast shaper / channel followed by a discri for auto-trigger

Digital section handles the acq, conversion and readout, providing a 26 bits coarse time measurement (TS)

. . . but only one common, leading edge 10 bit threshold

Planned developments

System Level Architecture



Once the current design is validated

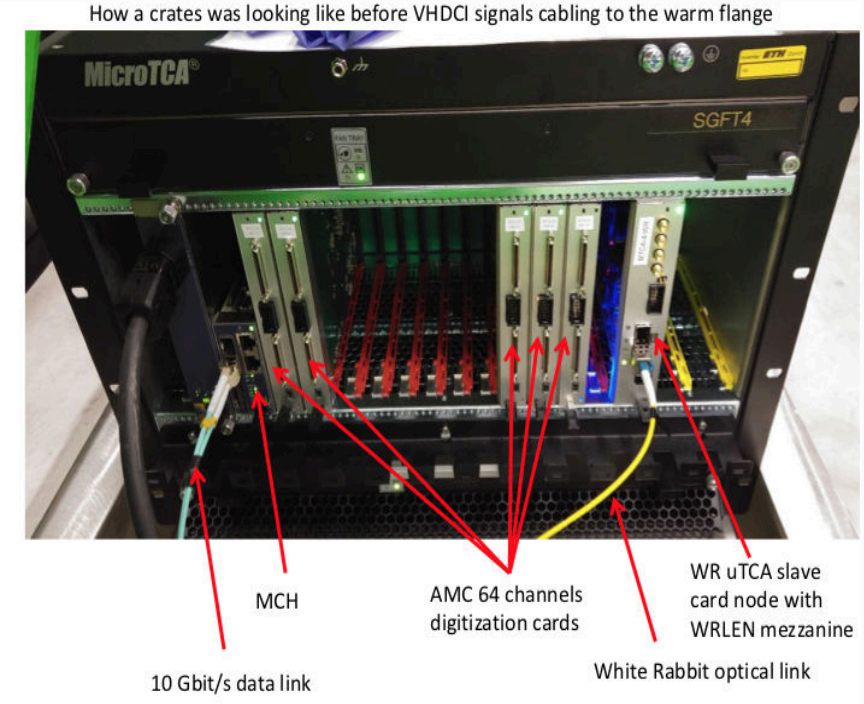
- Full NAT uTCA crate
- 10 AdvancedMC (AMC), double width slots
- 2 redundant MCH controller
- 1 AMC dedicated card for synchronizing
- 1 AMC dedicated card for trigger ORing

Home made hardware with 2 ASICs + 2 ADCs => 32 channels

Architecture compatible with charge readout DAQ

Global working mode - Synchronization

To be integrated in charge readout global DAQ.



Developed by / image from IPNL

32-Channels In sync within the same AMC hardware

AMC Units Each AMC mother board takes a clock through the uTCA backplane

Crate Sync A dedicated White Rabbit, uTCA slave node acts as a sync receiver, distributing clocks to the back plane

System sync All system electronics are in sync using White Rabbit and dedicated receiver units

Data readout Through the data link

Trigger distribution & scalability

32 channels x 11 slots = 352 channels / uTCA crate

All channels run synchronously, all events are time stamped

Integrated with the charge readout electronics via the common time base and the back-end receiving the data

32-Channels	Triggerless mode, with locally generated triggers (discriminator output of leading edge on fast shapper channel within the CatiROC ASIC)
AMC local trigger	ORing of all 32 triggers within the FPGA; output through spare outputs
Crate trigger	Daisy chain / star readout of AMC local triggers
System trigger	Global OR trigger of all channels

Triggerless operation or during beam time in an external trigger mode via white rabbit

Several crates in sync with the dedicated AMC slave node

Conclusions

Summary

- Work in progress ...
- Currently three 16 channels units
- Doing the firmware / software
- CatiROC fully characterized and understood

ADC Charge Measurement	14 bits	65 MHz
CatiROC ASIC	Analog processing	Time + Charge
Stratix IV FPGA	2 GB Memory	FMC
Event size	10 bytes	Customizable