

6x6x6 - Description of the light trigger and DAQ system; characteristics of the FEE

Cayetano Santos - On behalf of the IN2P3 group
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APC - Astroparticule et Cosmologie

CatiROC ASIC

Implement an PMT dedicated, latest generation ASIC
+ integrate with an state of the art Stratix IV FPGA

Advanced, non ASIC features

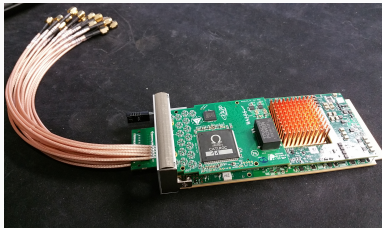
- Dead timeless monitoring system + digital event tagging
- Online trigger efficiency computing
- Endless (x-bits) time stamping, etc.

ADC Sampling

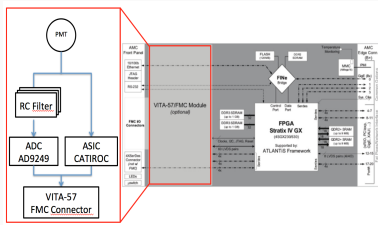
Perform DPP on the samples within FPGA fabric

- Sampling of analog signals
- Computing falling tail, averaging, windowing, etc.
- Event rejection, pile up handling, etc.

Mother board + Mezzanine



AMC + mezzanine / Block diagram



- Splitting of 16 PMT analog inputs
- Anti aliasing, low pass filter
- FMC connector / Mother board Bittware S4AM
- Dedicated ASIC, software controlled
- Full analog processing
- Readout from ASIC to FPGA
- Provides light trigger to experiment
- ADC to improve measurement of charge
- Samples are merged and processed in FPGA
- 4 Spare I/O signals



Home made, custom design

Three units produced

Features

- SMA, 20 channels splitter cable (16 analog + 4 spare)
- Analog frontend
- 16 channels CatiROC ASIC
- High data bandwidth, 400 pins VITA 57
- 65 MHz, 14 bits ADC
- FMC form factor

65 MSPS / 650 MHz Bandwidth

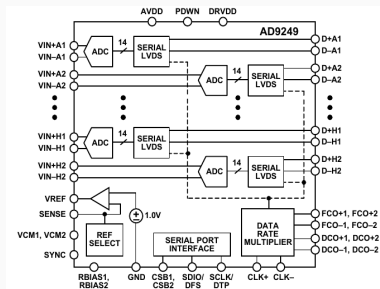
16 data out lines, fully differential

Serial LVDS

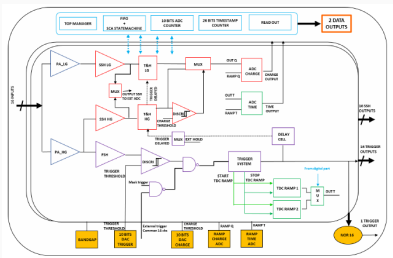
2 V_{p-p} - 14 bits - 75 dBFS SNR

DNL < 0.6 LSB; INL < 0.9 LSB

- AD9249, fully configurable device
- Low voltage & low power
- Small footprint
- Capture FCO, DCO and clock available
- SPI Serial port control for slow control
- Configurable sampling frequency
- Anti aliasing filter necessary



Detailed datasheet available at omega.in2p3.fr



- 328 bits, slow control 1-bit shift register
- Fast channel for trigger and time measurement
- Slow channel for charge measurement
- Two capacitors for dead time reduction
- Ch. discriminator output / analog probe

| | |
|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Detector Read-Out | PMTs |
| Number of Channels | 16 |
| Signal Polarity | negative |
| Sensitivity | voltage |
| Timing | Time stamp: 26 bits counter @ 40 MHz Fine time: resolution < 100 ps (simulation) A.TDC ramp for each channel |
| Charge Dynamic Range | 160 fC up to 100pC |
| Trigger | Triggerless acquisition Noise= 5 fC; Minimum threshold= 25 fC (5 σ) |
| Digital | Conversion: 10 bits ADC at 160 MHz Two Read out: 80 MHz Read out frame: 50 bits 2 frames of (29+21) bits 1st frame/8chs: Ch nbr= 3; coarse time= 26 2nd frame/8chs: Gain used= 1; Charge converted= 10, Fine time converted= 10 |
| Packaging & Dimension | TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm |
| Power Consumption | 30 mW/channel |
| Outputs | 16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurement over 10 bits |
| Main Internal Programmable Features | Variable preamplifier gain Shaping time of the charge shaper (variable shaping and gain) Common trigger threshold adjustment Common gain threshold adjustment |

- Ch. dynamic range 160 fC / 70 pC PA
Gain of 20
- Measured timing around 200 ps.
- Low gain / high gain modes.

16 channels readout chip for PMTs - fully independent charge and time measurements

16 negative inputs: each voltage input is sent to high/low noise amplifiers for small and large signals to ensure a good charge precision (30 fC)

2 x 16 effective channels (two capacitors)

Charge: variable 8 bit gain / amplifier / channel

Preamp followed by 2 variable slow shapers sent to analog memories to measure ~ 100 pC

Variable / fixed gain scales

Time: coarse + fine timing

10 bits Wilkinson ADC to convert charge and fine time @ 160 MHz; dead time ~ 5 us.

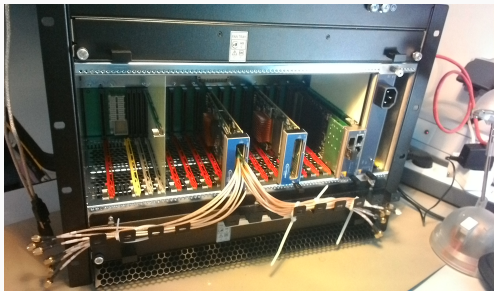
A fast shaper / channel followed by a discrim for auto-trigger

Digital section handles the acq, conversion and readout, providing a 26 bits coarse time measurement (TS)

Maximum input amplitude

Around ~ 700 mV.; beyond, coupling between channels

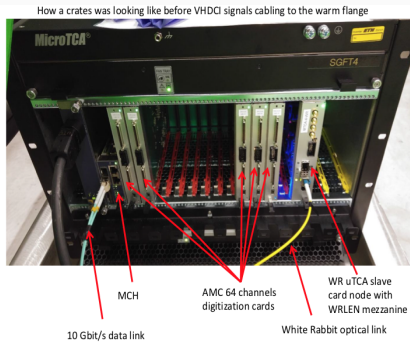
... but only one common, leading edge 10 bit threshold



- Full NAT uTCA crate
- 3 AdvancedMC (AMC) slots
- 1 MCH controller
- 1 AMC dedicated card for synchronizing
- Trigger ORing

Architecture compatible with charge readout DAQ

To be integrated in charge readout global DAQ.



Developed by / image from IPNL

12-Channels In sync within the same AMC hardware

AMC Units Each AMC mother board takes a clock through the uTCA backplane

Crate Sync A dedicated White Rabbit, uTCA slave node acts as a sync receiver, distributing clocks to the back plane

System sync All system electronics are in sync using White Rabbit and dedicated receiver units

Data readout Through the data link

12 channels x 3 slots = 36 channels / uTCA crate

All channels run synchronously, all events are time stamped

Integrated with the charge readout electronics via the common time base and the back-end receiving the data

12-Channels Triggerless mode, with locally generated triggers (discriminator output of leading edge on fast shapper channel within the CatiROC ASIC)

AMC local trigger ORing of all 12 triggers within the FPGA; output through spare outputs

Crate trigger Daisy chain / star readout of AMC local triggers

System trigger Global OR trigger of all channels

Triggerless operation or during beam time in an external trigger mode via white rabbit

Several crates in sync with the dedicated AMC slave node