Building the CMS Pixel Barrel Detector: Assembling, Testing and Integration

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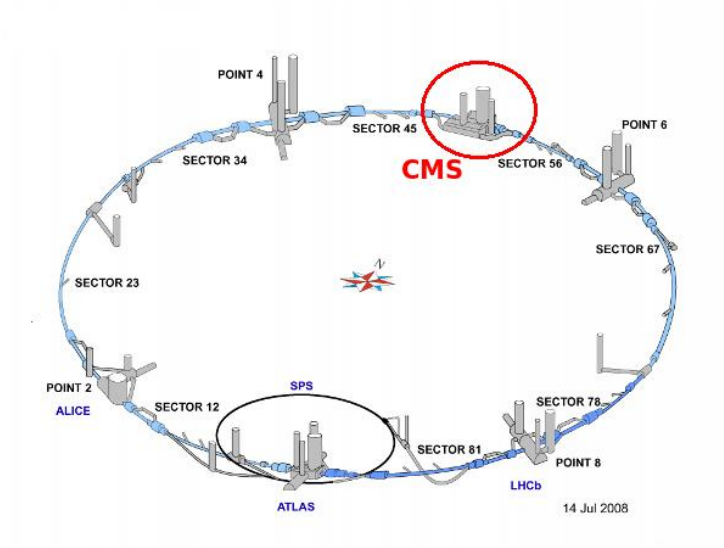
Outline

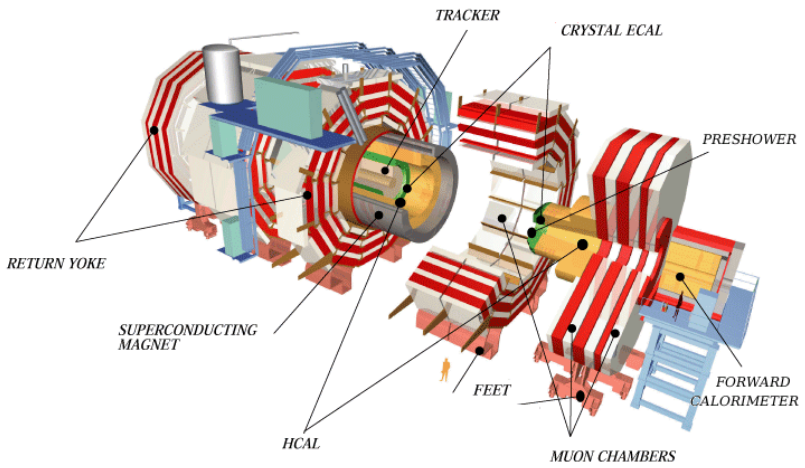
- Introduction: what is the CMS Barrel Pixel Detector?
- Assembling modules: components, main steps and experience
- Testing modules: test procedures and results
- Integration barrel pixel detector: mounting modules and integration of services
- Conclusions: what did we learn?

CMS at LHC



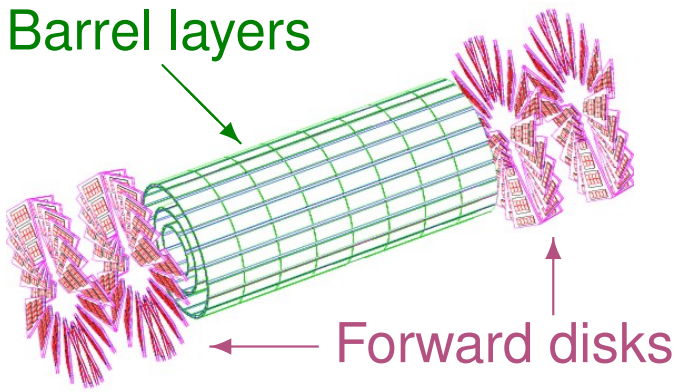
LHC:

- 27 *km* ring, 1232 superconducting (1.9 *K*) dipoles
- $p - p$ collider, 7 *TeV* each beam
- nominal luminosity $10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, rate 40 *MHz*



CMS:

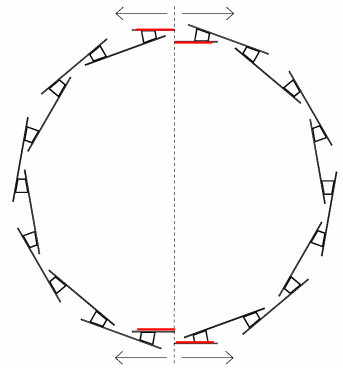
- Length 22 *m* , diameter 15 *m*, weight 12.5 kton
- Magnetic field 3.8 Tesla



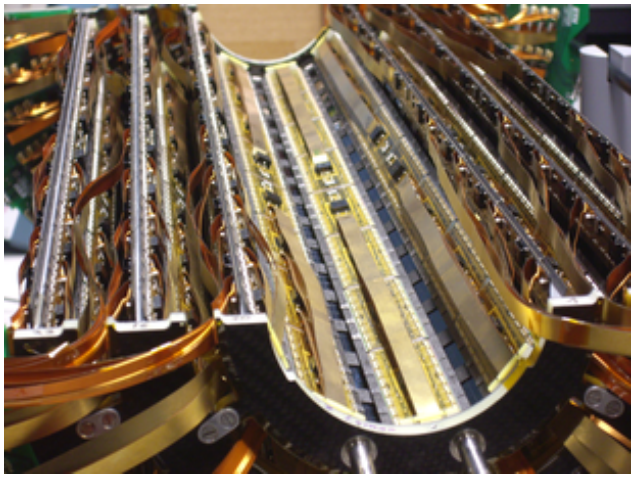
CMS Pixel:

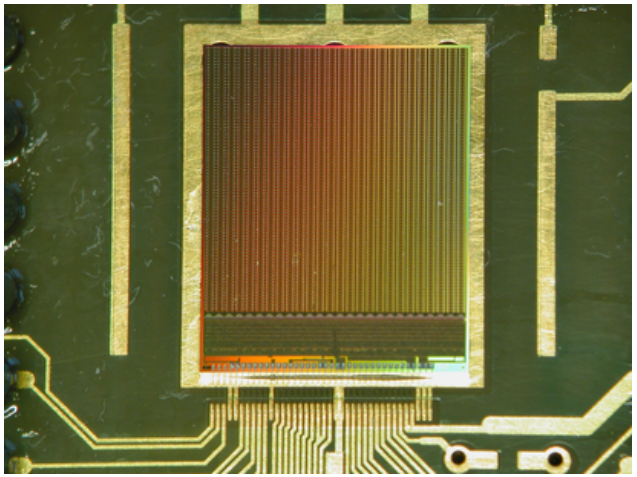
- Barrel layers: $l = 53\ cm$, $R = 4.2,\ 7.3,\ 11\ cm$
- Forward disks: $z = 34.5, 46.5\ cm$, $R = 6 \div 15\ cm$
- Area $\sim 1.1\ m^2$, 15840 ROCs, 65.9M channels

Barrel pixel detector

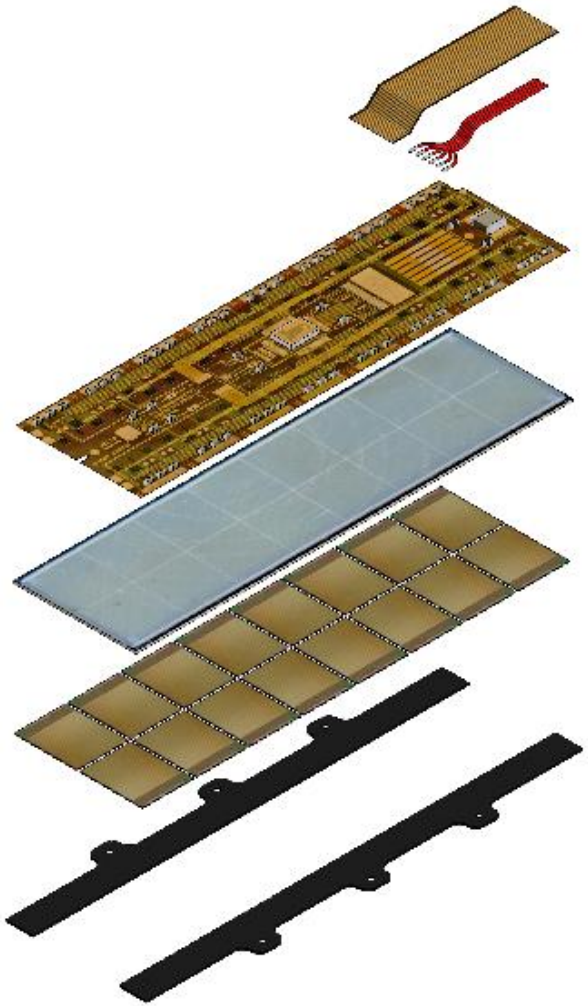


- Barrel pixel detector is built of 768 modules:
  - full modules (16 ROCs): 672=128+224+320
  - half modules (8 ROCs): 96=3x32
- Read Out Chip:
  - Each ROC is segmented in 4160 pixels
  - Pixels in a ROC organized in 26 double columns (z) and 80 rows ($r - \phi$)
  - Pixel size: 100 μ in $r - \phi$ and 150 μ in z
  - 29 DACs are used to tune a ROC





Break-up of the module



Cables: signal&power

HDI print

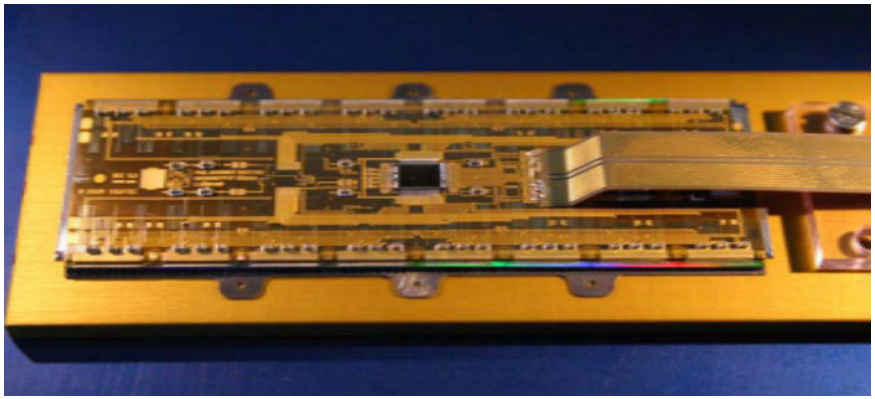
Si sensor

16 ROCs

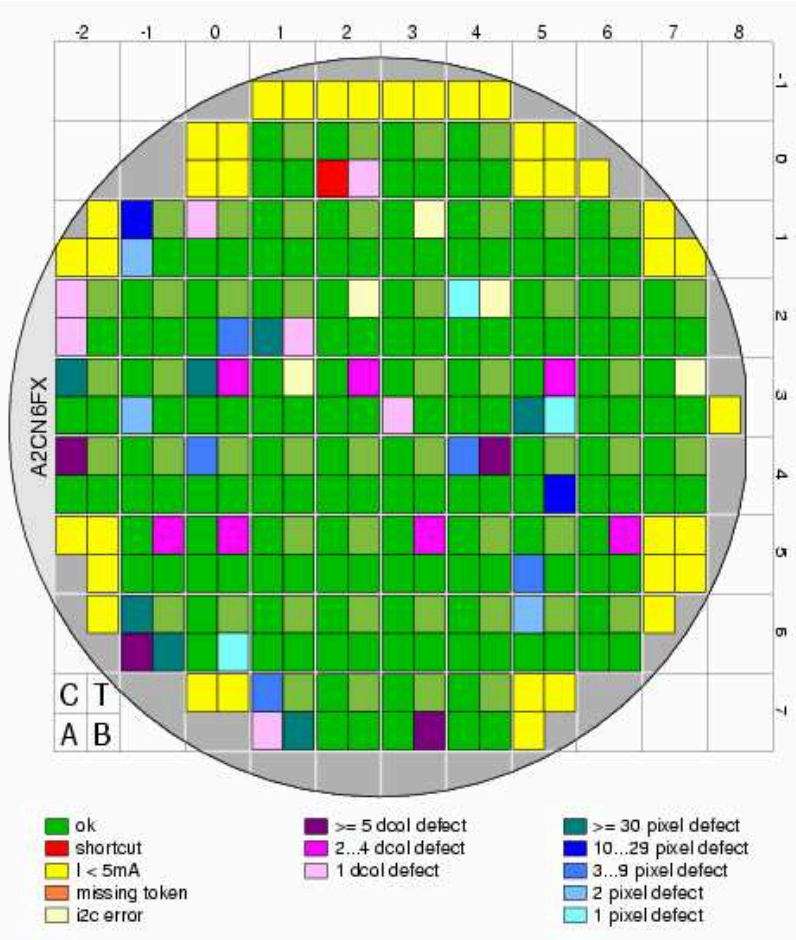
Base strips: Si_3N_4

Module parameters:

Size: 66.6 mm $\times$ 26 mm
Weight: 3.5 g
Segmentation: 66560 pixels
Si sensor thickness: 285 μ

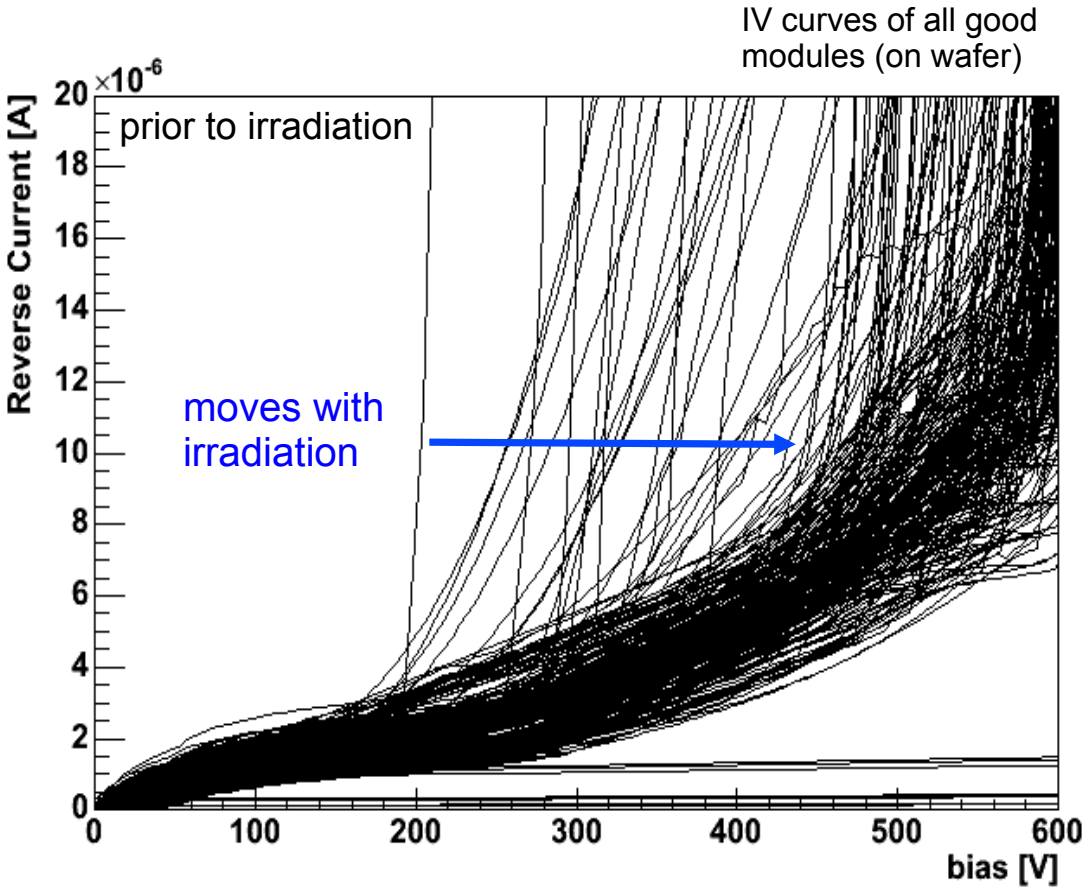


Chips testing at wafer level



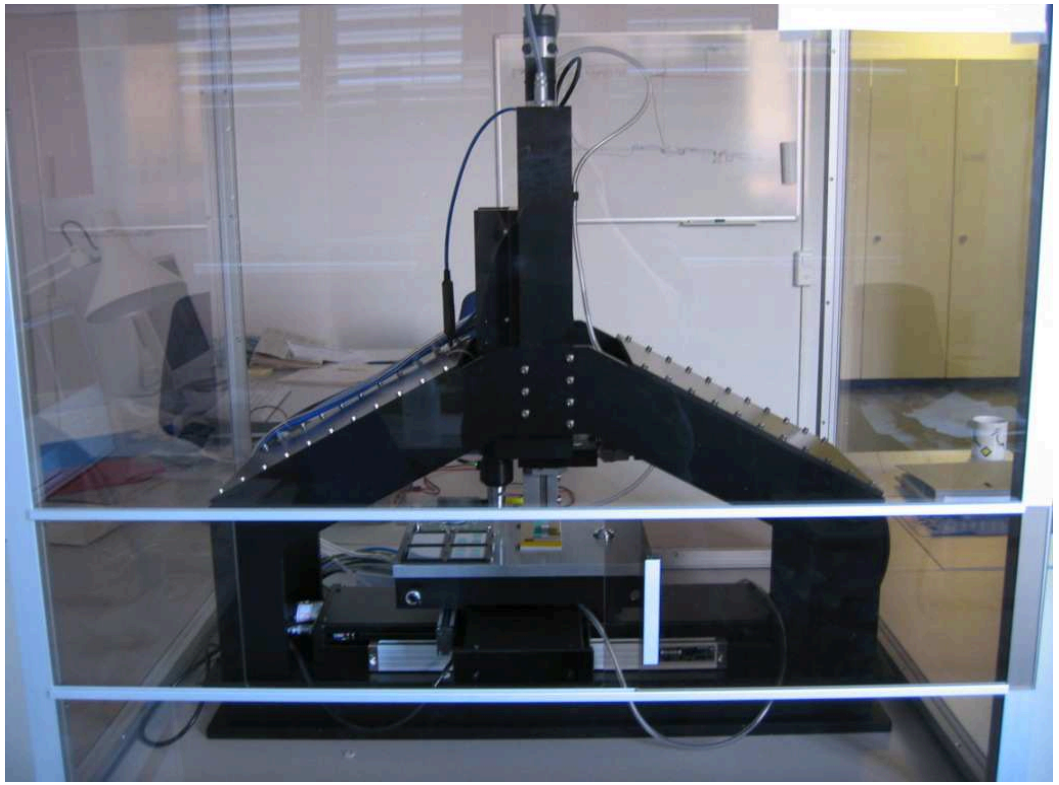
- Automated Suss Prober (8”):
- Test procedure
  - Threshold scan for all pixels
  - Test all DACs
  - Check all trim bits & mask
  - Check all data buffers
  - Check all time stamp buffers
  - Check power consumption
- 400K I2C commands to ROC
- Time 70 sec/chip, 1 wafer/day
- Average yield 74%

BPix sensors

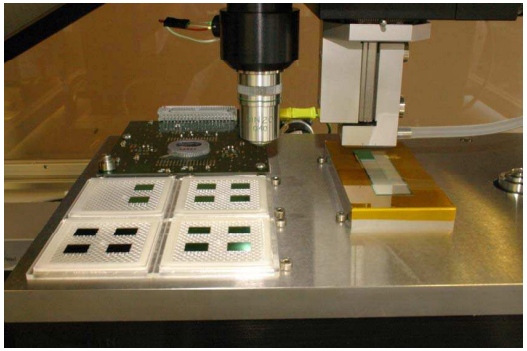


- 3 full modules / wafer
- Sensor specifications:
  - same ingot ($V_{depl} \sim 55 \div 65$ V)
  - I(150V)< 2μA
  - I(150V)/I(100V)<2
- Sensors lost:
  - 10% in bump deposition and cutting
  - 5% in module production

Chip-sensor bump bonding

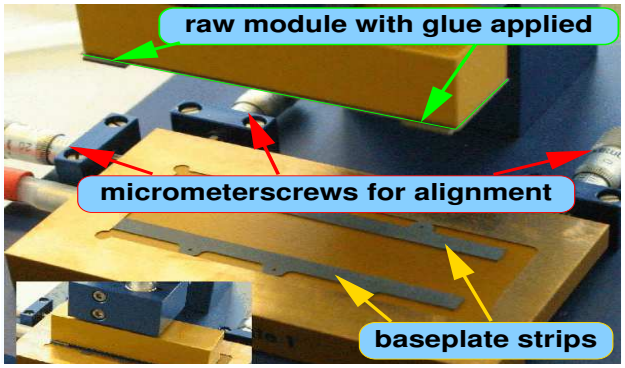


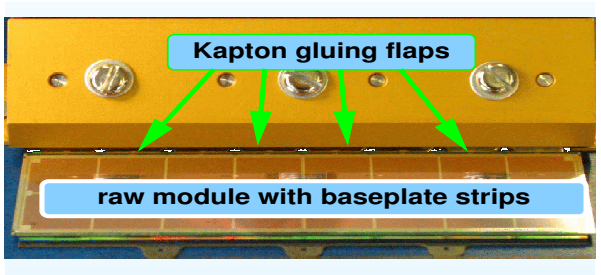
- Precision: $1 \div 2\,\mu\mathrm{m}$
- Production rate:
  - 6 modules / day + tests
  - automated: 1 hr/module
- Bare module test:
  - IV-curve
  - ROC functionality
  - bump yield
  - rework: 80% success

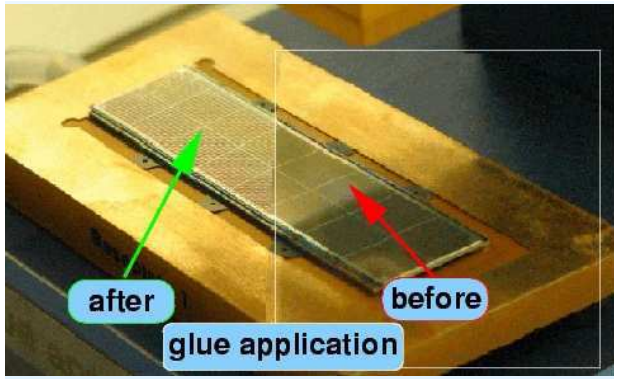


Assembly line

- Production rate:
  - 4 full + 2 half modules / day
  - or 6 full modules / day
- Three glueing steps:
  - glue basestrips to raw module
  - underfill sensor with glue
  - glue HDI to complete assembly
- Important: custom-made tools

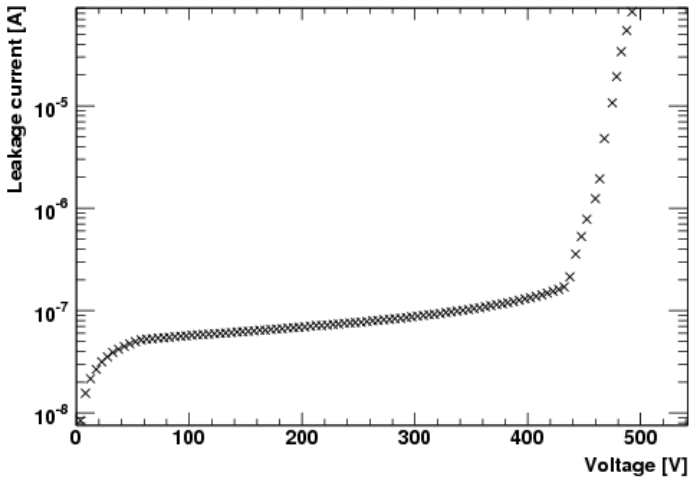


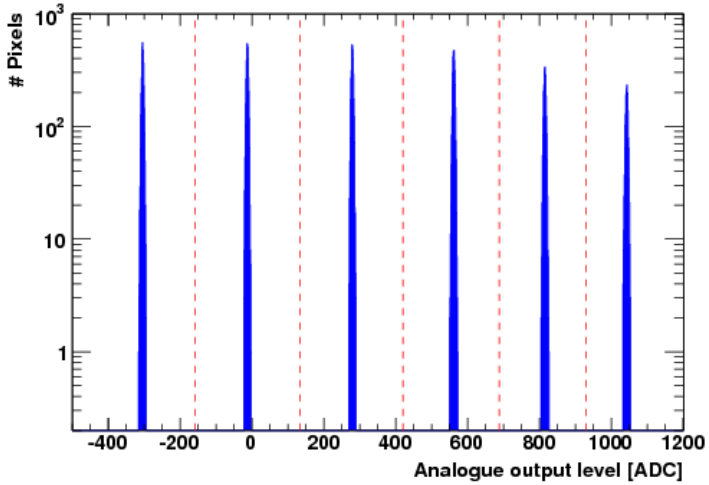




Module test classifications

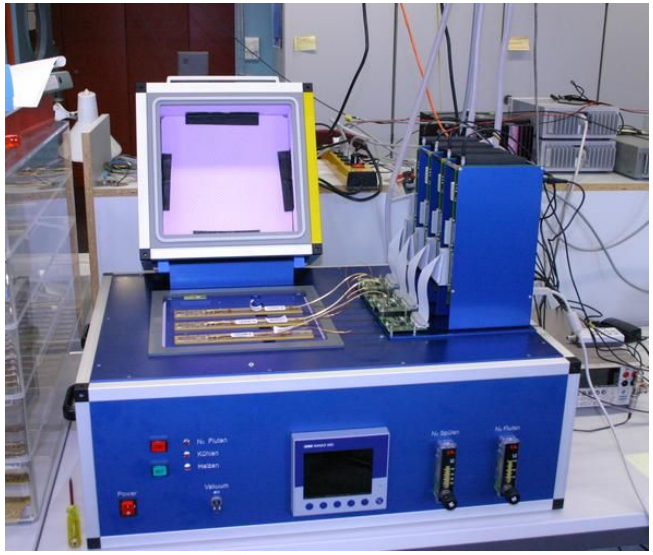
- Start-up adjustments
  - Analog current setting
  - Threshold and delay settings
  - Analog levels setting
- Functionality tests
  - Verification of pixel readout
  - Check bump bonding quality
  - Functionality of 4 trim bits
- Performance tests
  - Pixel noise measurements
  - Si sensor IV curves
- Calibrations
  - Find separation between address levels
  - Calibration of pulse height
  - Threshold unification (trimming)
  - Internal signal calibration (with X-rays)

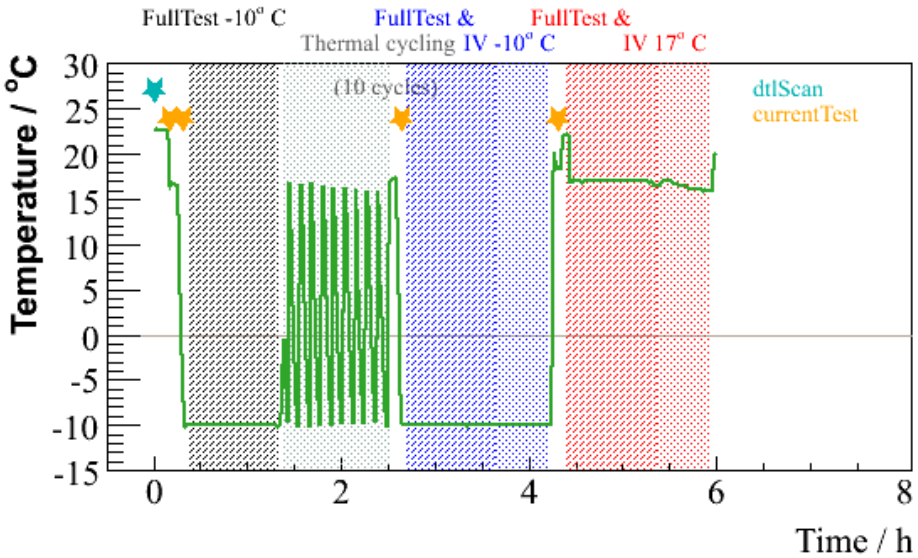




Testing set up and procedure

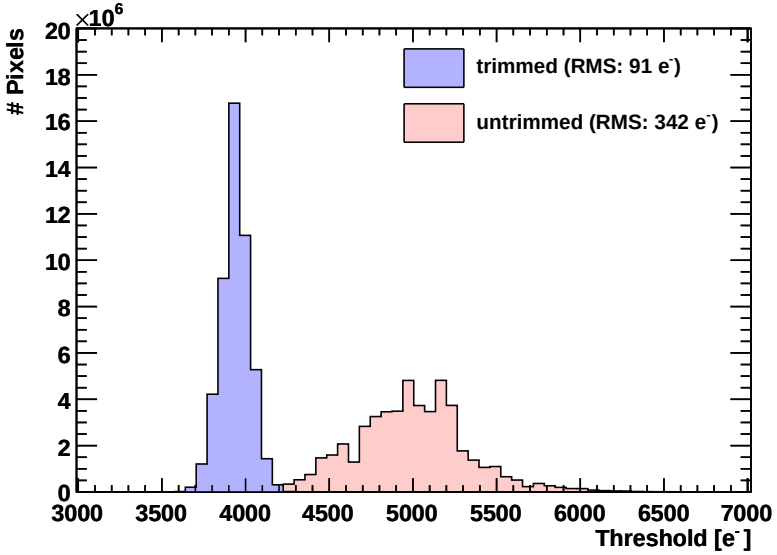
- Challenges
  - Huge number of channels: $5 \div 6\text{x}10^7$
  - Multy-dimensional parameter space: 29 DACs/ROC
  - Temperature dependence: tests done at -10°C and +17°C
- Test set up
  - Programmable cooling box
  - 4 modules at a time
  - Castom built test-boards with FPGA
- Procedure
  - Start-up adjustments
  - Full Test at -10°C
  - 10 thermal cycles
  - Full Tests and IV at -10°C and +17°C





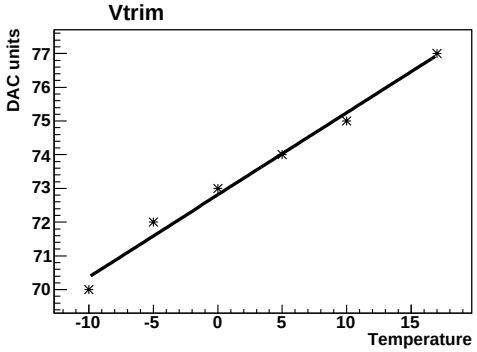
Example test: Trimming

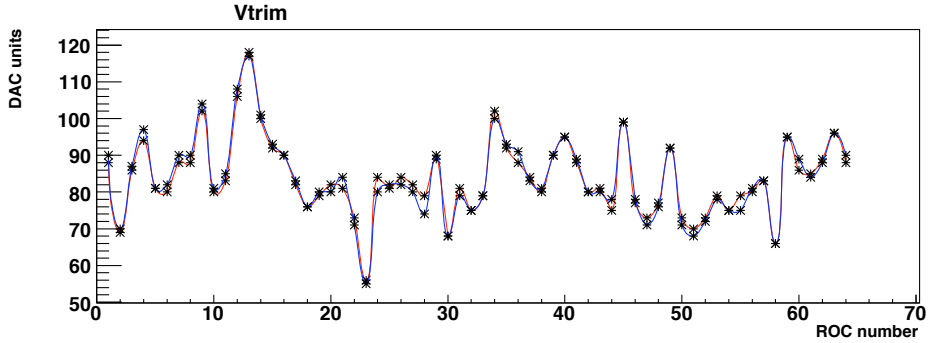
- The goal of trimming is threshold unification of ALL pixels
- Threshold = *VthrComp* - *Vtrim* x *Trimbits*
  - *VthrComp* and *Vtrim* are set per ROC
  - *Trimbits* (range: 0÷15) are set per pixel
  - Target Threshold is defined in terms of *Vcal* ('ionization charge')
- Trimming in the lab:
  - For fixed *Vcal* take *VthrComp* map
  - Set highest threshold and take *Vcal* map
  - Take pixel with highest *Vcal* and find *Vtrim* to set it to target threshold (all *Trimbits* enabled)
  - Determine *Trimbits* for other pixels to set them to target threshold

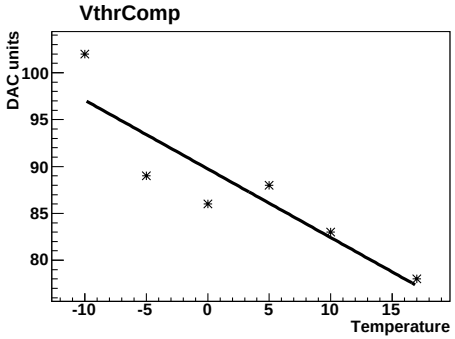


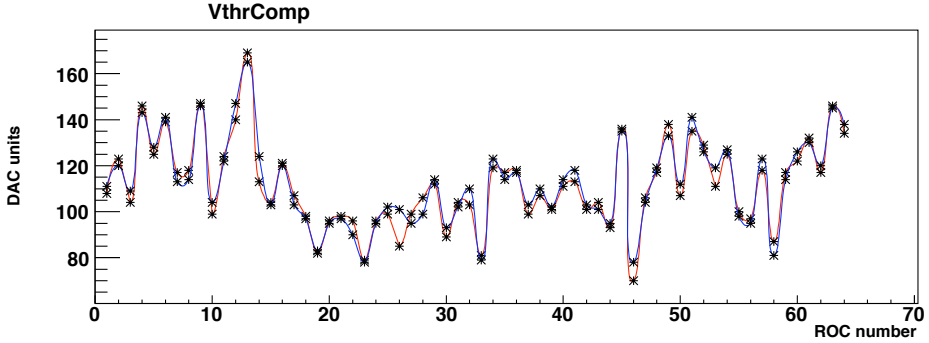
Trimming: parametrization

- Trimming is iterative procedure $\Rightarrow$ can't be done in situ
- Trim bit values do not depend on target Threshold, T and irradiation dose
- *VthrComp* and *Vtrim* depend on target Threshold and T:
  - $V_{ThrComp}(V_{Cal}) = V_{ThrComp}(60) - 0.65 \times (V_{Cal} - 60)$
  - $V_{Trim}(V_{Cal}) = V_{Trim}(60) - 0.45 \times (V_{Cal} - 60)$



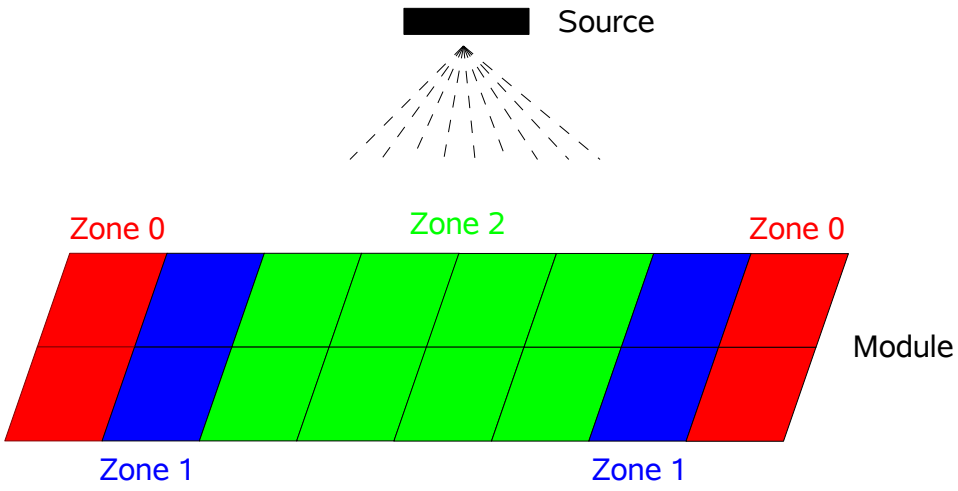






X-ray test

- Twofold purpose:
  - test module response to the injected charge into Si sensor
  - calibrate internal signal used for the trimming (setting threshold)
- X-ray source:
  - Primary source: Americium-241
  - Targets: Mo(4844 e^-), Ag(6139$^-$), Ba (8906 e^-)
  - Random trigger, stretched bunch-crossing
- Test setup:

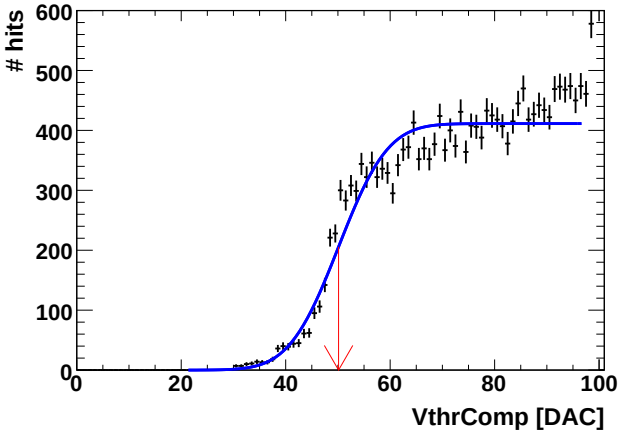


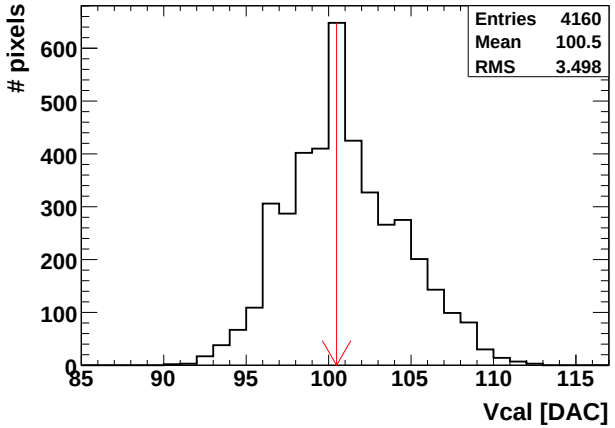
Calibration procedure

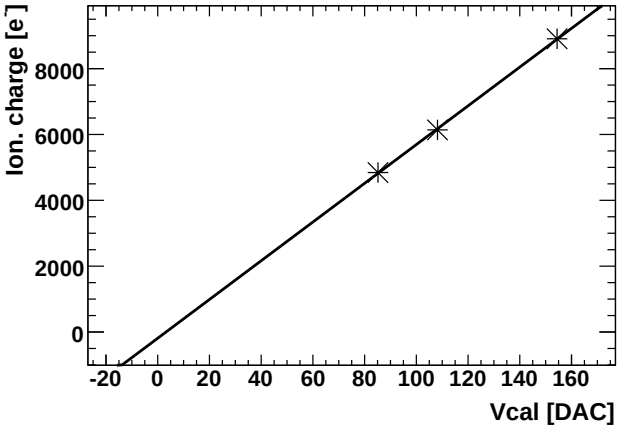
- Trim ROC
- Measure # of hits vs threshold
- Fit with error function
- Find threshold (50%)

- Set VthrComp to found value
- Measure Vcal value for all pixels
- Take mean Vcal

- Combine Vcal from different sources
- Fit with a straight line
- Determine slope and offset

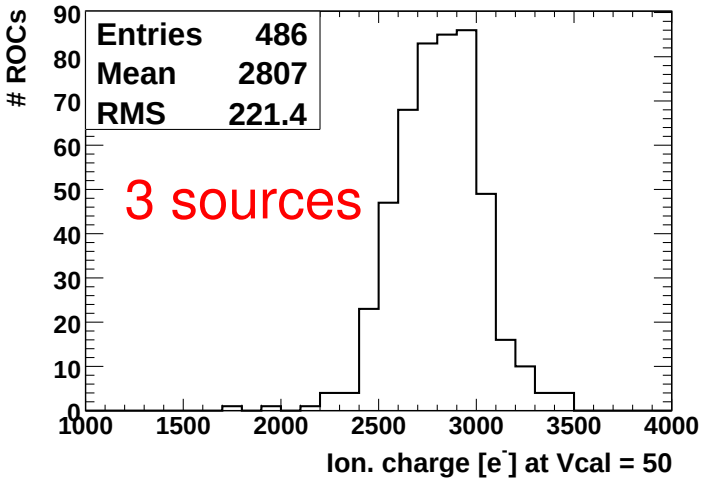


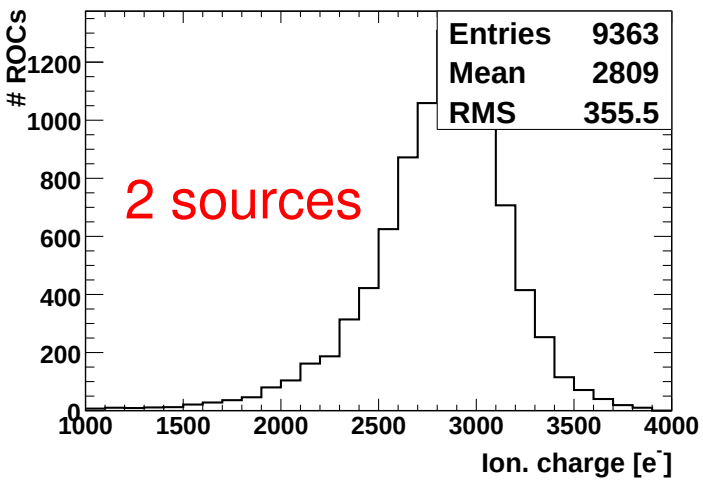




Calibration: conclusions

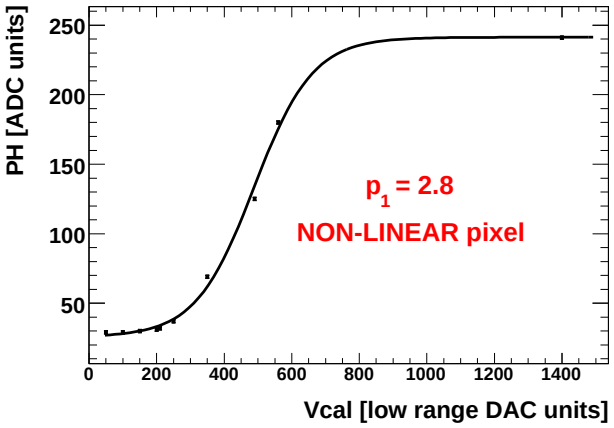
- On average 1 Vcal DAC corresponds to 66 e^-
- The mean offset at Vcal=0 is around -420 e^-
- Trimming with Vcal=50 corresponds to threshold of 2800 e^-
- For calibration use
  - if available, results for individual ROC from 3 sources
  - otherwise, mean from 2 sources average over module

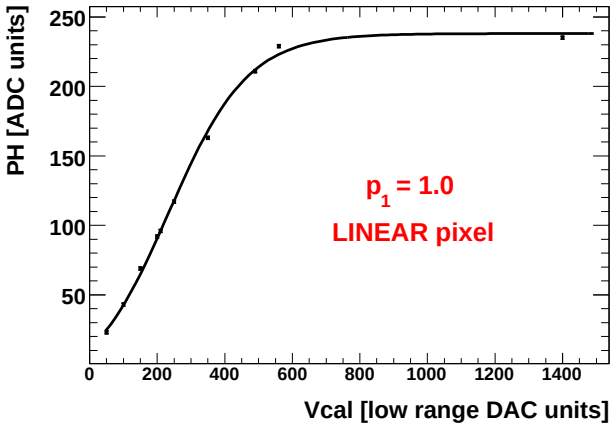


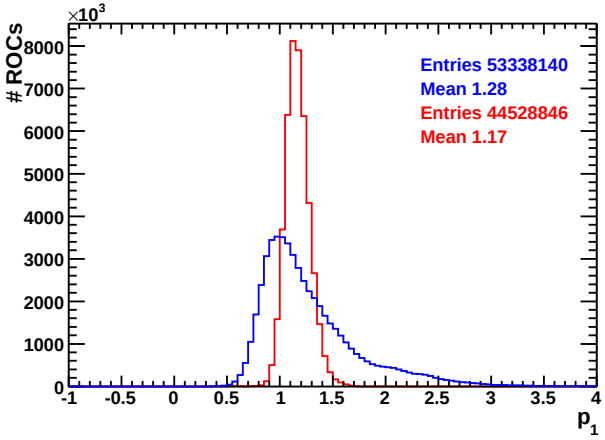


DAC optimization

- Several DACs have been optimized to set:
  - Analog and digital currents
  - Digital levels of TBM and ROC (Ultra Black)
  - Thresholds and delays
  - Pulse height ADC range and linearity
- Example: Pulse height linearity
  - Fit function: $y = p_3 + p_2 \cdot tanh(p_0 \cdot x - p_1)$



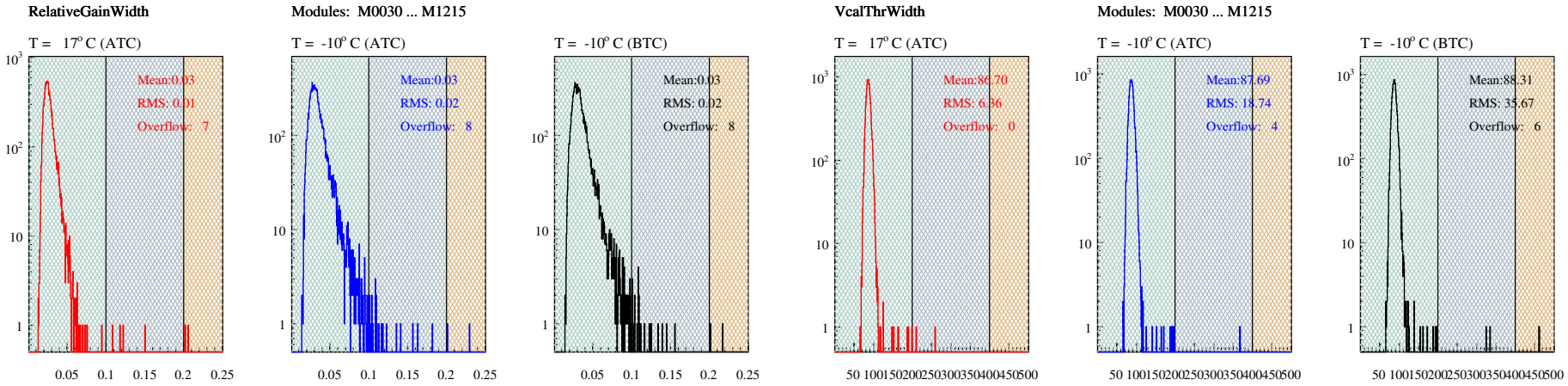




Grading

	Pixel	Mask	Noise	Gain	Pedestal	Thr.	I^{meas}_{+17}(150V)	I^{calc}_{-10}(150V)
A	$\leq$ 1%	0	$\leq$ 500e^-	$\leq$ 10%	<2.5ke^-	<200e^-	<2μA	<3μA
B	$\leq$ 4%	0	$\leq$ 1000e^-	$\leq$ 20%	<5.0ke^-	<400e^-	<10 μA	<15μA
C	$>$ 4%	$\geq$ 1%	$\geq$ 1000e^-	$>$ 20%	>5.0ke^-	>400e^-	>10μA	>15μA

- Pixel defects/chip
- Mask: permanent readout
- Noise in e^-
- Relative Gain width
- Pedestal spread in e^-
- Vcal Threshold Width in e^-
- I^{meas}_{+17}(150V): measured leakage current at $+17°$
- I^{calc}_{-10}(150V): recalculated leakage current at $-10°$



Production summary

948 modules tested (827 full/ 121 half)

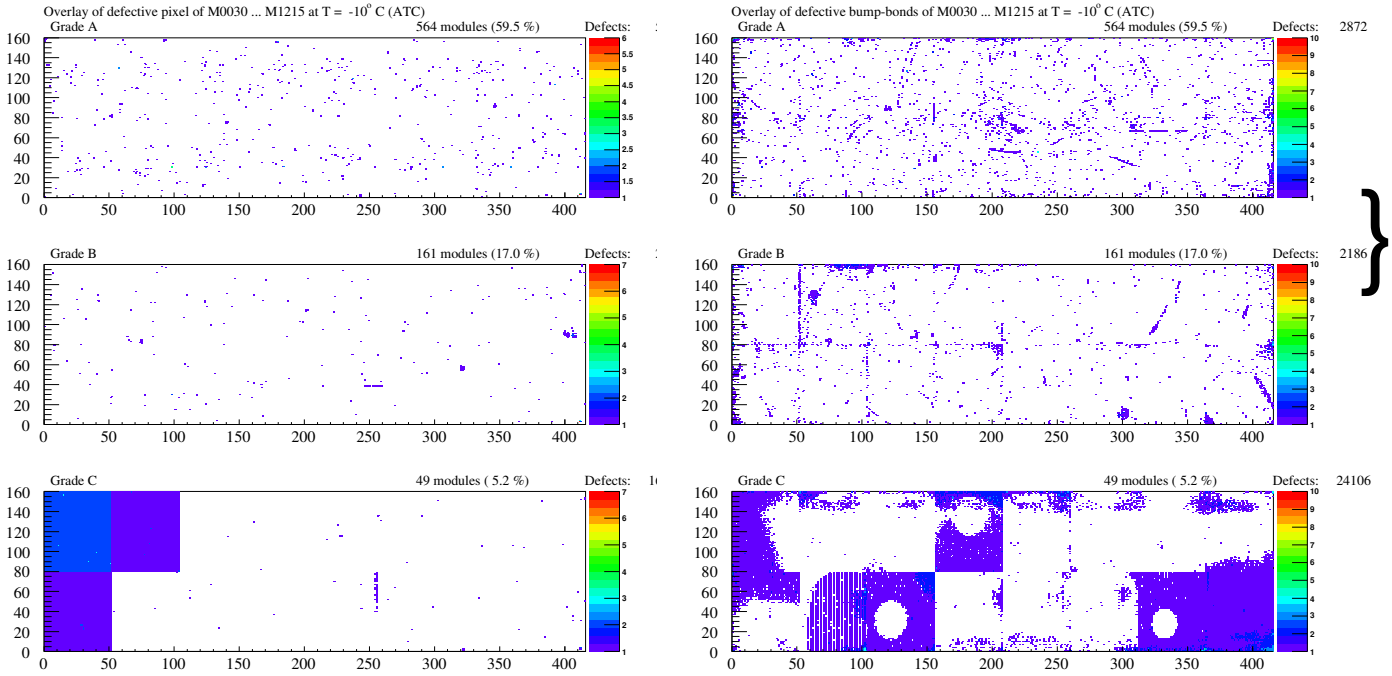
- 565/161 graded as A/B → 88% ‖ 87/23 → 91%
- 101 graded as C → 12% ‖ 11 → 9%

Overlay of modules tested at T = -10° C (ATC)

Final Grade A (564 modules)

Final Grade B (161 modules)

Final Grade C (49 modules)



} 48.3M pixels

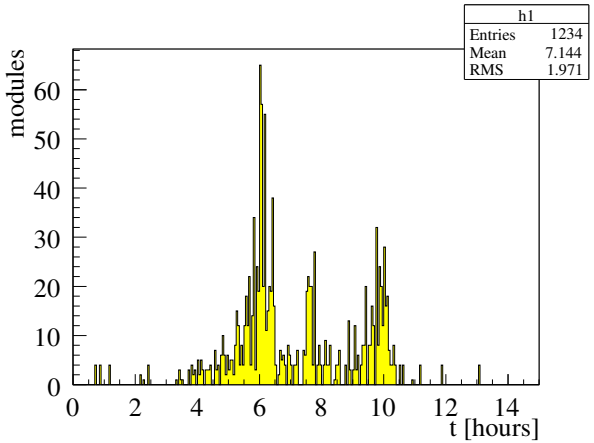
3.3M pixels

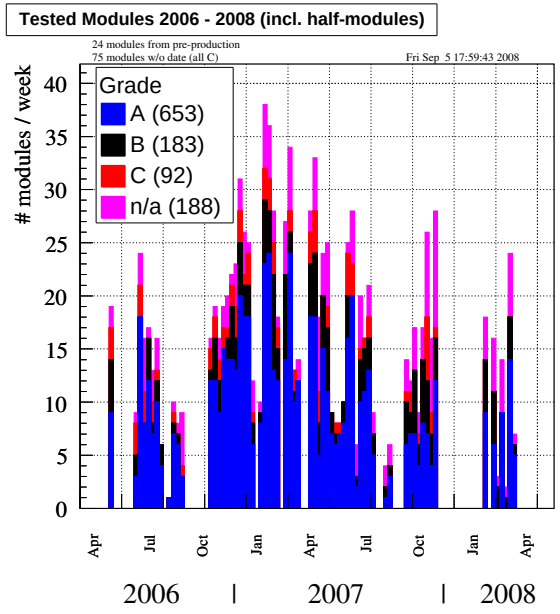
Dead pixels

Dead bumps

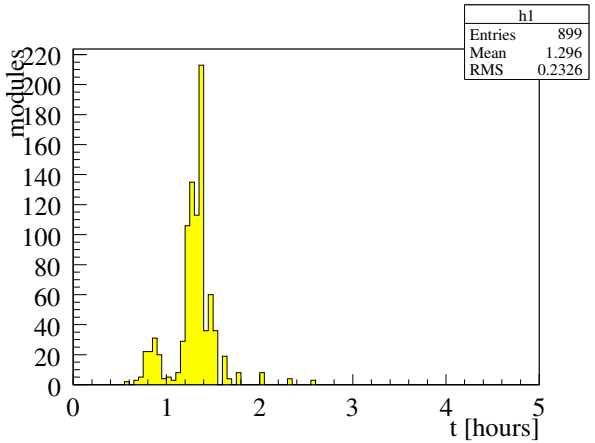
Production in time

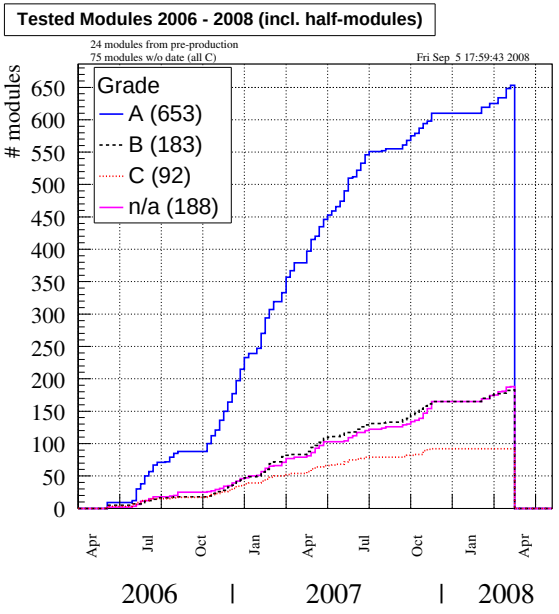
Full tests



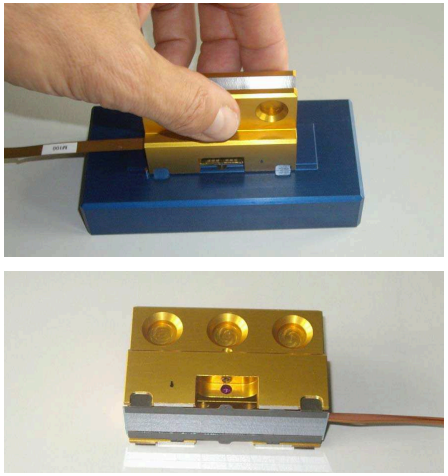


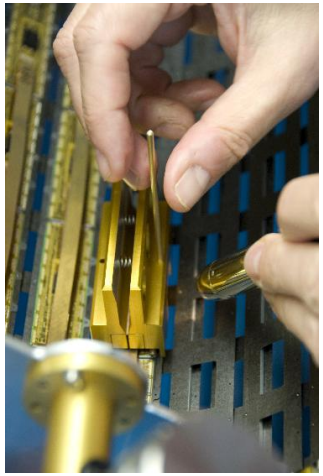
Short tests (w/o x-ray)

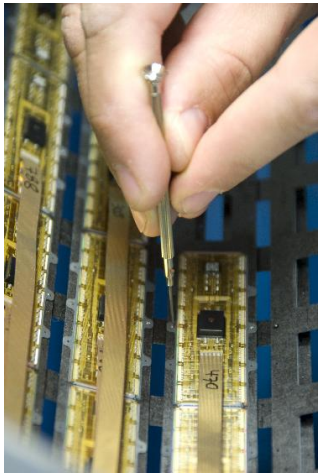


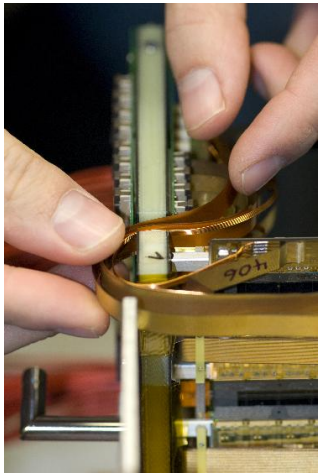


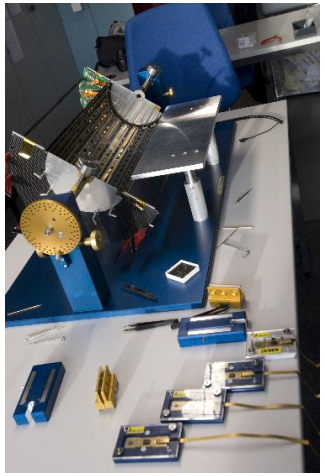
Module mounting and survey







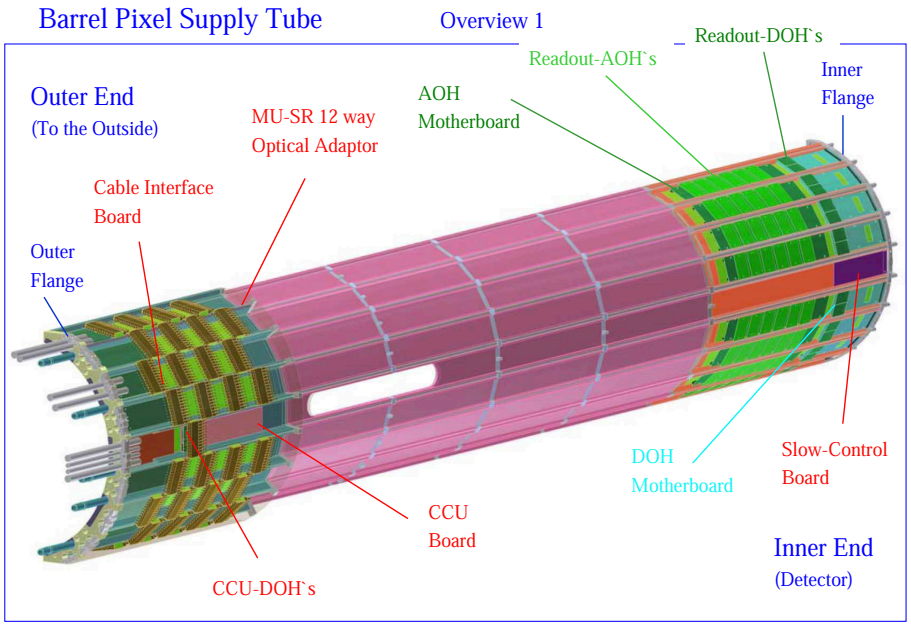




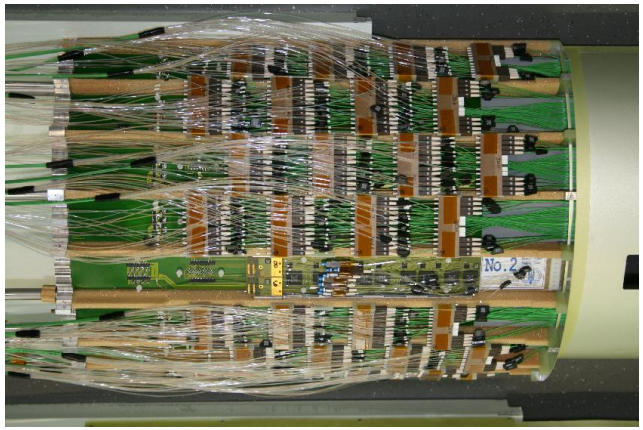
- 768 modules to mount
- Mounting tool is crucial
- Up to 60 modules / day
- Only 3 modules destroyed
- About 10 modules repaired:
  - broken wire bonds
  - bad connector

- Difficult object to survey
- Module position/ladder in 2D
- Pictures of 2 facing modules
- Optical pattern recognition SW
- Mean errors (z-dependent):
  - $r - \phi$=9.5 μm, z=4.5 μm
  - γ=240μrad

Supply tube

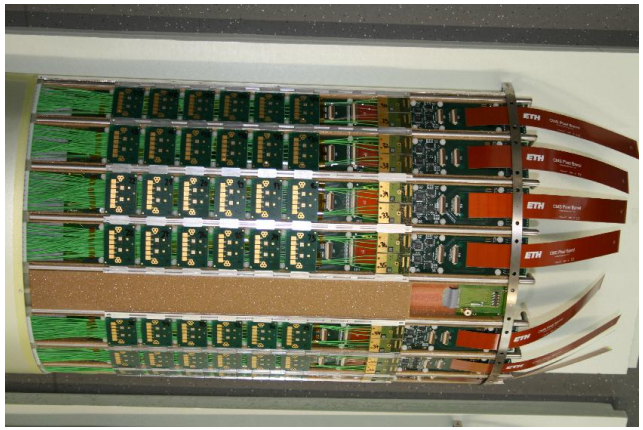


- Complex design and production:
  radial shell thickness 1-2cm
- Supply tube contains:
  - AOHs for 1152 optical r/o fibers
  - optical links for FE programming
  - optical links for detector control
  - boards for power distribution
  - temperature and humidity sensors
- Production time about 10 weeks

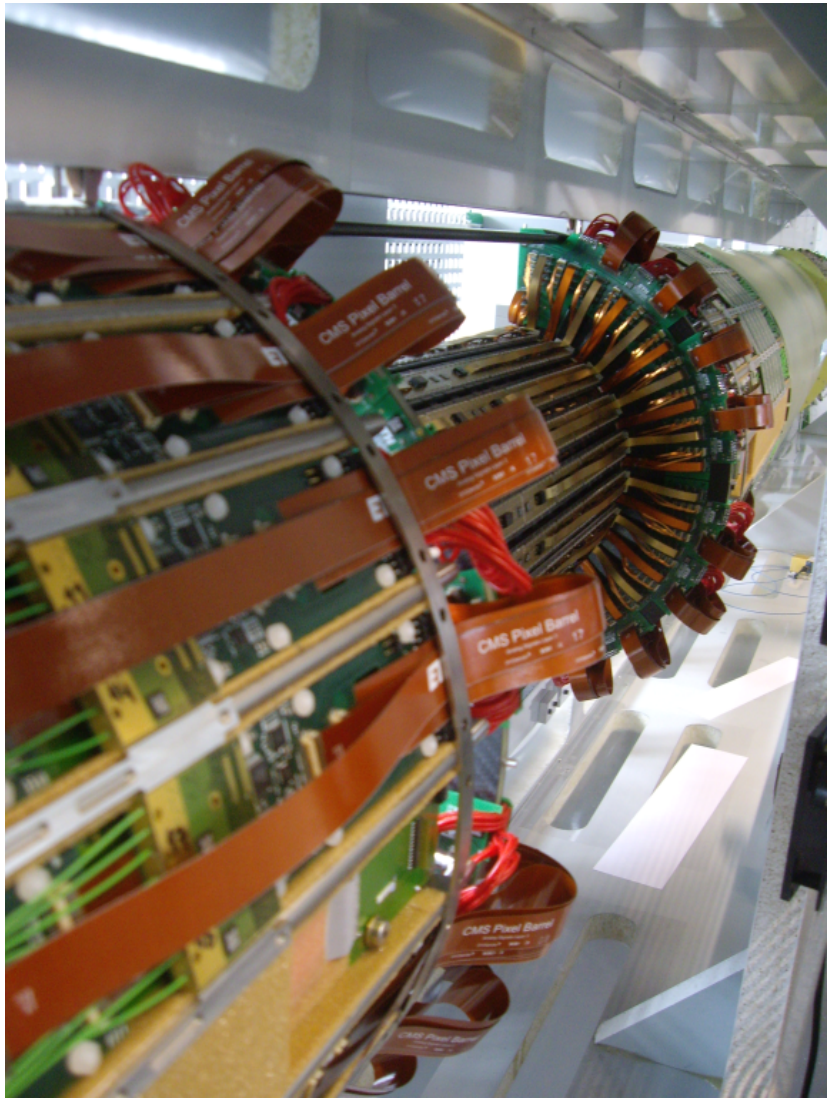


Outer End

Inner End



Tests before installation



- Mechanical tests:
  - left/right clearance: 1mm
  - real detector and mock-up rail system
- Transport test
  - PSI-CERN-PSI
  - 'commissioning system' + accelerometer
- Insertion test:
  - 'commissioning system'
  - true mechanical structure
  - prototype half supply tube
  - one sector (1/32) equipped with modules

What did we learn?

- Team of 10-15 people: sensor, chip, mechanics, cooling, cabling, production, testing, performance, operation, calibration
- Construction time about 2 years, with many more years ($\sim$10) of preliminary studies, design, tests
- Crucial for the speed of the construction:
  - automated procedures: bump-bonding, module tests
  - automated qualification after module tests
  - special tools for module assembling and mounting
- DB is a must component: no other way to keep track module test results and logistic