LAUREN TOMPKINS

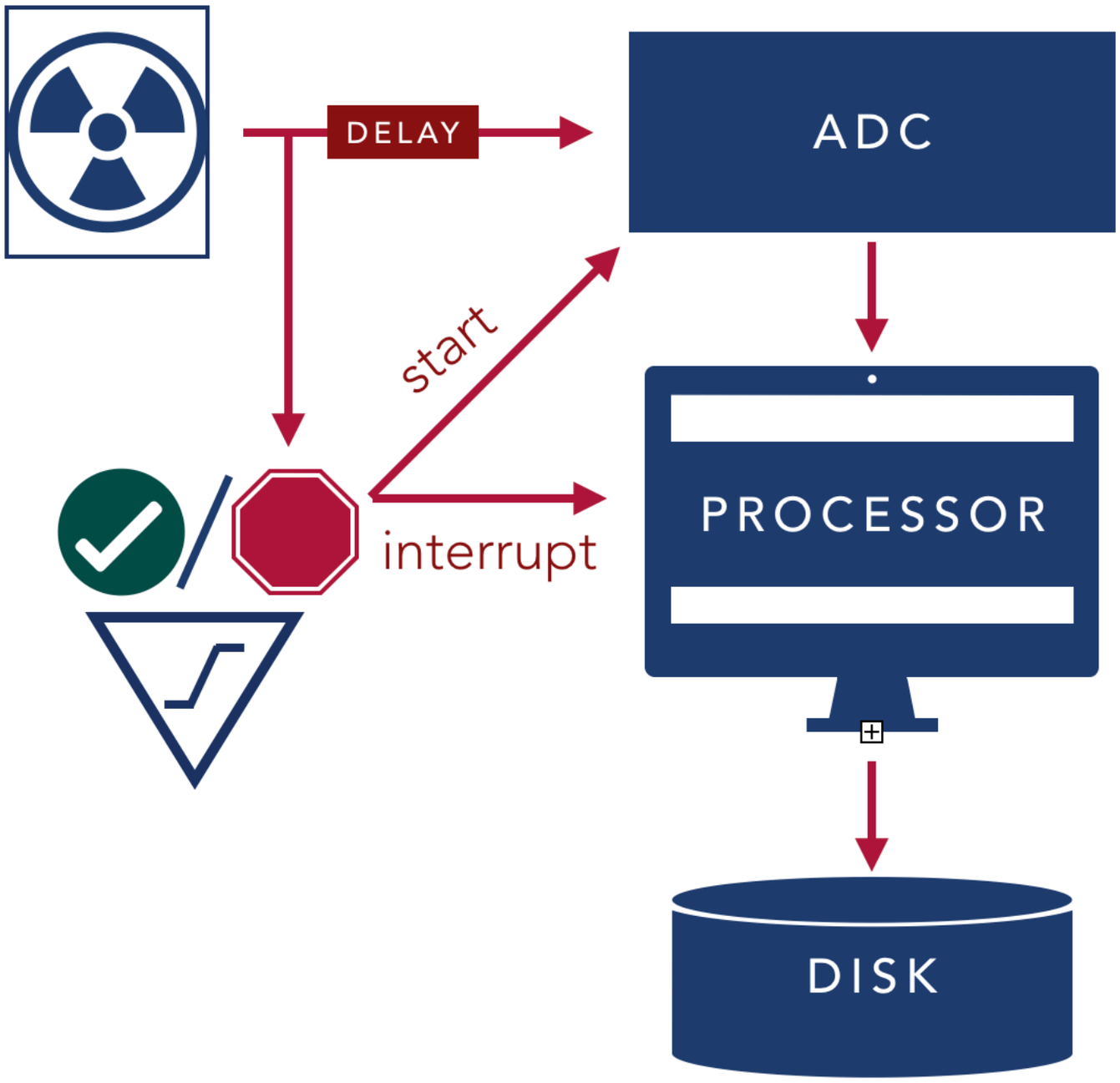
HCPSS 2018

TRIGGER AND DATA ACQUISITION

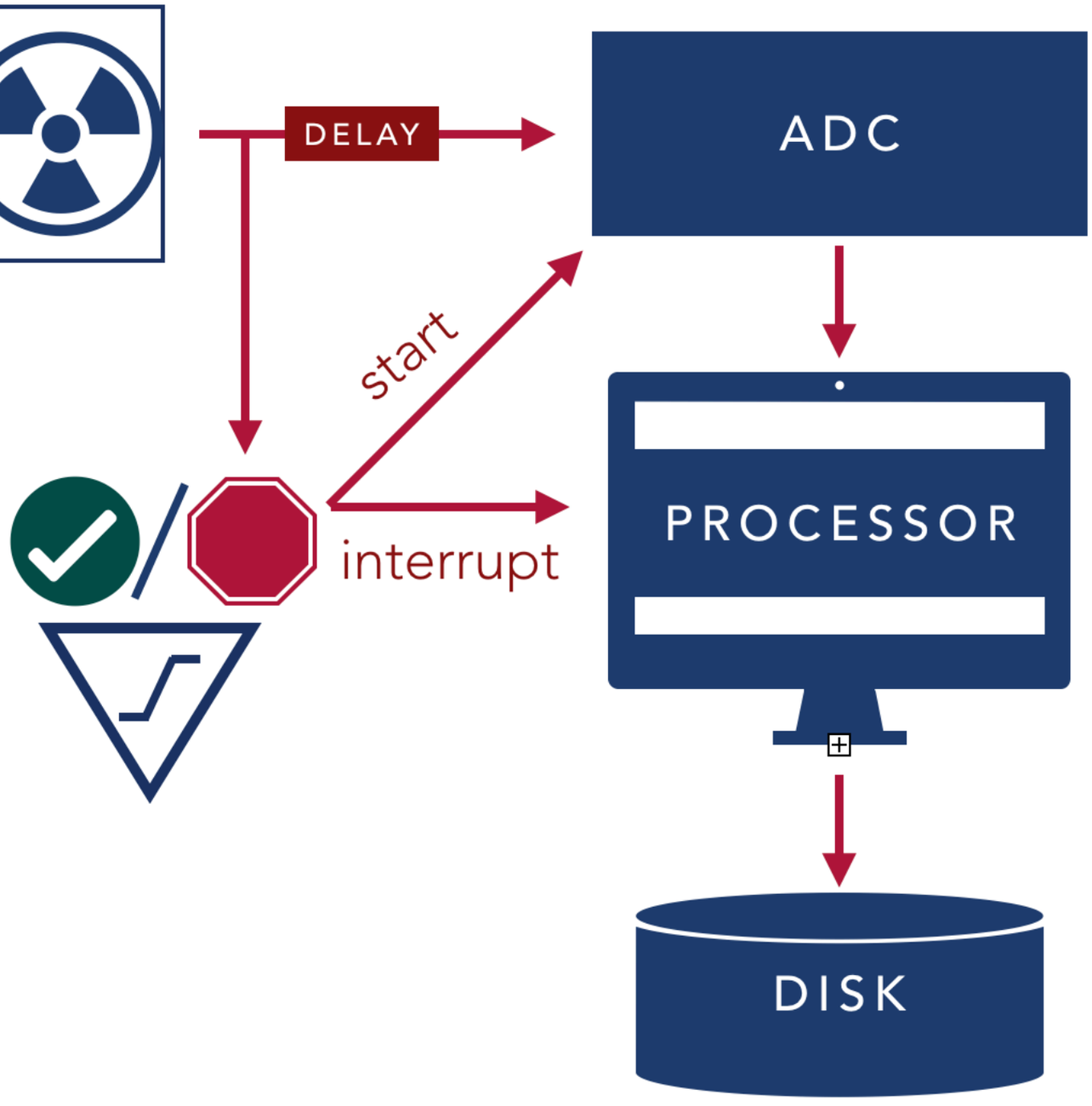
Stanford University

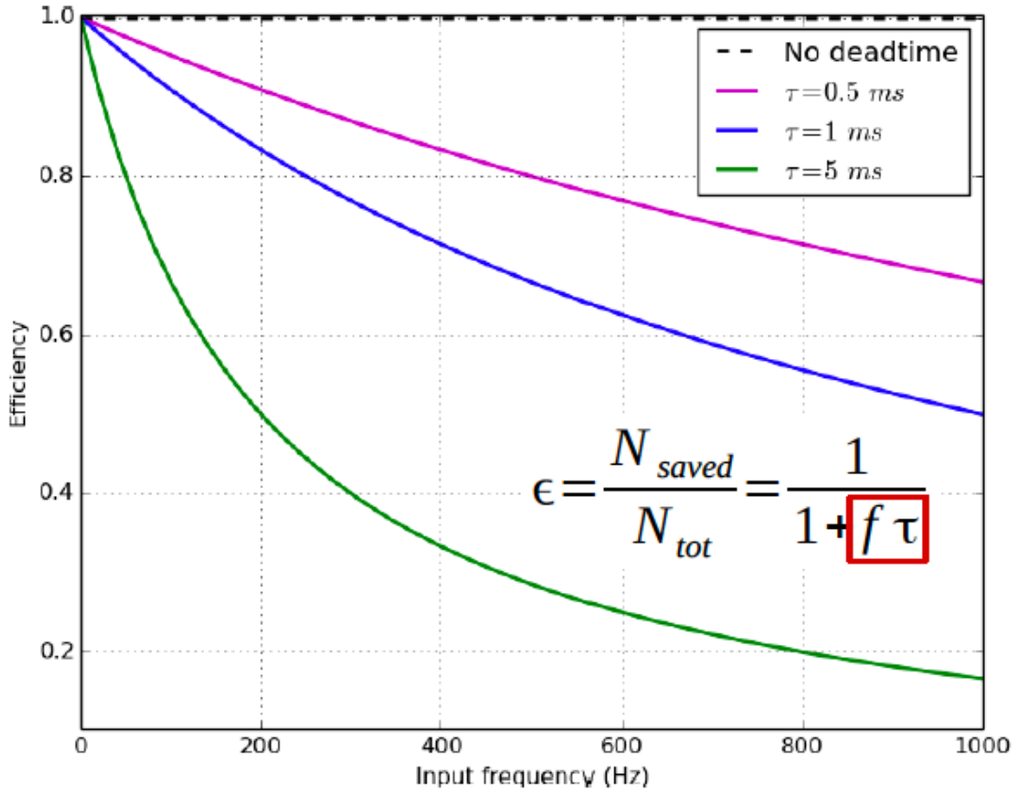
REMINDER FROM YESTERDAY

REMINDER FROM YESTERDAY

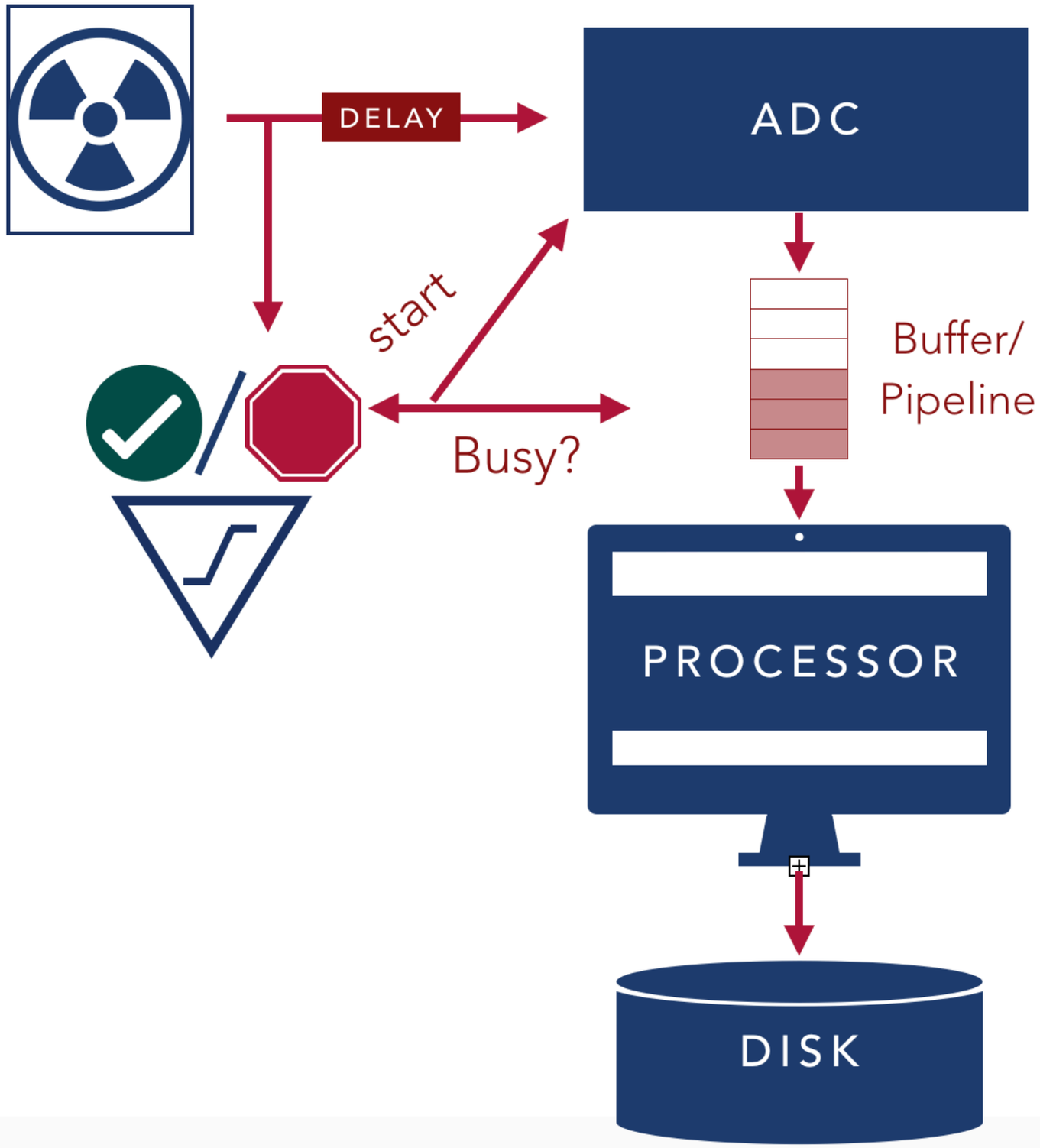


REMINDER FROM YESTERDAY

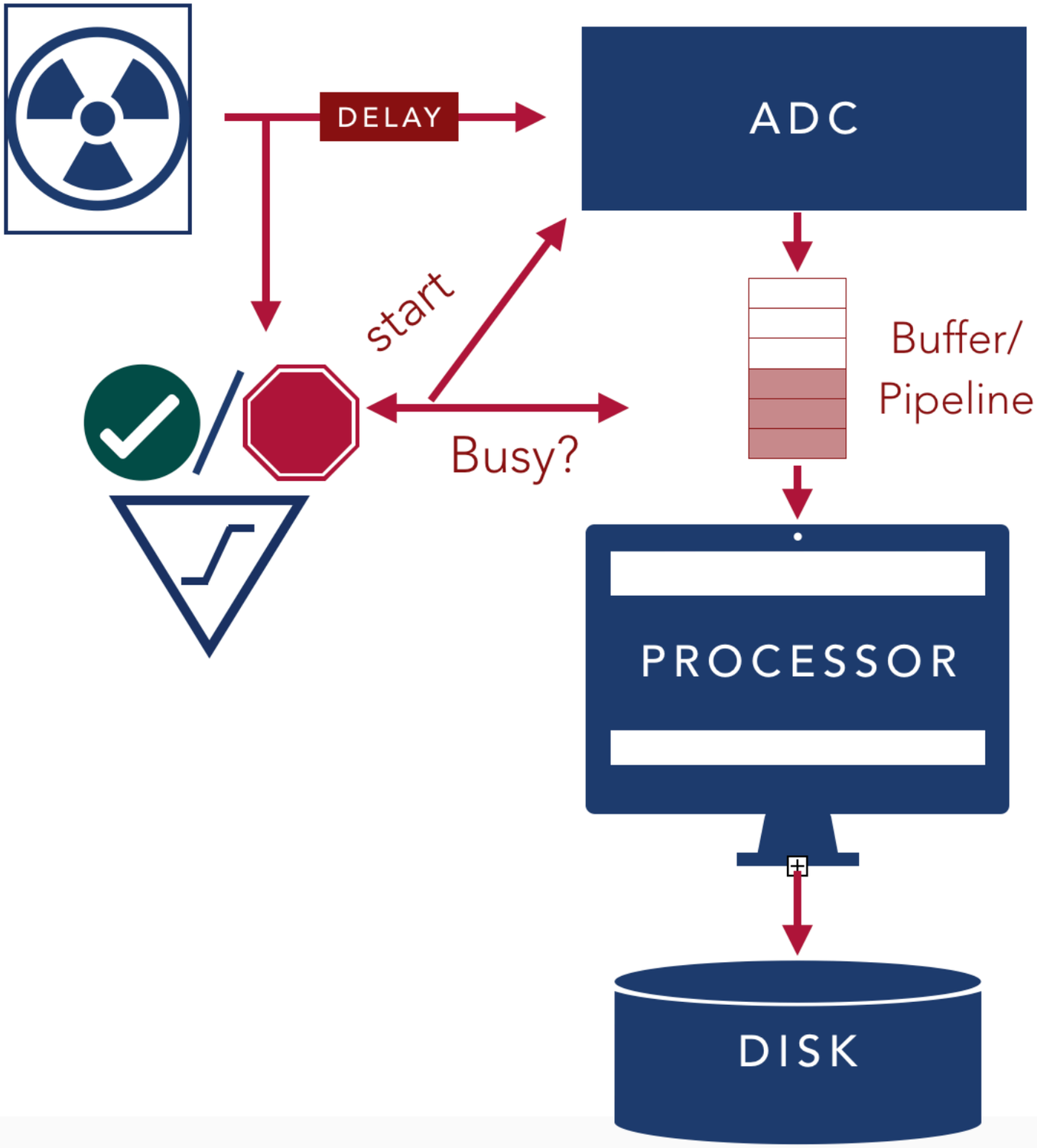


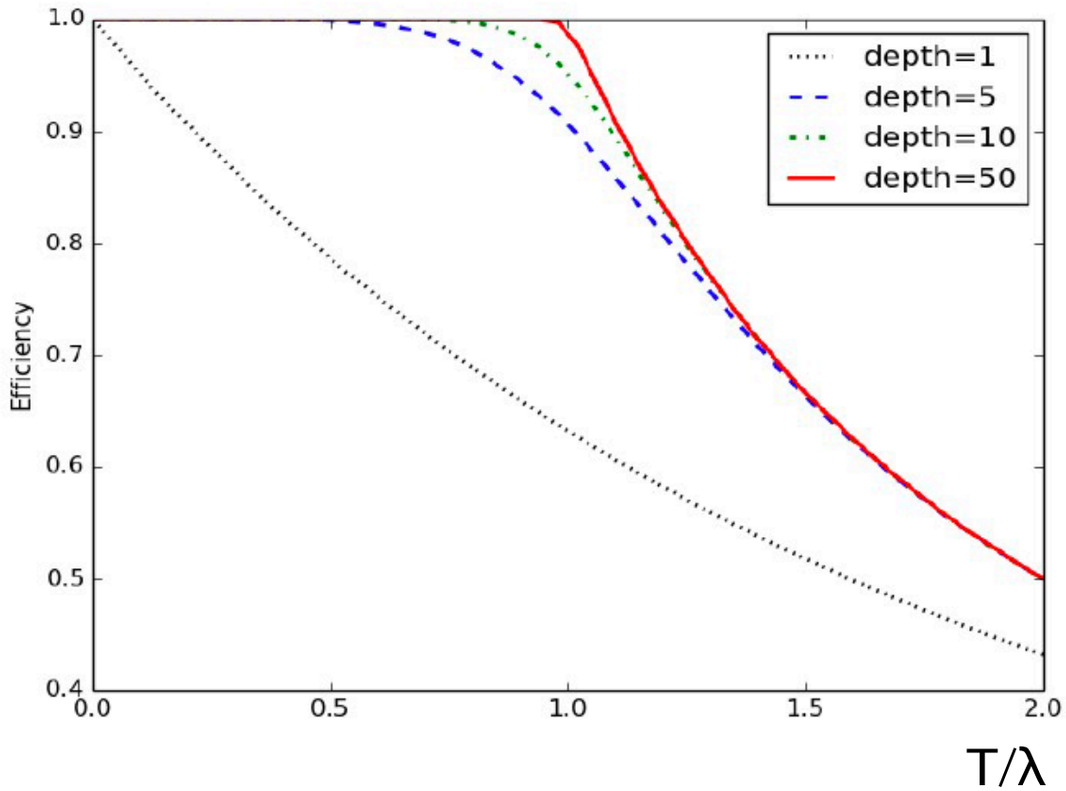


REMINDER FROM YESTERDAY

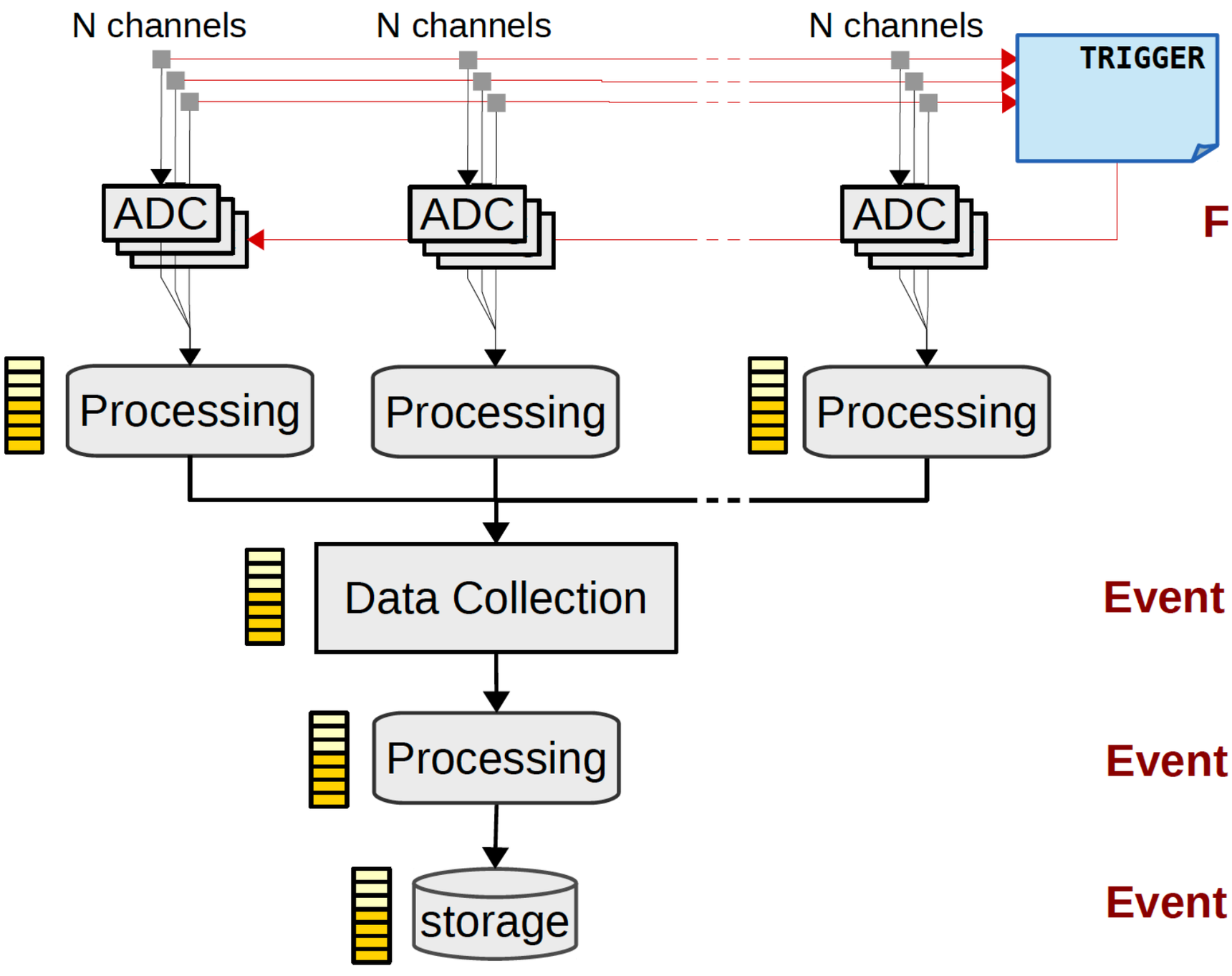


REMINDER FROM YESTERDAY





REMINDER FROM YESTERDAY



Front-End	data digitization data buffering
Readout	data extraction data formatting data buffering
Event Building	event assembly event buffering
Event Filtering	event rejection event buffering
Event Logging	file storage file buffering

THE REST OF THE LECTURES

- Overview of the current ATLAS & CMS TDAQ architecture
  - ATLAS Level 1 Trigger & DAQ
  - CMS High Level Trigger & DAQ
- How triggers are constructed for the LHC environment
  - The art of menu building
  - Creative solutions to challenging conditions
- Looking forward to the upgrades
  - LHCb: The trigger-less future?
  - Contending with 200 simultaneous collisions

TDAQ: CMS & ATLAS STYLE

ATLAS RUN II TDAQ SYSTEM

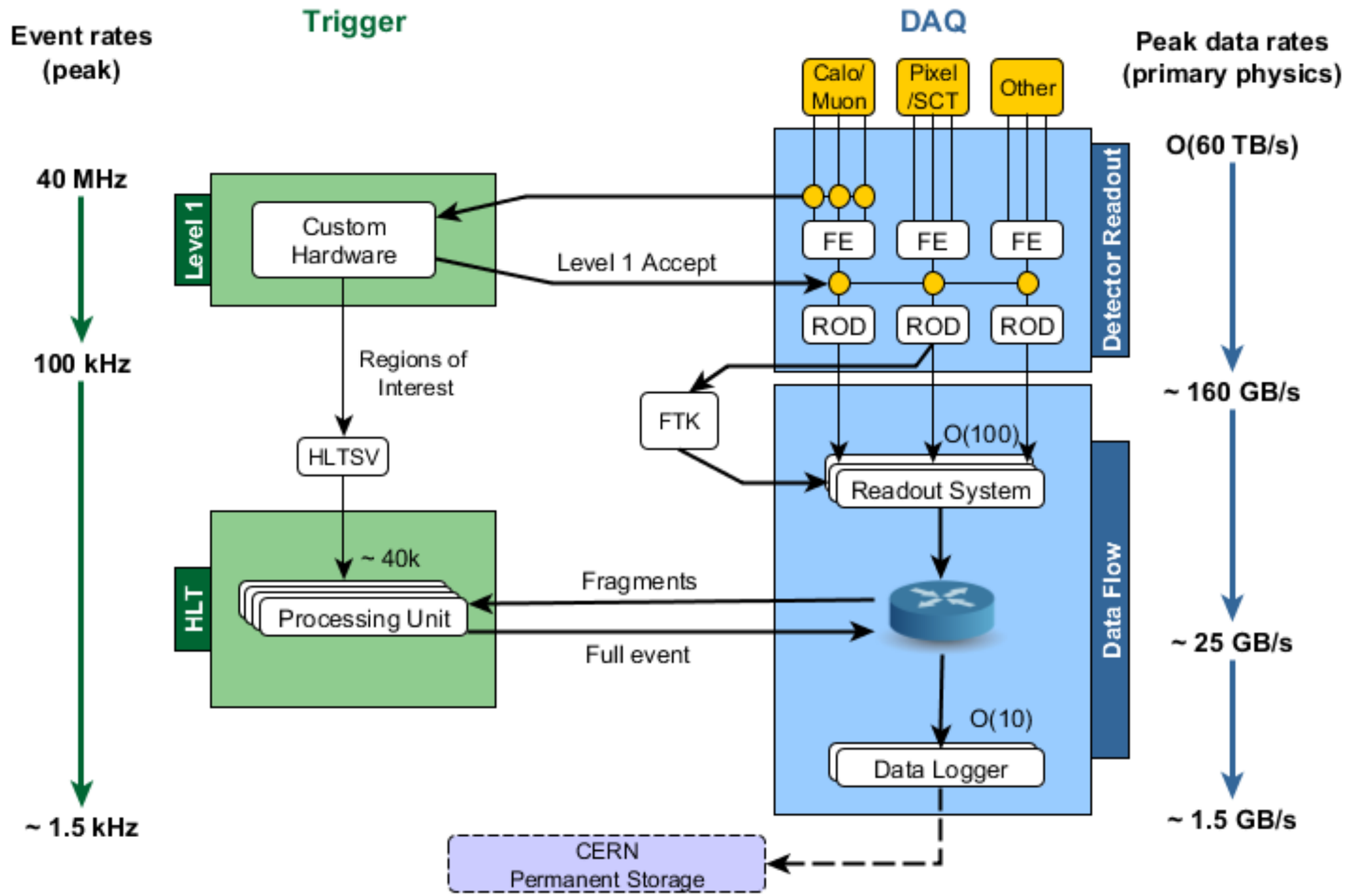


Fig. Ref

ATLAS RUN II TDAQ SYSTEM

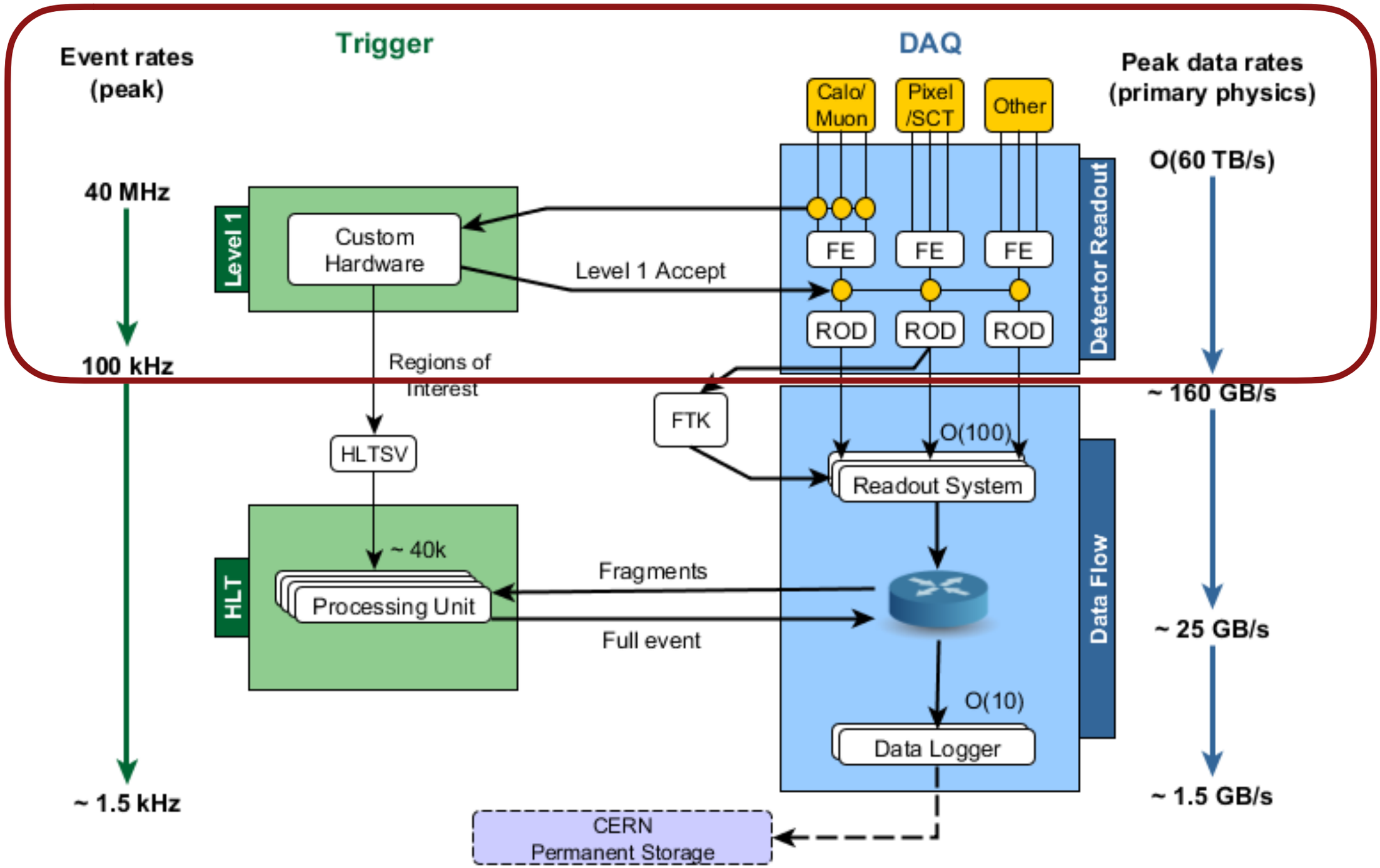


Fig. Ref

ATLAS RUN II TDAQ SYSTEM

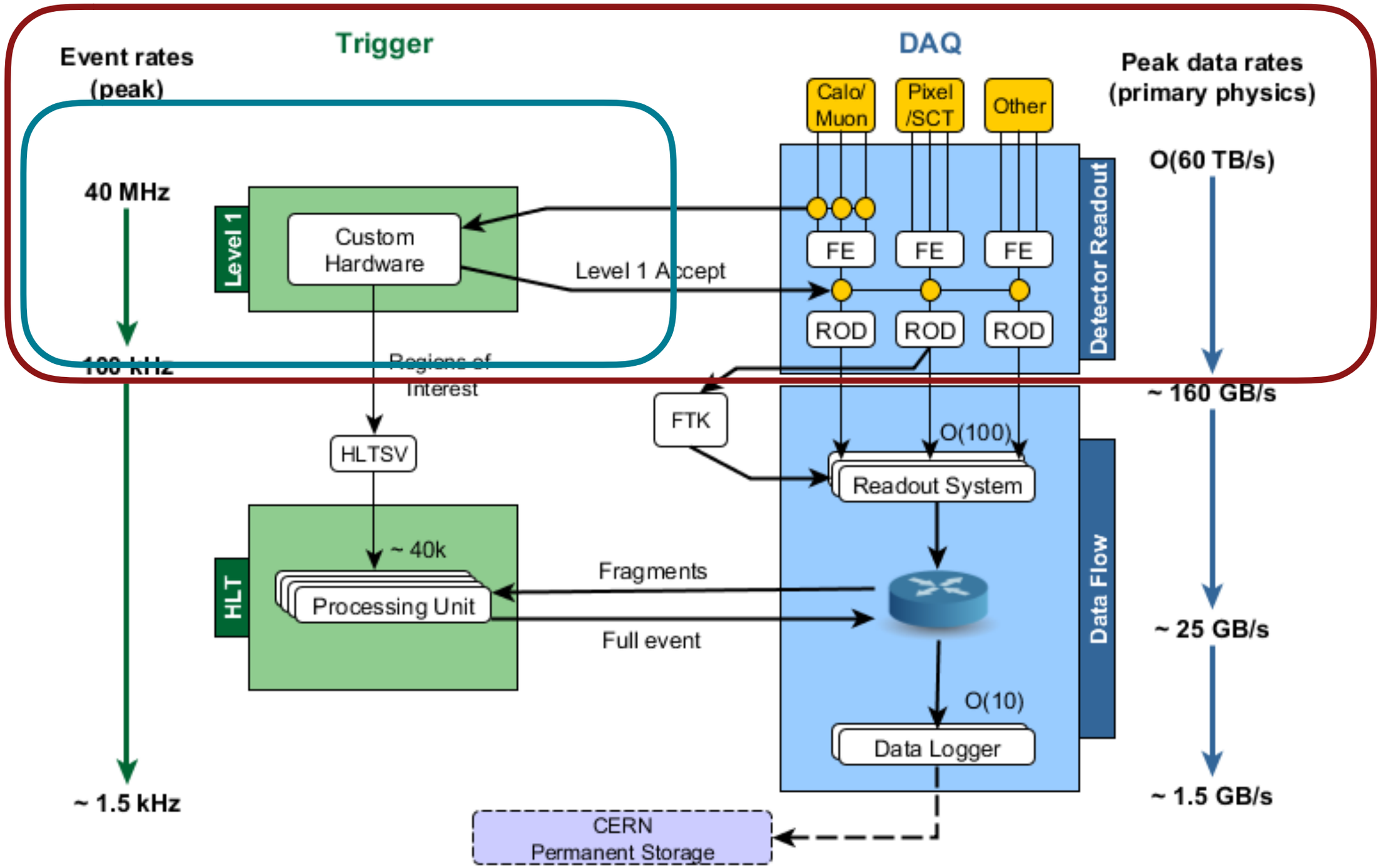
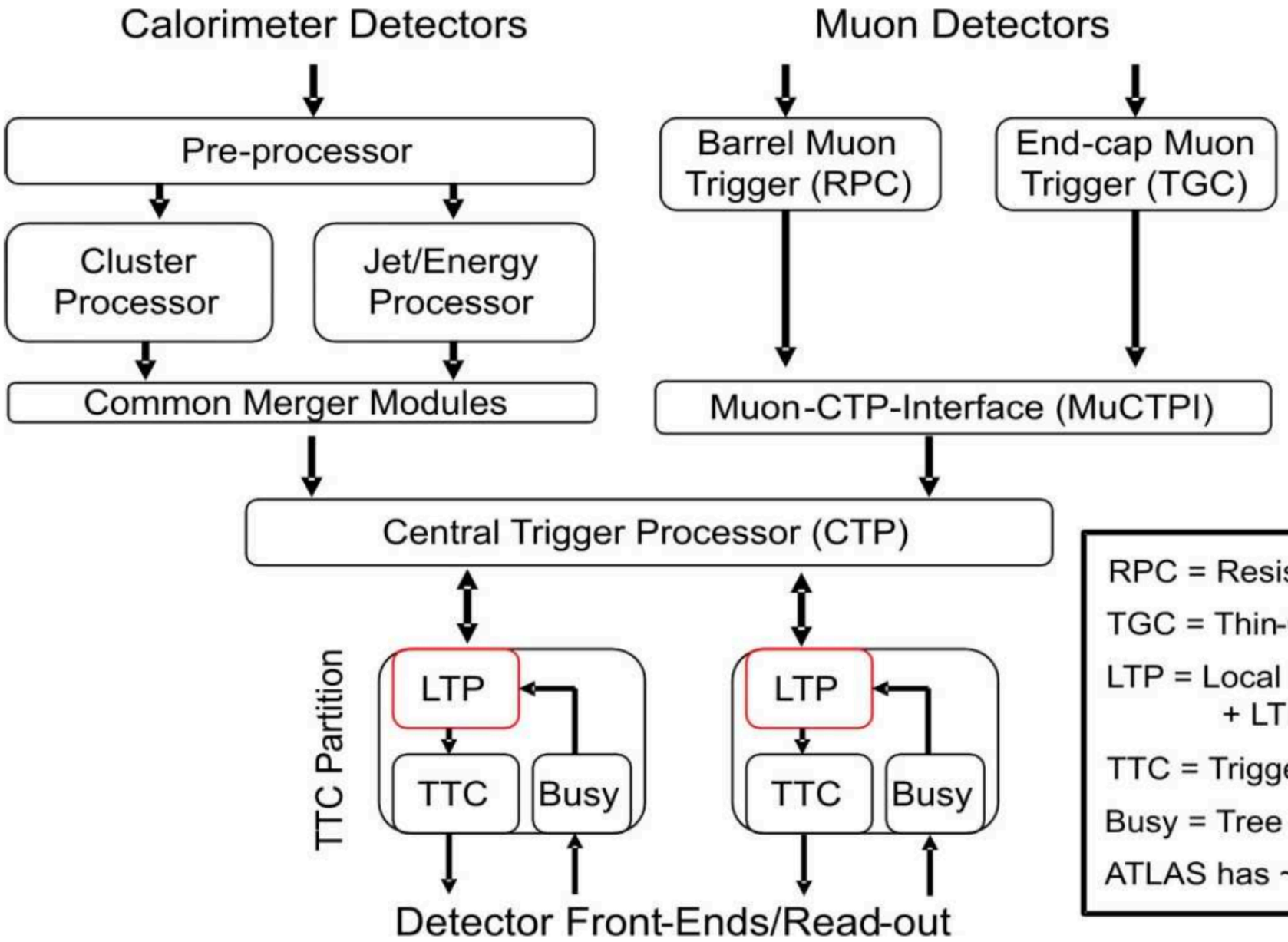


Fig. Ref

ATLAS LEVEL 1 TRIGGER SYSTEM



RPC = Resistive-Plate Chamber

TGC = Thin-Gap Plate Chamber

LTP = Local Trigger Processor + LTP interface

TTC = Trigger Timing & Control

Busy = Tree of ROD_Busy modules

ATLAS has ~40 TTC partitions

Fig. Ref

ATLAS LEVEL 1 TRIGGER SYSTEM

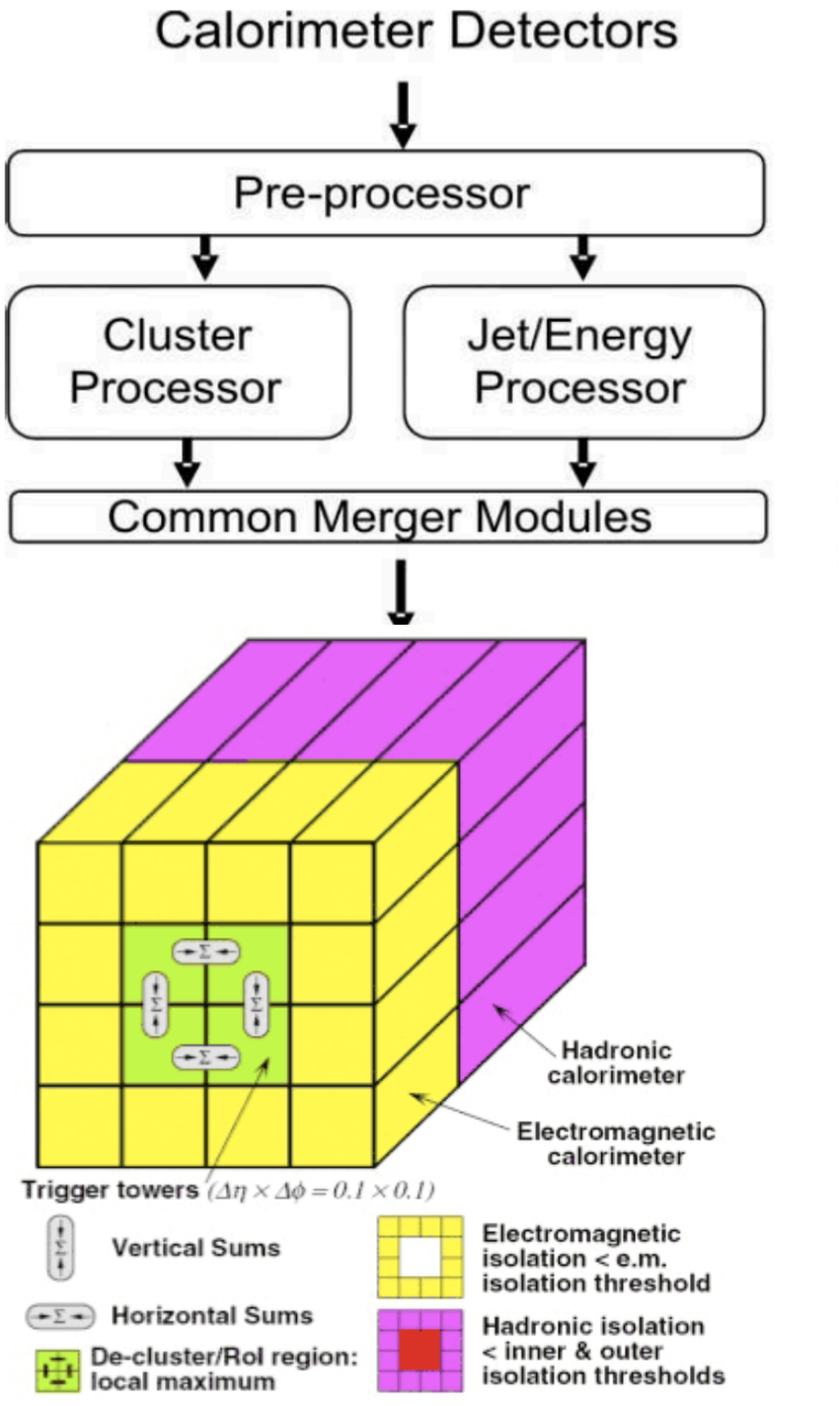
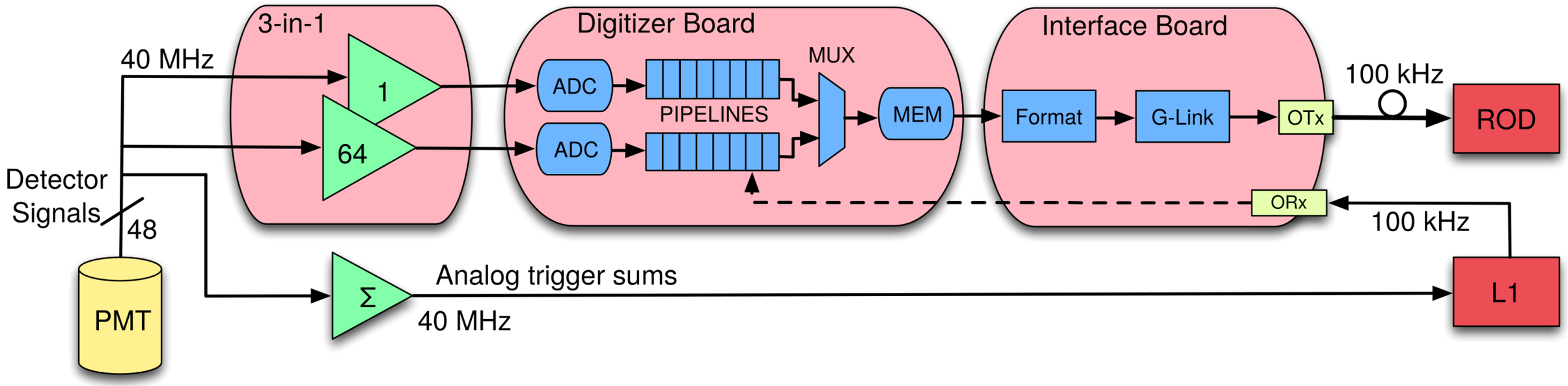


Fig. Ref

ATLAS LEVEL 1 TRIGGER SYSTEM



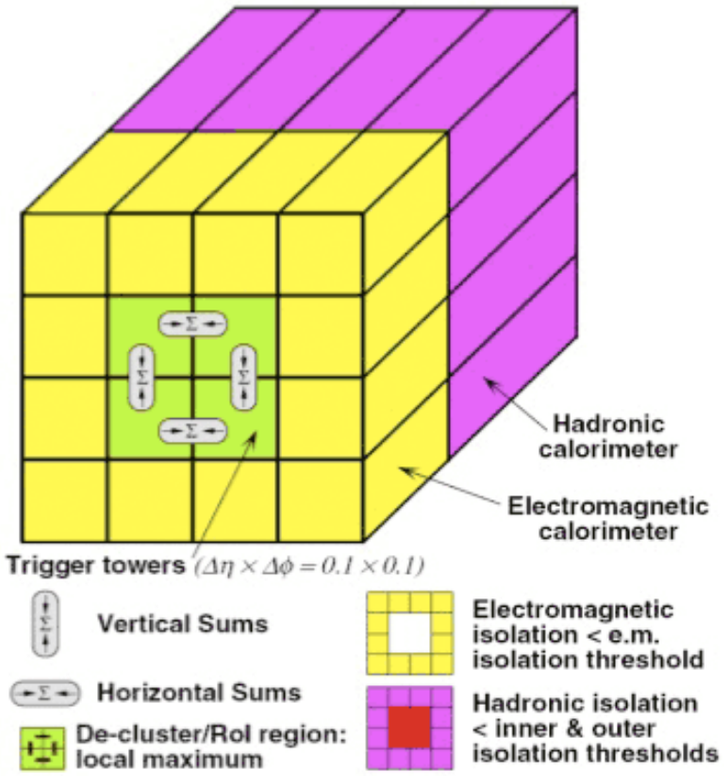


Fig. Ref

TOPOLOGICAL TRIGGERS

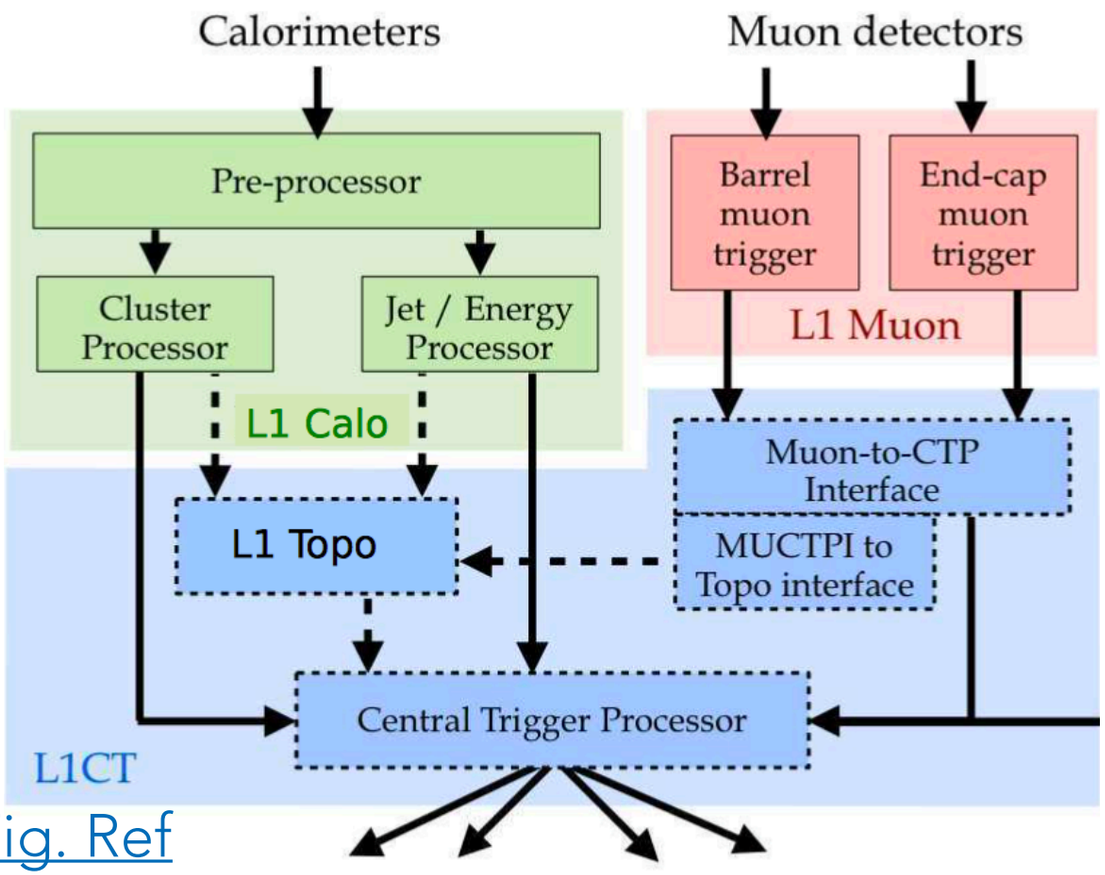
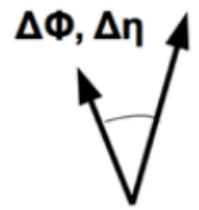
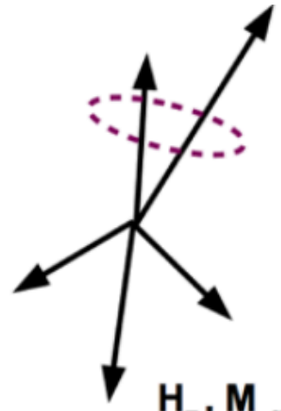


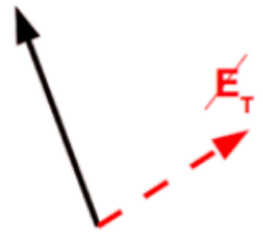
Fig. Ref



Isolation, overlap removal, b-tagging...



Fat jets



Transverse Mass, ΔΦ(jet, E_T)

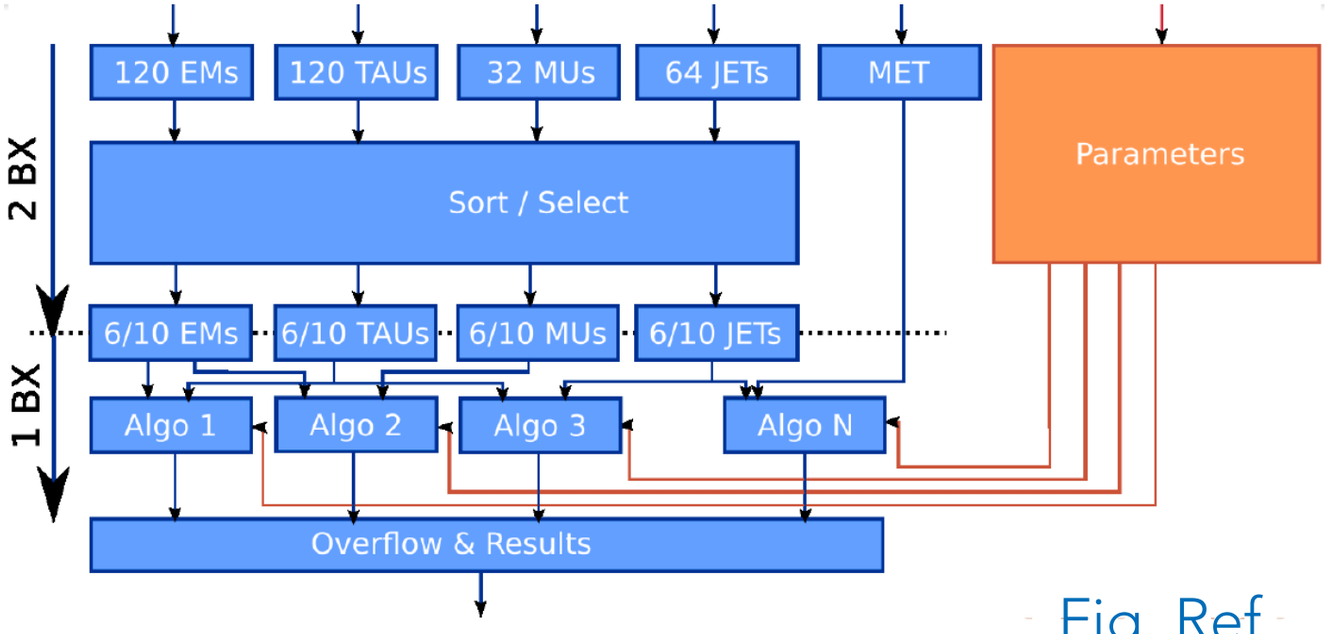
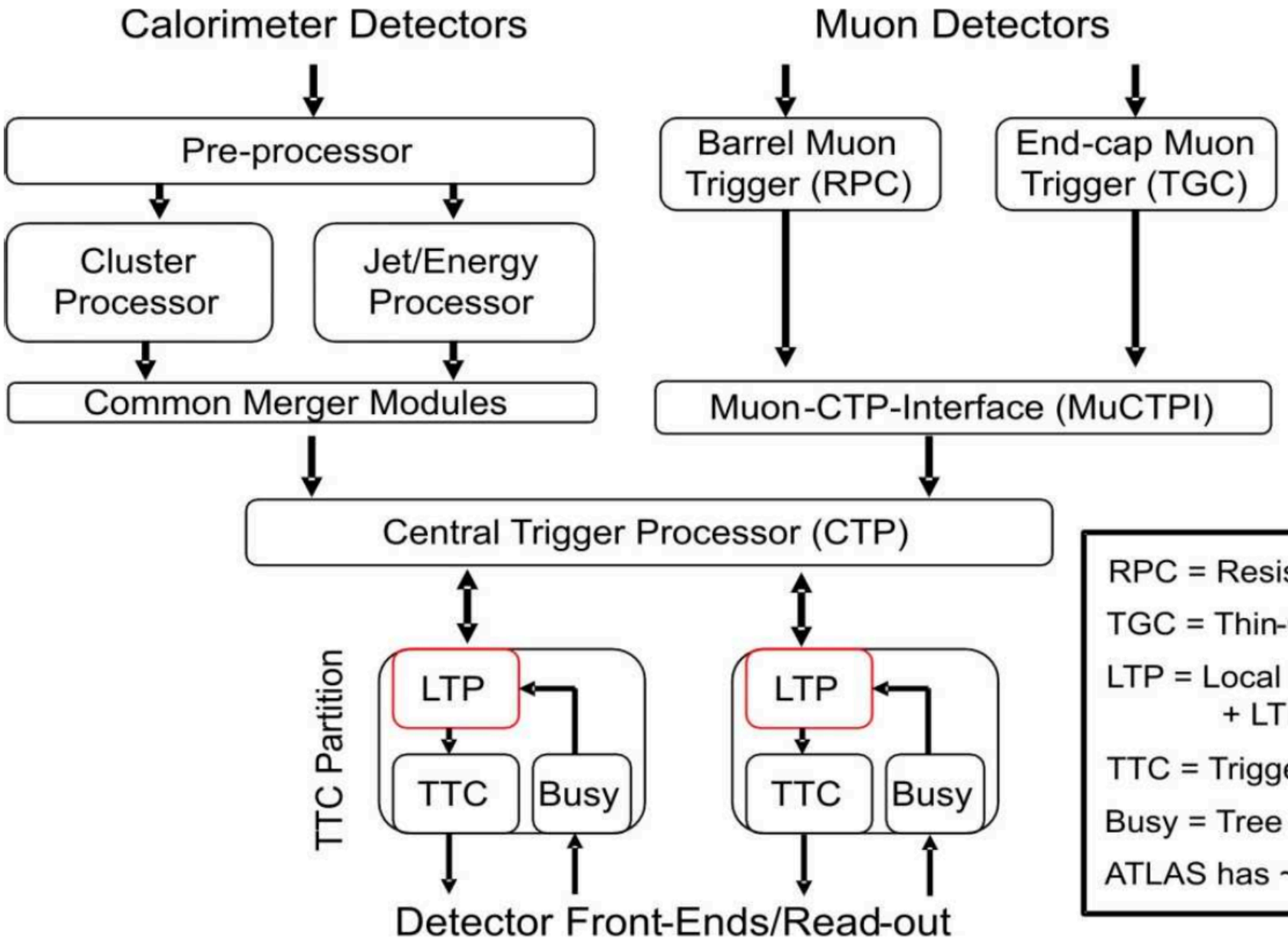


Fig. Ref

ATLAS LEVEL 1 TRIGGER SYSTEM



RPC = Resistive-Plate Chamber

TGC = Thin-Gap Plate Chamber

LTP = Local Trigger Processor + LTP interface

TTC = Trigger Timing & Control

Busy = Tree of ROD_Busy modules

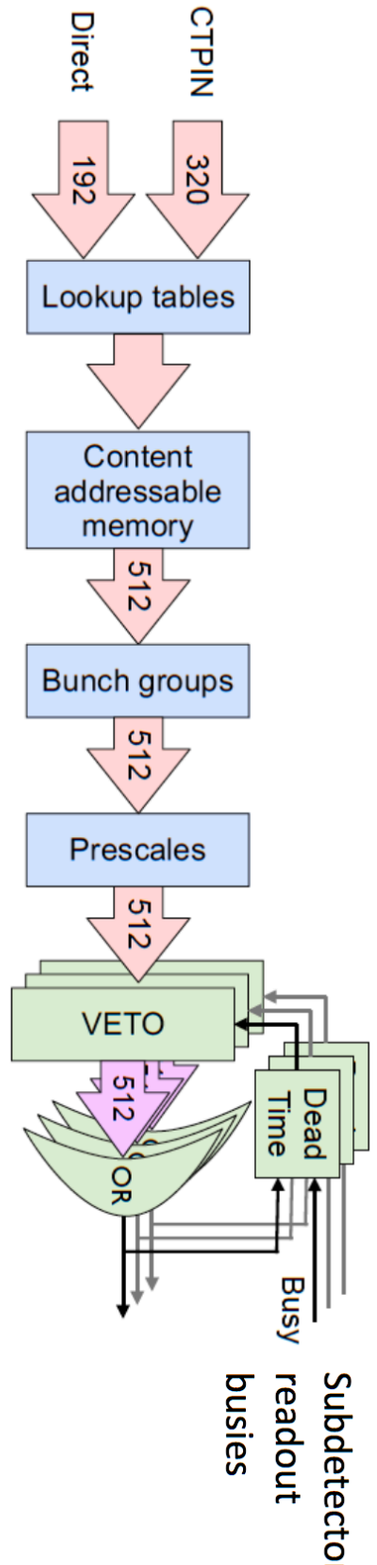
ATLAS has ~40 TTC partitions

Fig. Ref

CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

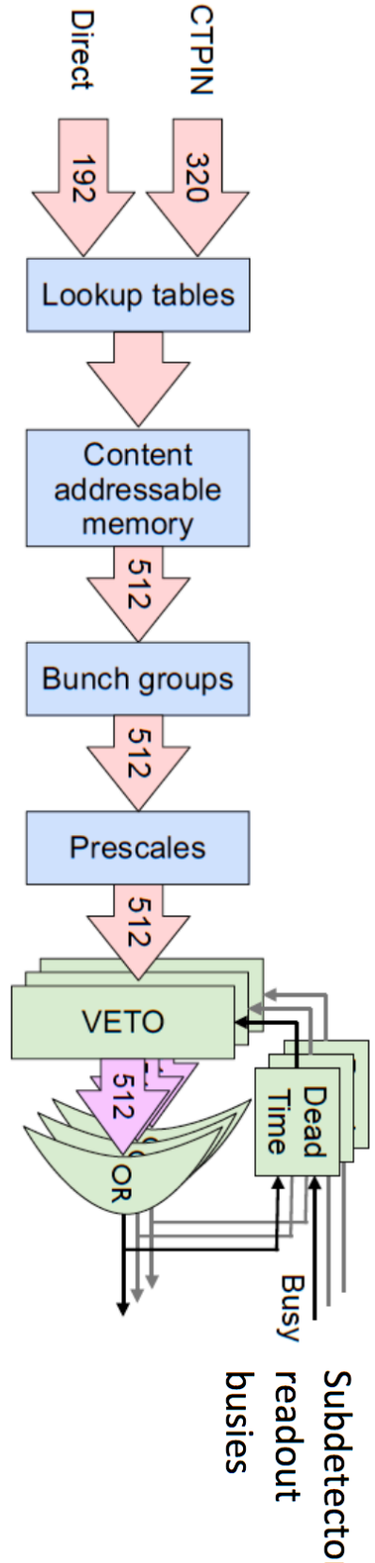
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:



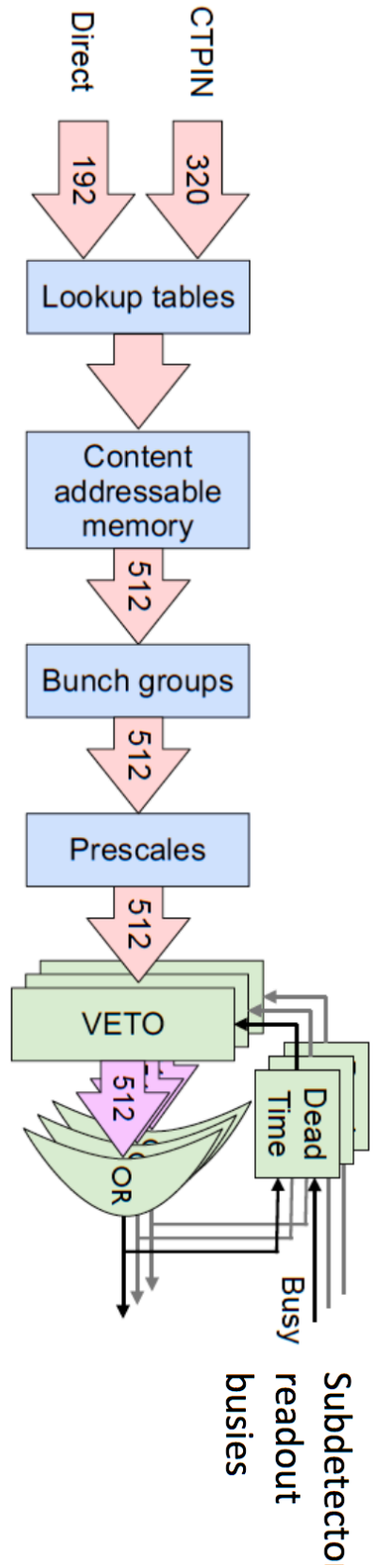
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions



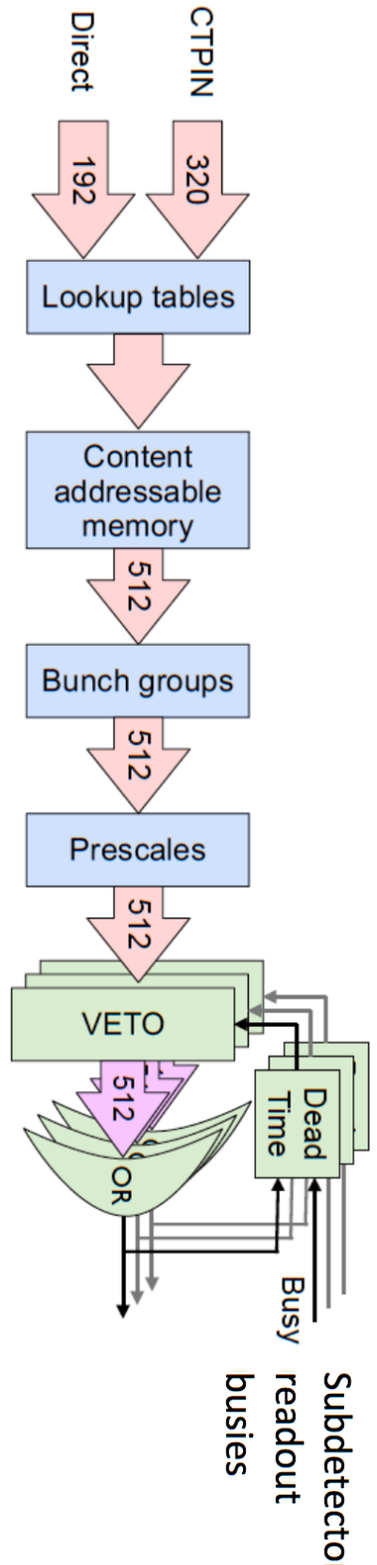
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions
  - Produces Level 1 Accept (L1A), a unique event identifier (24 + 8 bits) which is used, along with Bunch Crossing ID, to synchronize data to the rest of the system



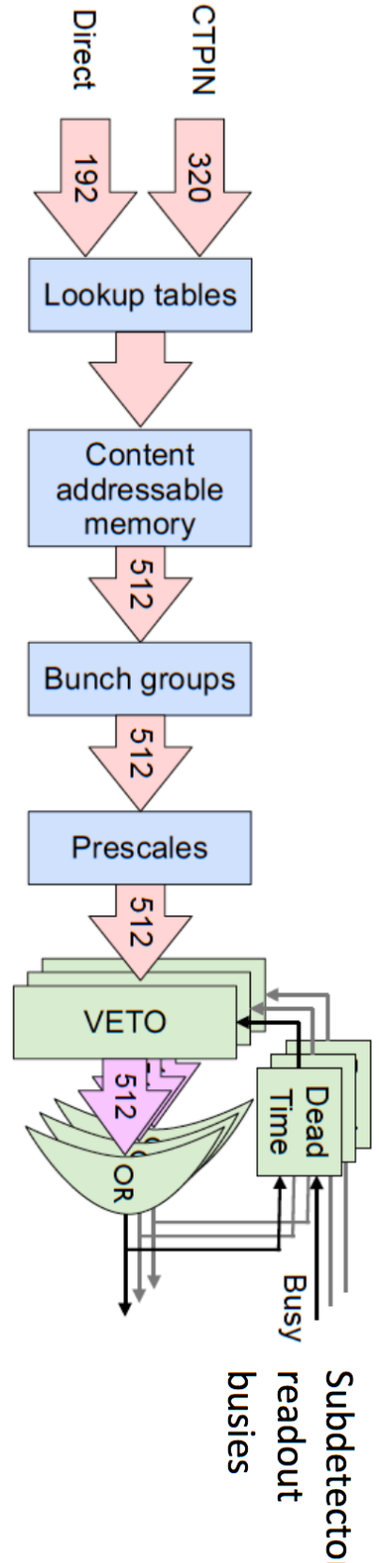
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions
  - Produces Level 1 Accept (L1A), a unique event identifier (24 + 8 bits) which is used, along with Bunch Crossing ID, to synchronize data to the rest of the system
  - Provides timing information to subdetectors from the LHC



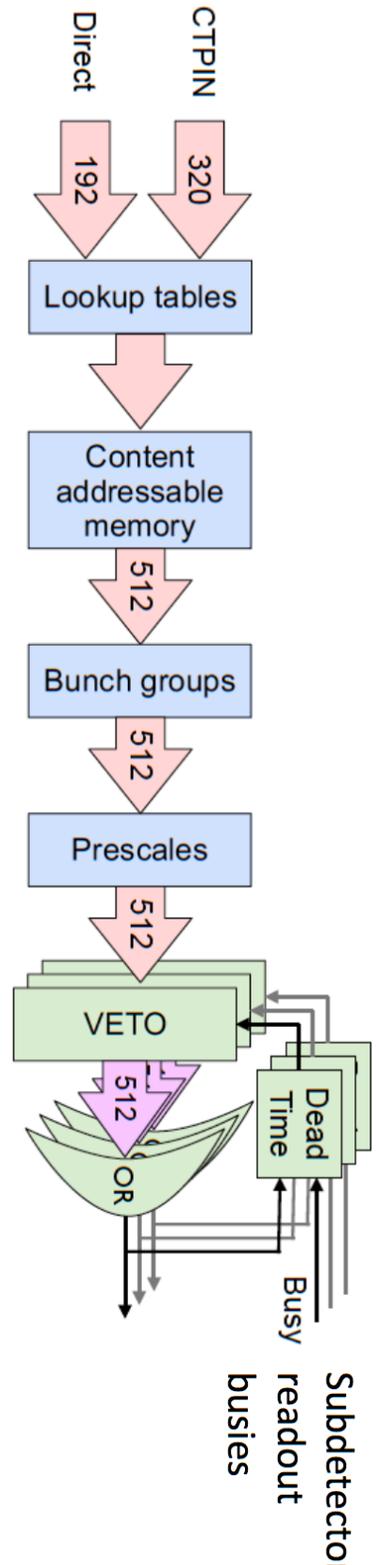
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions
  - Produces Level 1 Accept (L1A), a unique event identifier (24 + 8 bits) which is used, along with Bunch Crossing ID, to synchronize data to the rest of the system
  - Provides timing information to subdetectors from the LHC
  - Provides a GPS-based UTC time stamp that is included in the trigger information that is sent to the readout system



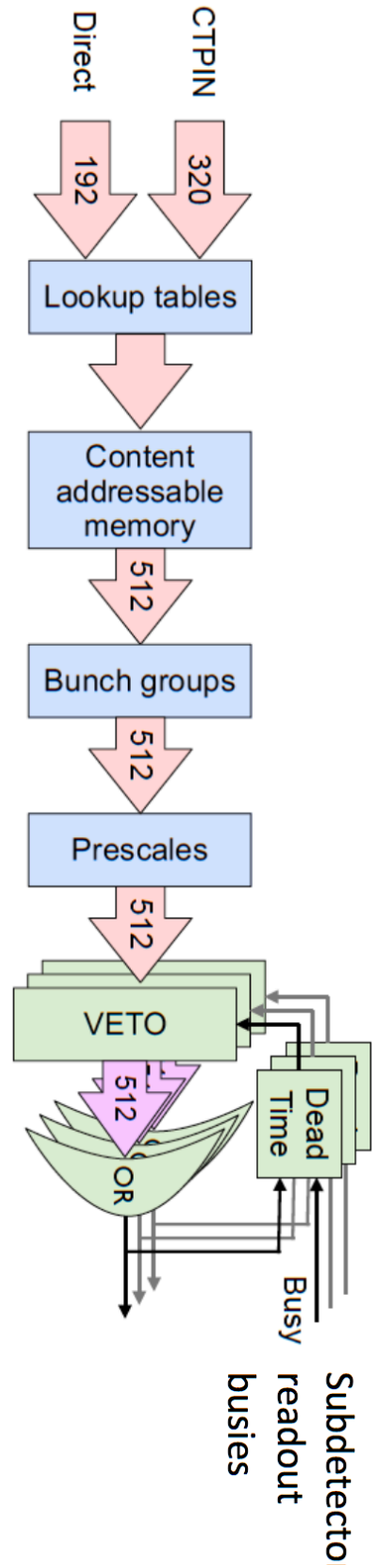
CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions
  - Produces Level 1 Accept (L1A), a unique event identifier (24 + 8 bits) which is used, along with Bunch Crossing ID, to synchronize data to the rest of the system
  - Provides timing information to subdetectors from the LHC
  - Provides a GPS-based UTC time stamp that is included in the trigger information that is sent to the readout system
  - Controls trigger operation under detector BUSY

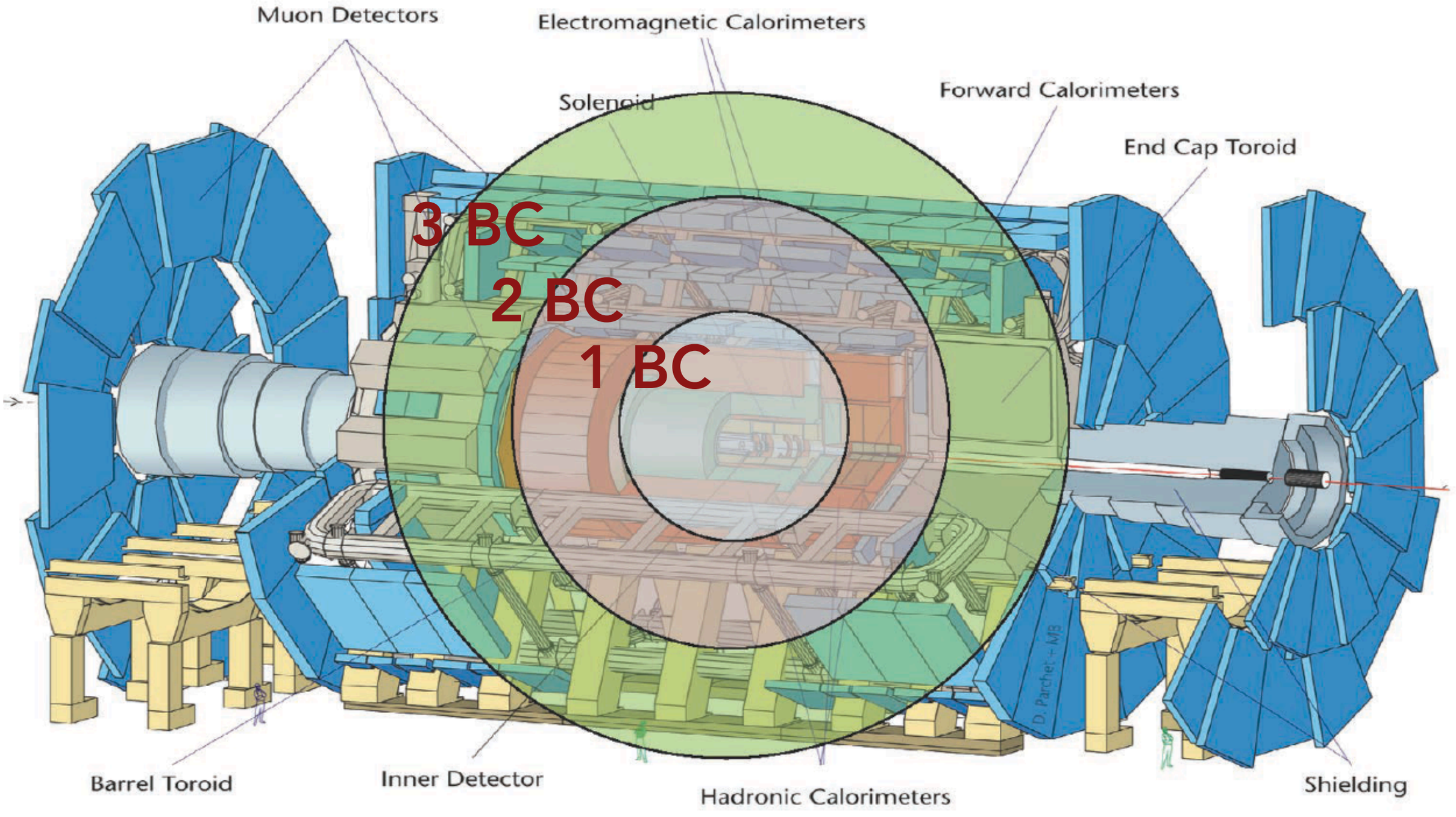


CENTRAL TRIGGER PROCESSOR & TIMING TRIGGER AND CONTROL SYSTEM

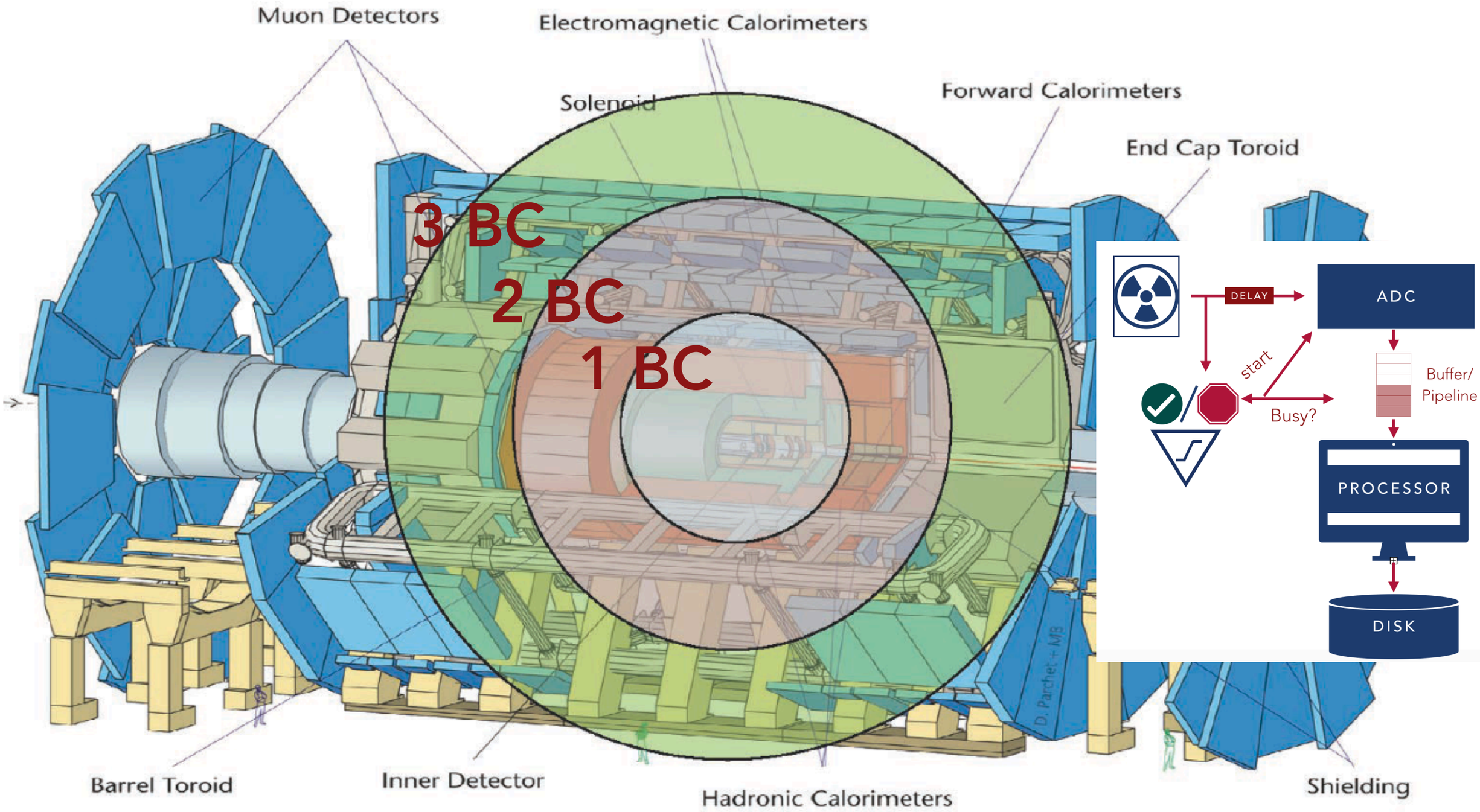
- Central Trigger Processor (CTP) and the Trigger Timing and Control (TTC) form the brains of the Level-1 Trigger:
  - Takes primitives from L1Calo/L1Muon/L1Topo and determines trigger decisions
  - Produces Level 1 Accept (L1A), a unique event identifier (24 + 8 bits) which is used, along with Bunch Crossing ID, to synchronize data to the rest of the system
- Provides timing information to subdetectors from the LHC
- Provides a GPS-based UTC time stamp that is included in the trigger information that is sent to the readout system
- Controls trigger operation under detector BUSY
- ***All within 100ns***



TIMING IS EVERYTHING



TIMING IS EVERYTHING



ATLAS DEADTIME

- Simple dead-time veto:
  - No new L1A after fixed number of BC
- Leaky-bucket Deadtime Algorithm:
  - Bucket leaks at rate R
  - Contents increase by X at each L1A until full, then BUSY is asserted
- Allows system to maintain high efficiency for data taking

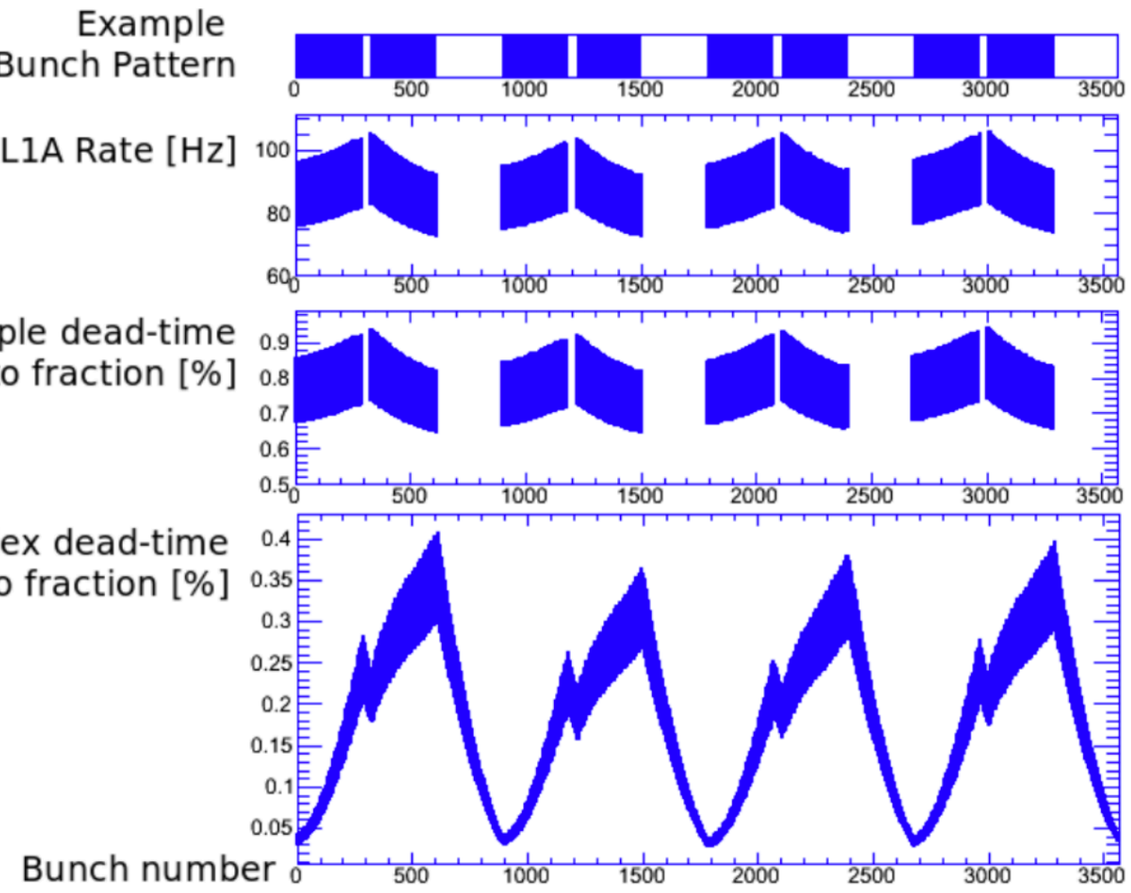


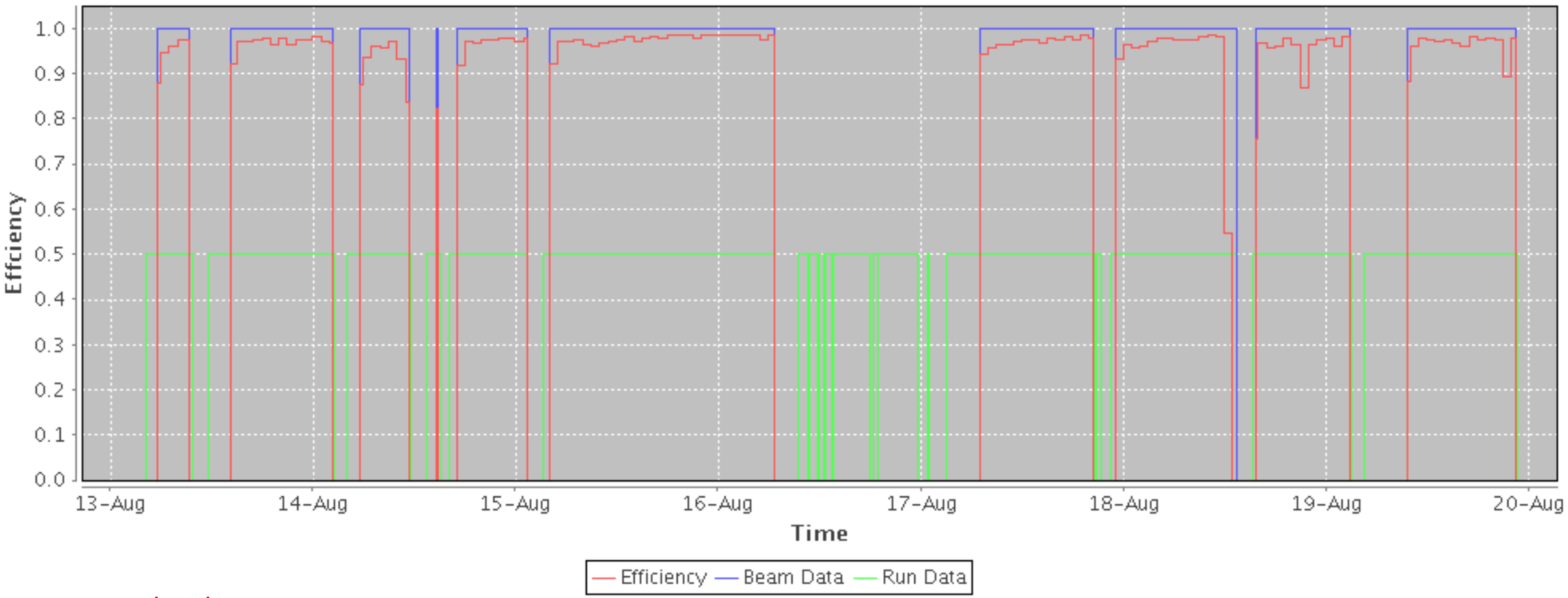
Fig. Ref

ATLAS DEADTIME

- Simple dead-time veto:
  - No new L1A after fixed number of BC
- Leaky-bucket Deadtime Algorithm:
  - Bucket leaks at rate R
  - Contents increase by X at each L1A until full, then BUSY is asserted
- Allows system to maintain high efficiency for data taking

Fig. Ref

ATLAS DEADTIME

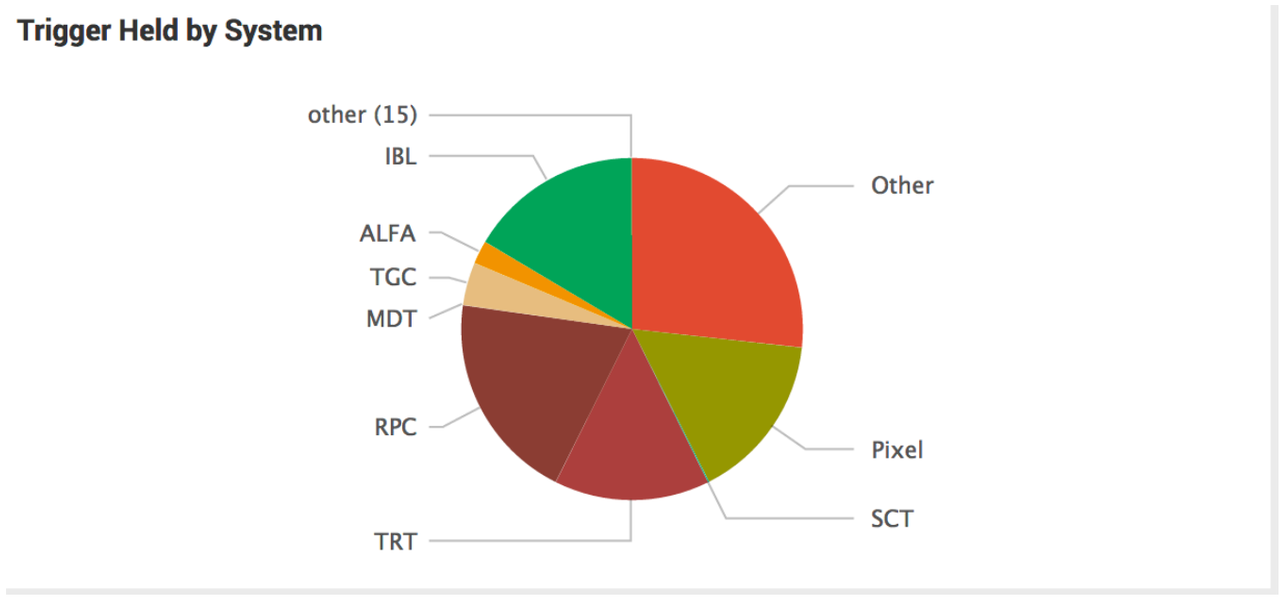
- Simple dead-time veto:
- 

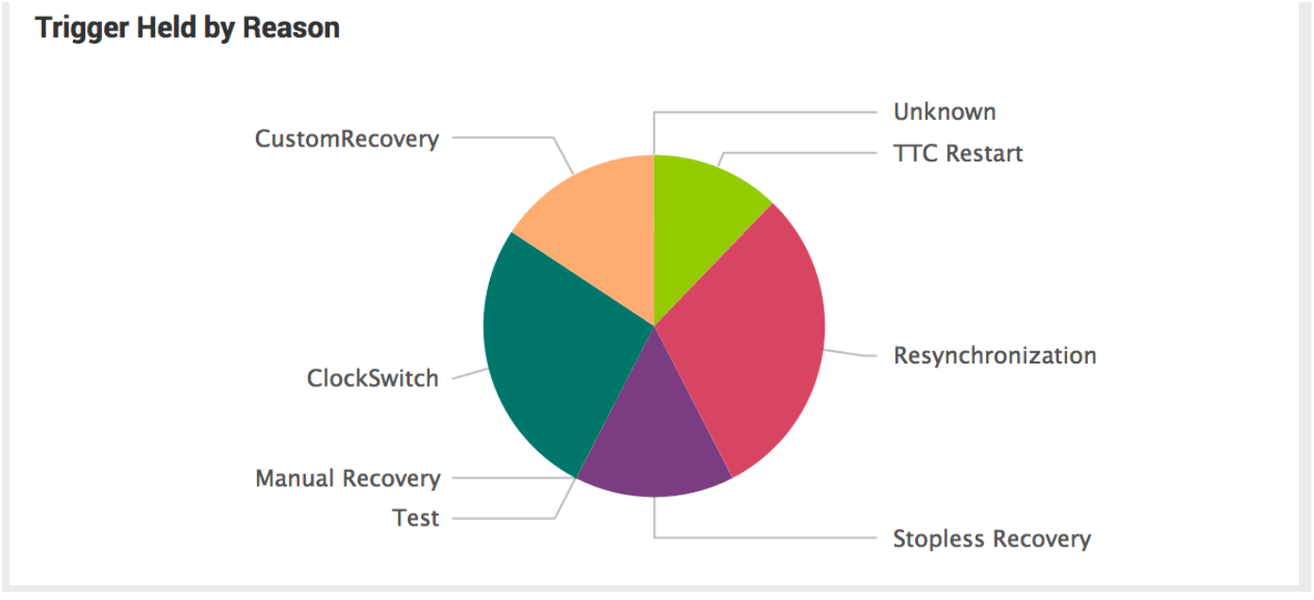
asserted

- Allows system to maintain high efficiency for data taking

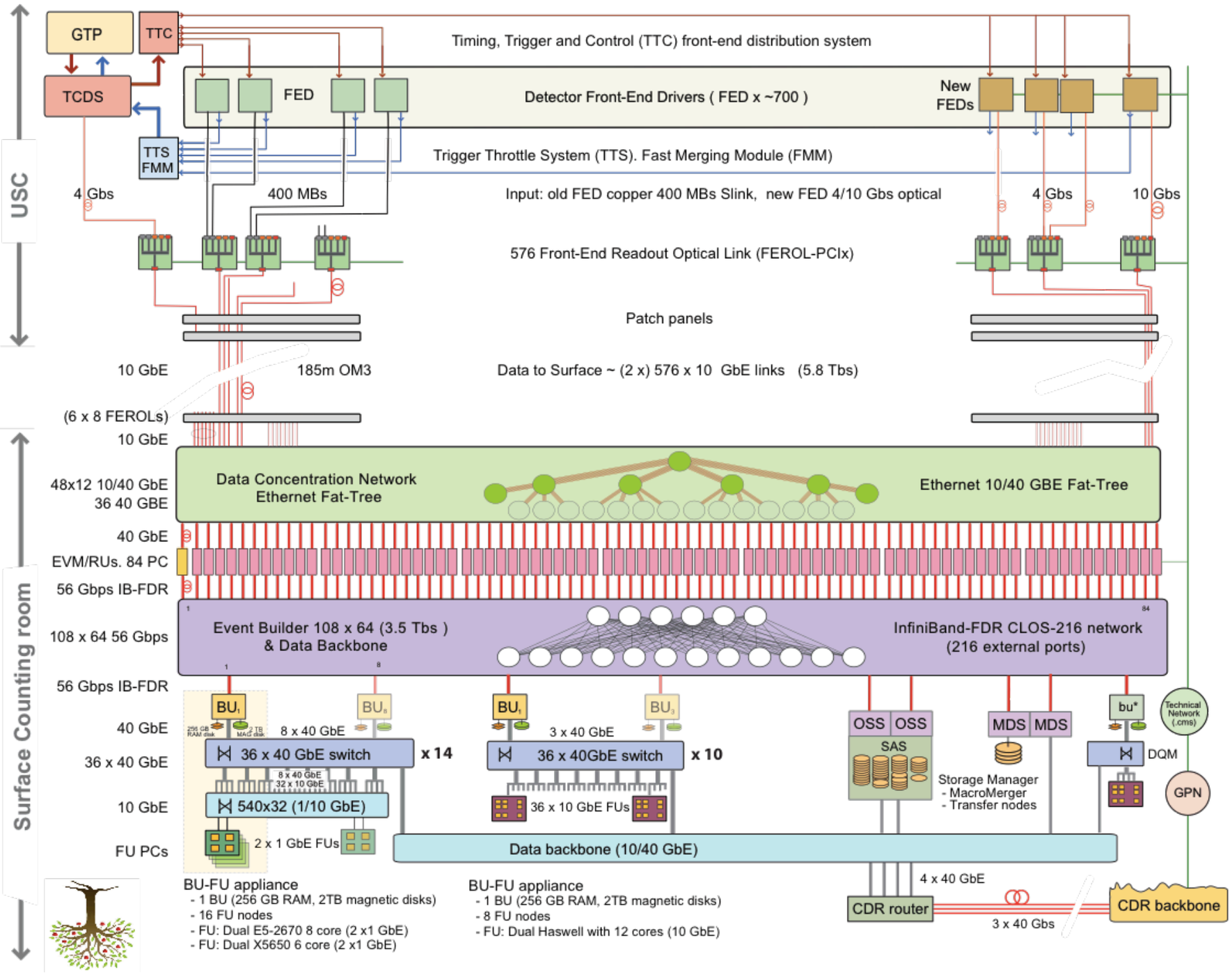
ATLAS DEADTIME

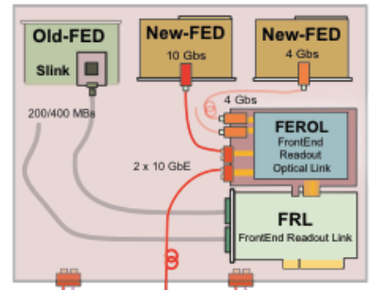
- Simple dead-time veto:
  - No new L1A after fixed number of BC
- Leaky-bucket Deadtime Algorithm:
  - Bucket leaks at rate R
  - Contents increase by X at each L1A until full, then BUSY is asserted
- Allows system to maintain high efficiency for data taking





CMS RUN II TDAQ





FEROLs

30 m

864, LC-LC patch cables

Patch panel #1

10 m

864, LC-E2K cords

Patch panel #2

185 m OM3

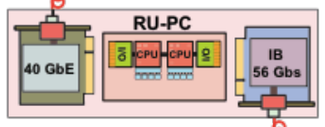
E2K-E2K pair fibers

Patch panel #3

10 m

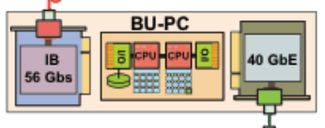
E2k-LC cords

576 x 84 FED router and concentrator
48x12 (10/40 GbE) switches

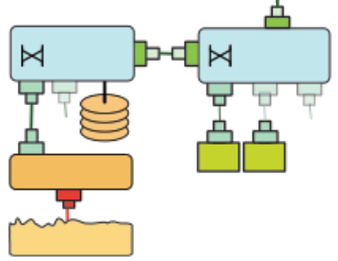


84 Readout Units (RU)
- Dual E5-2670 (8 core), 32 GB RAM
- Data aggregation
- Event fragments buffer (seconds)
- EVM control and synchronization

84 x 64 Event Builder



64 Builder Units (BU)
- Dual E5-2670 (8 core), 32+256 GB RAM
- Event building
- Temoporary recording FS FU-inoput (256 GB RAM disk)
- Temoporary recording FS FU-ioutput (2 TB magnetic disk RAID)



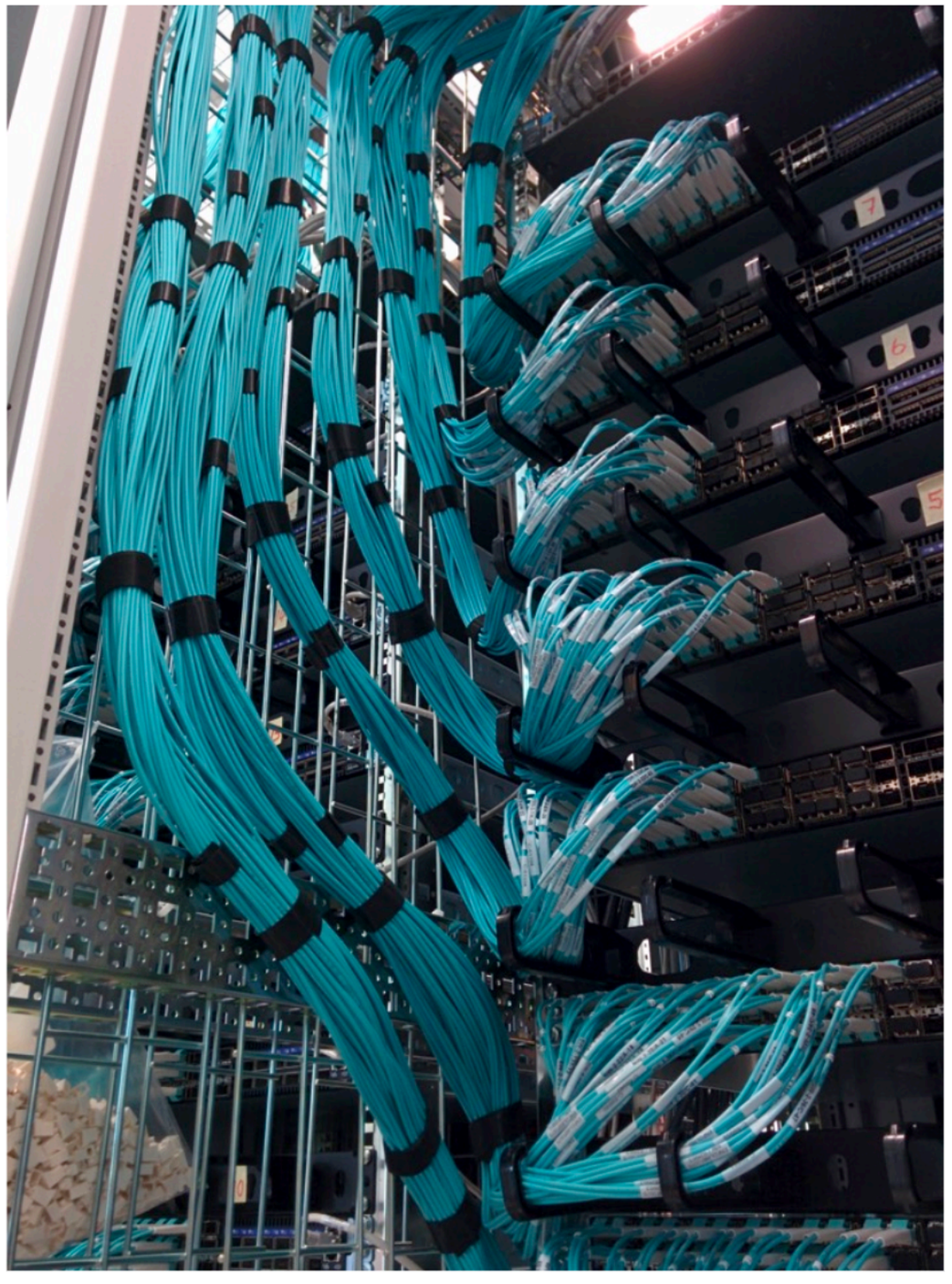
Filter farms (FU)
- 288 x dual X5650 (6 core), 24 GB RAM
- 256 x dual E5-2670 (8 core), 32 GB RAM
- 360 x dual E5-26803 (12 core), 64 GB RM
- total of 904 nodes, 16192 cores

Storage Manager (SM)

[Fig. Ref]

CMS DAQ/HLT NETWORK STATISTICS

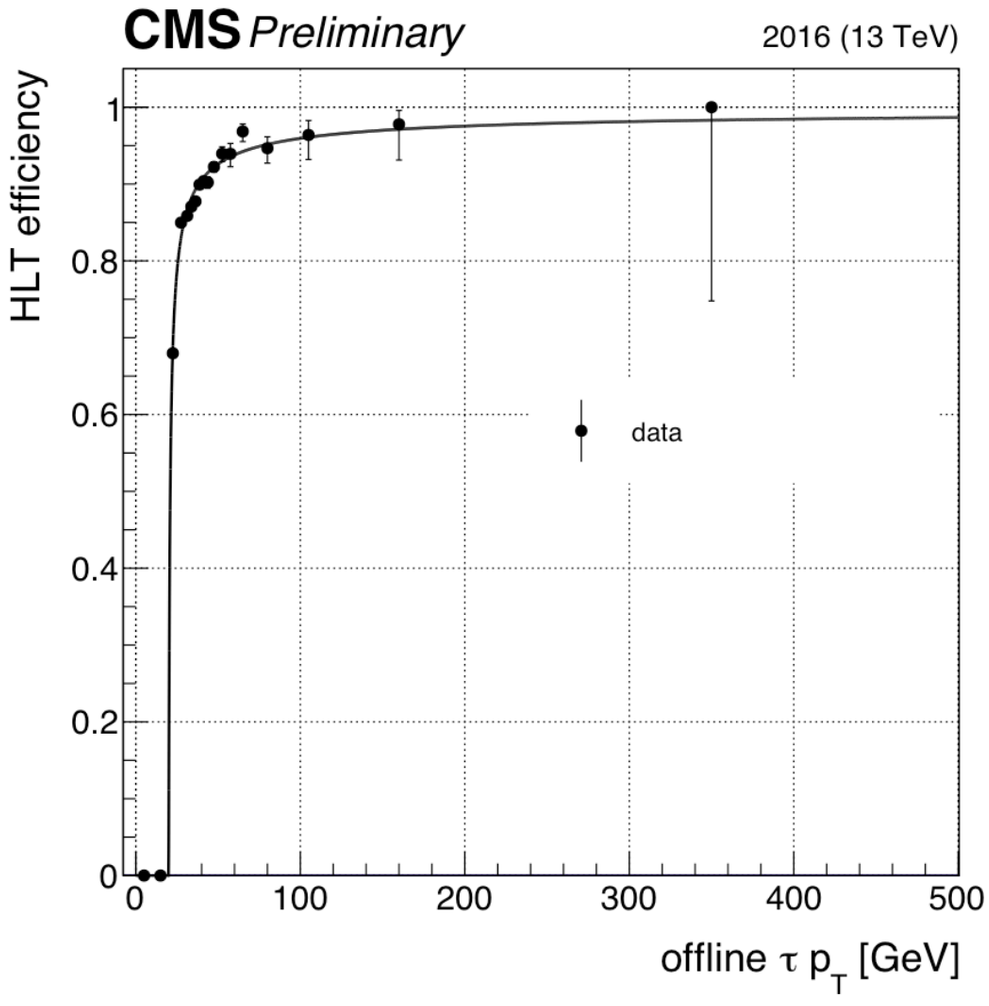
Data concentrator patch panels



and switches

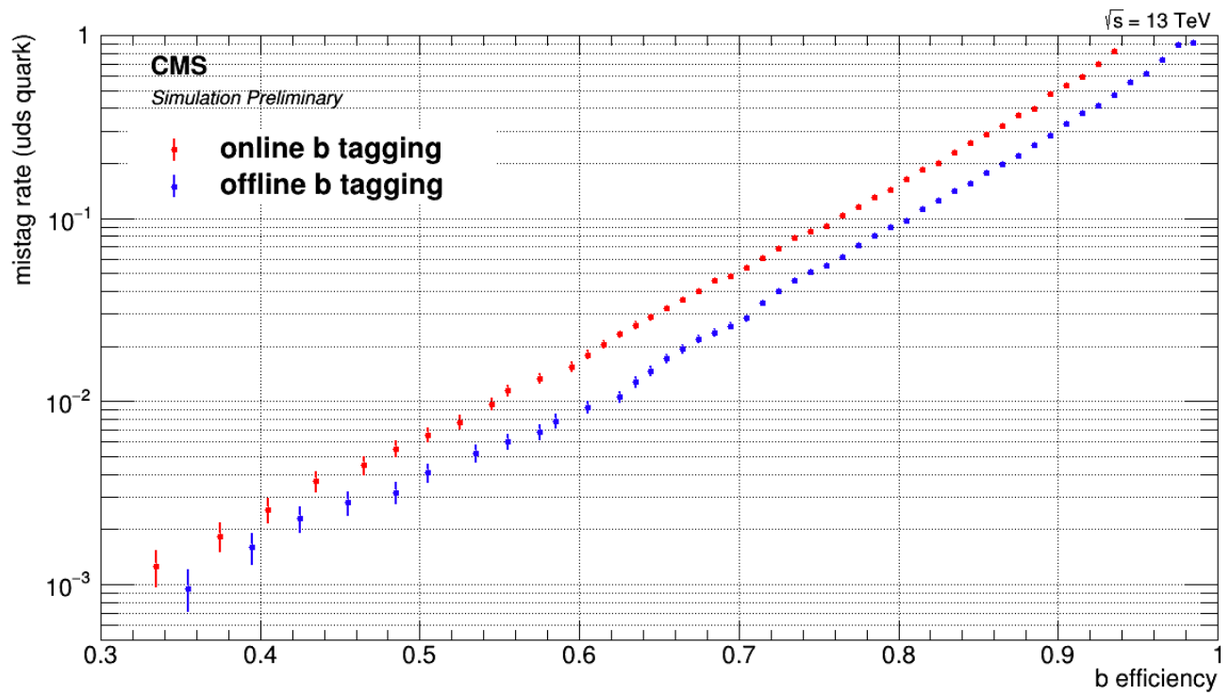
HIGH LEVEL TRIGGERS

- Goal of HLT is to make trigger selections from objects which are as close to offline selections as possible within CPU constraints
  - Minimizes unnecessary loss of efficiency, and importantly, systematic uncertainties!
- Typical trade-offs:
  - Less precise energy resolution
  - Raising thresholds to save CPU
  - Narrower cones for isolation requirements, tracking for b-tagging, etc.



HIGH LEVEL TRIGGERS

- Goal of HLT is to make trigger selections from objects which are as close to offline selections as possible within CPU constraints
  - Minimizes unnecessary loss of efficiency, and importantly, systematic uncertainties!



- Typical trade-offs:
  - Less precise energy resolution
  - Raising thresholds to save CPU
  - Narrower cones for isolation requirements, tracking for b-tagging, etc.

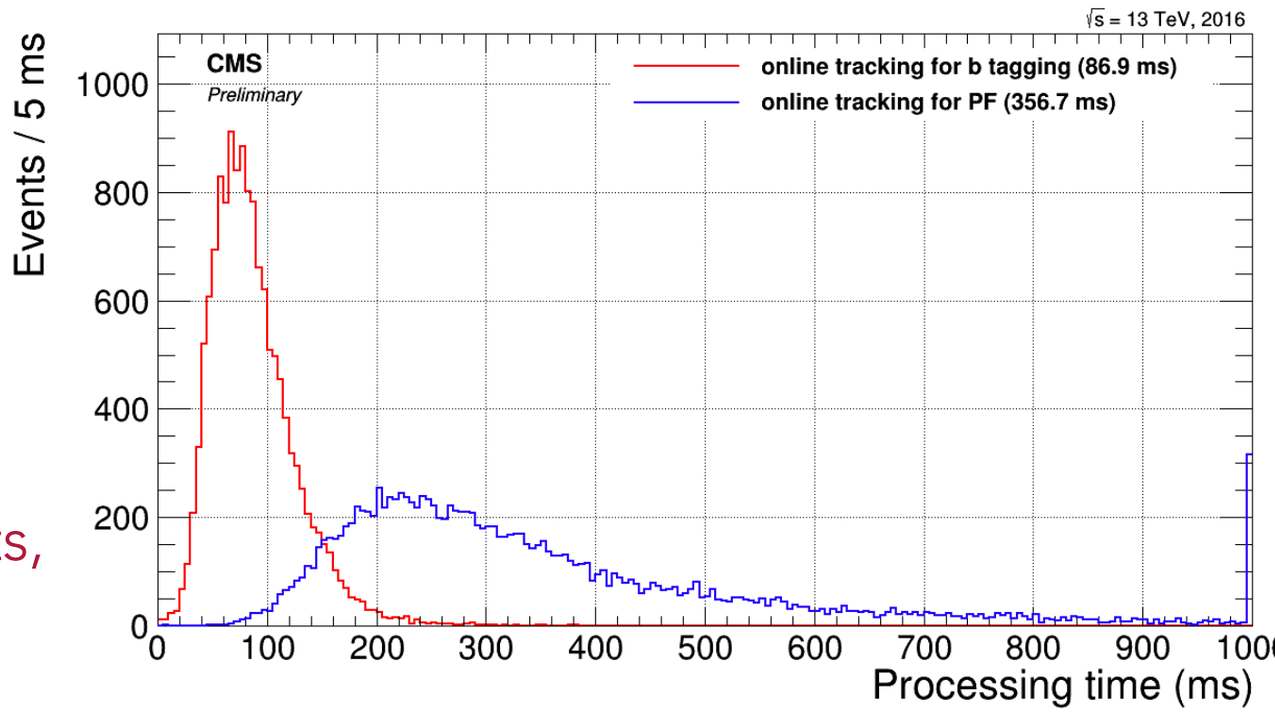
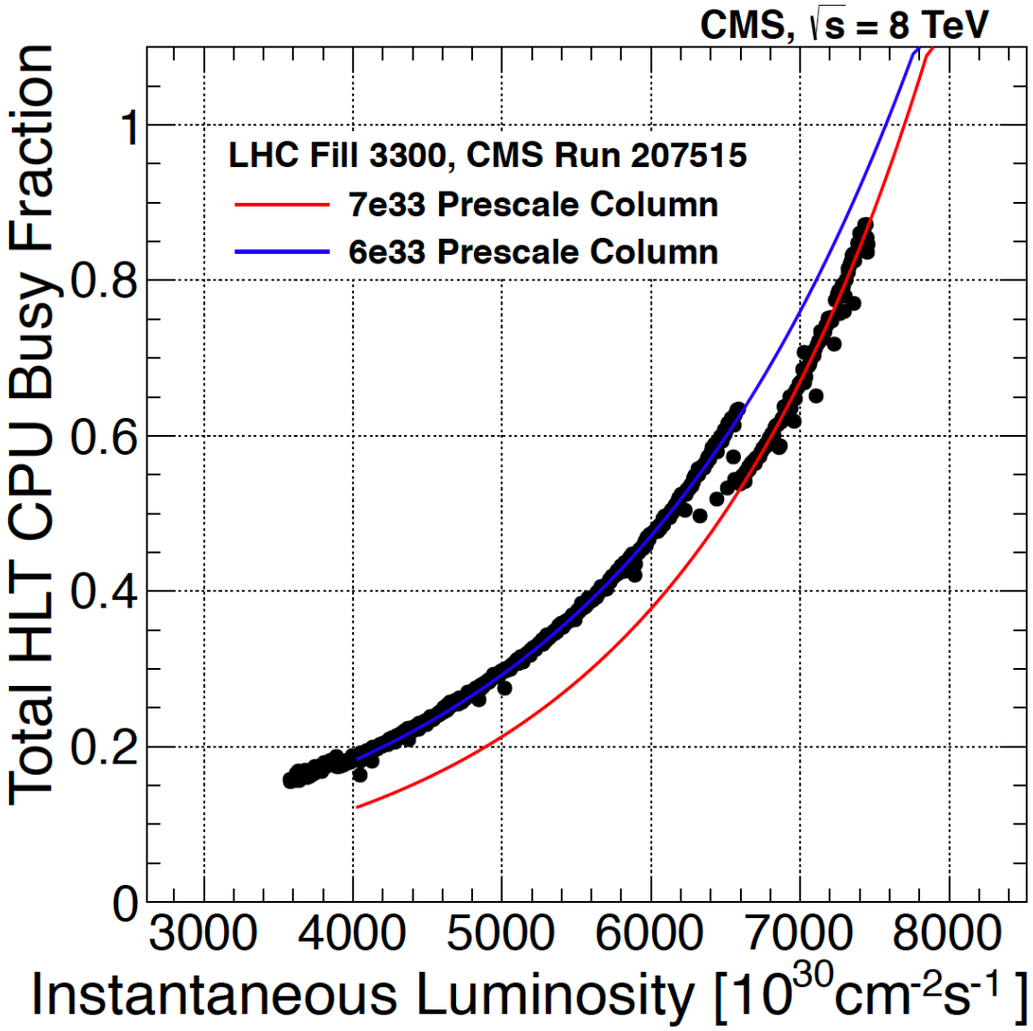
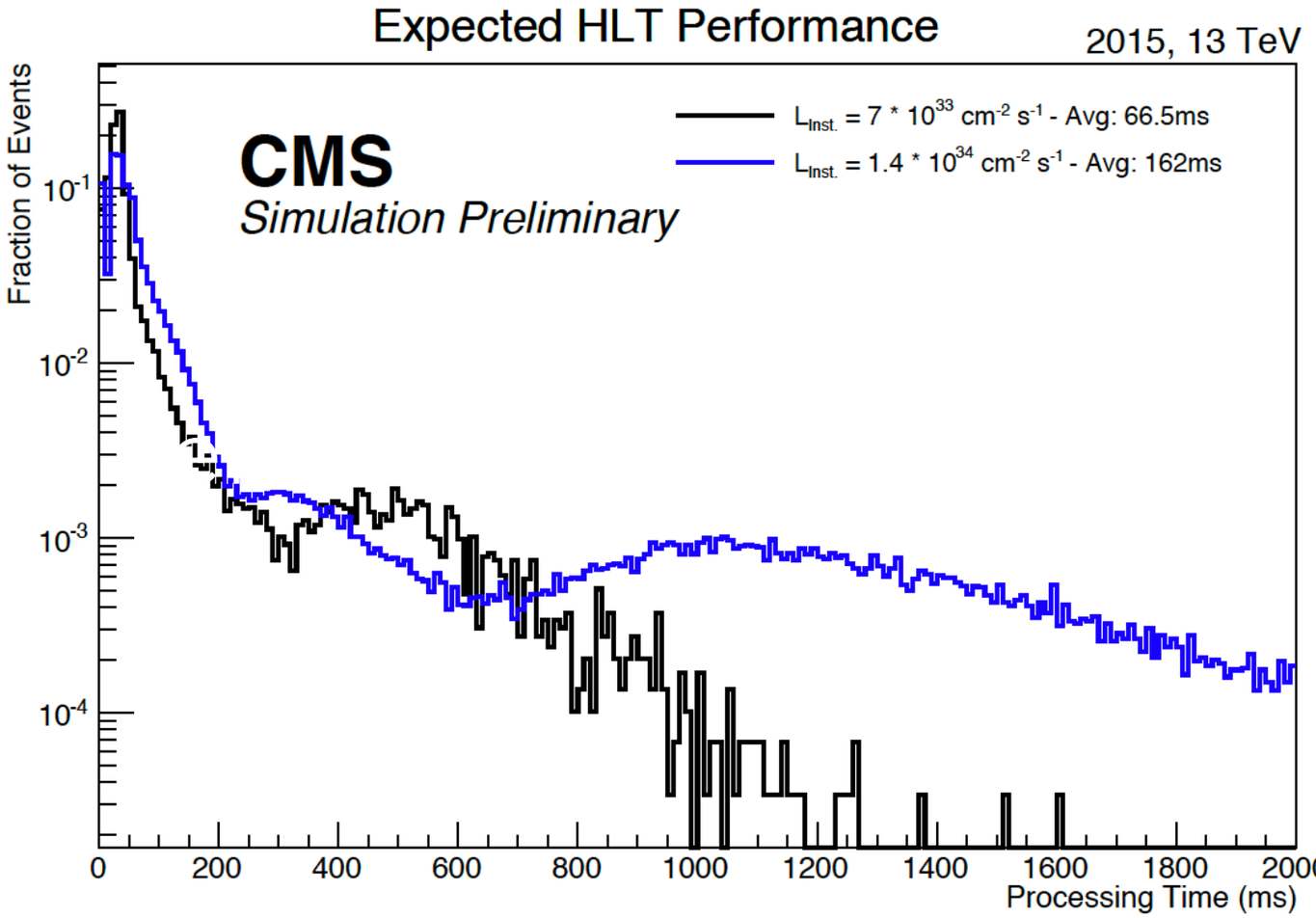


Fig Ref.

TIMING



[Fig Ref.]



[Fig Ref.]

TIMING

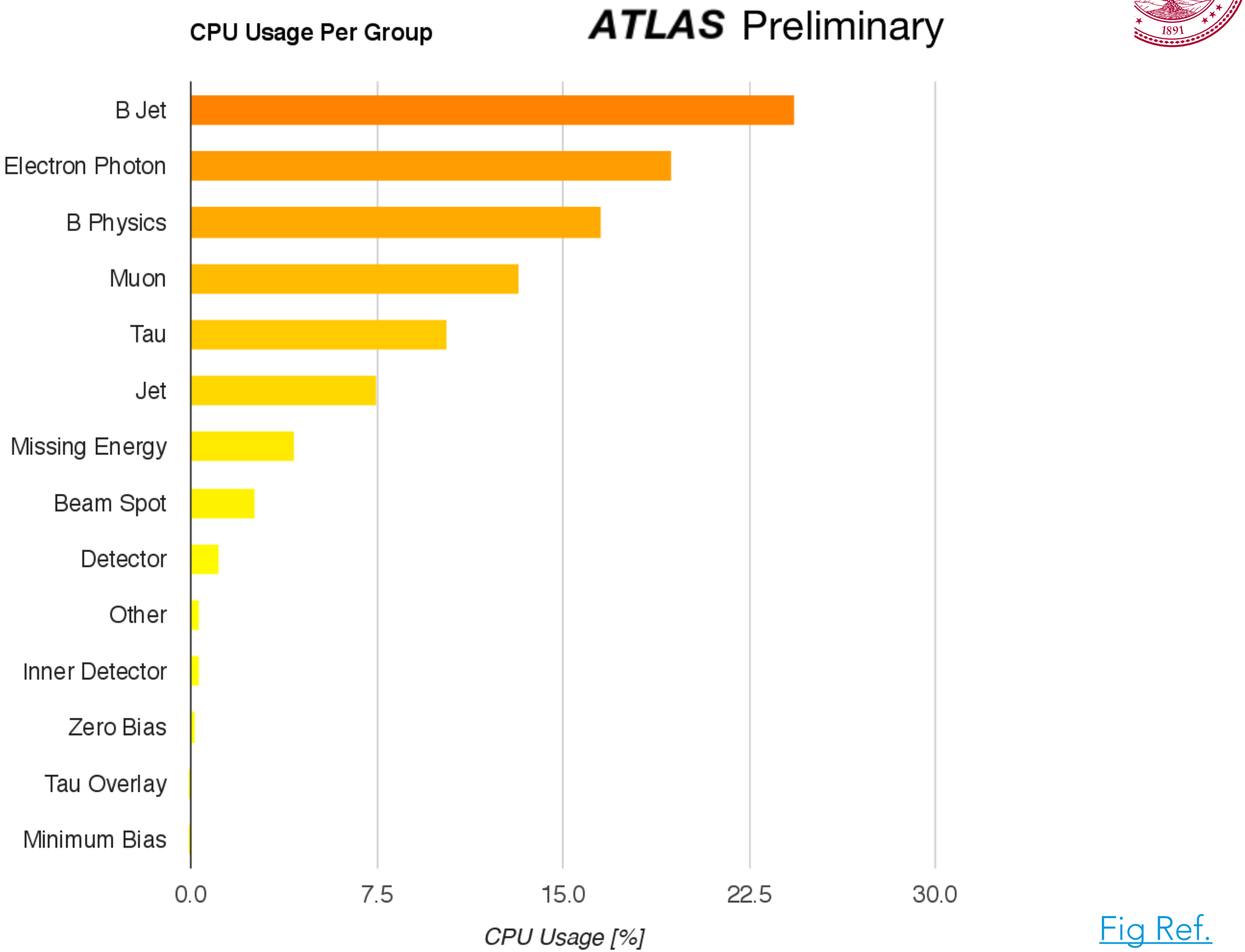


Fig Ref.

THE ART OF MENU BUILDING

OPTIMIZING FOR PHYSICS

- Trigger menu building is an optimization of trigger & DAQ resources to meet an experiment's priorities

- Balance:

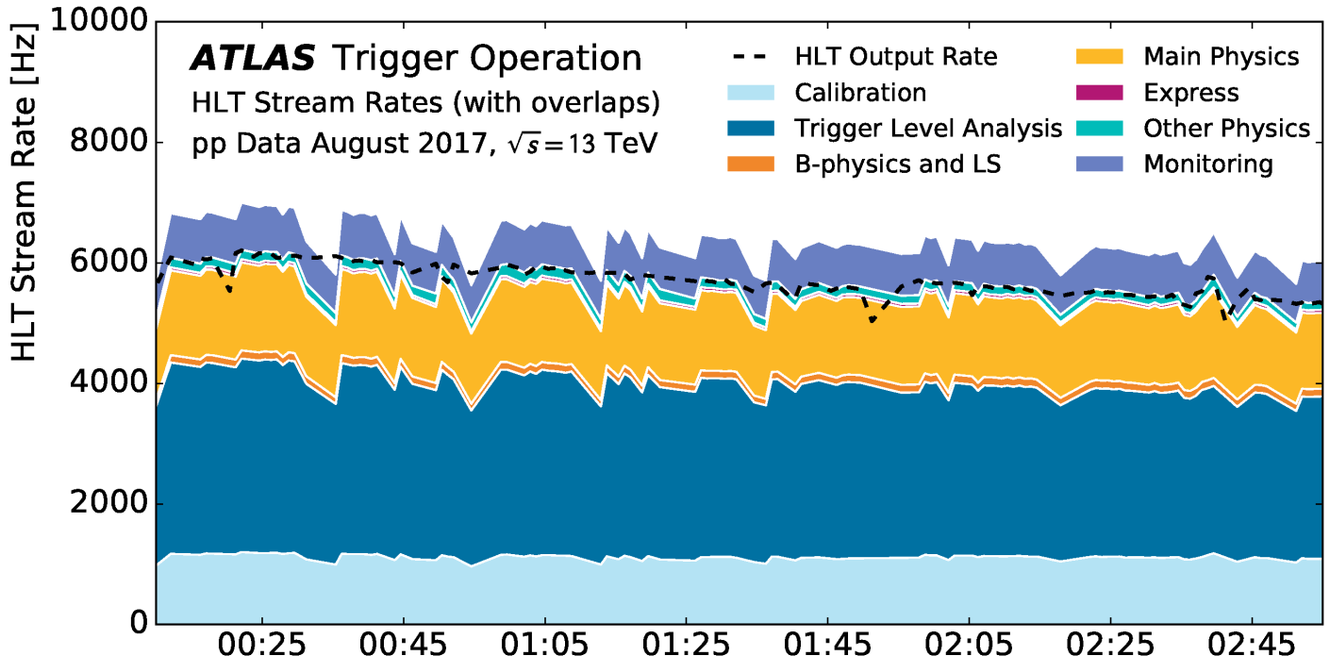
  - Bandwidth of L1 output

  - Availability of CPU resources in HLT

    - Rate of events to process versus the complexity of algorithms

  - Output bandwidth to storage

- ***What physics do we want to record?***



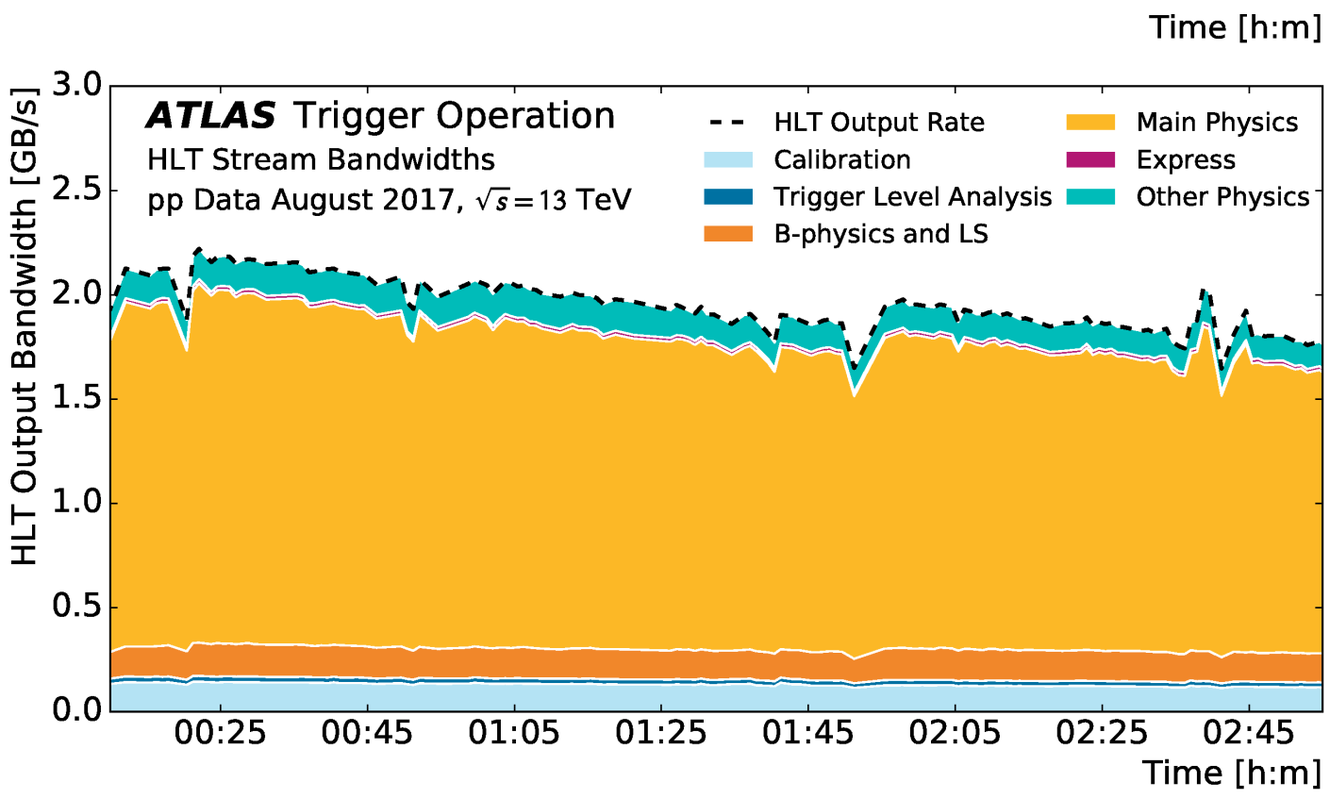


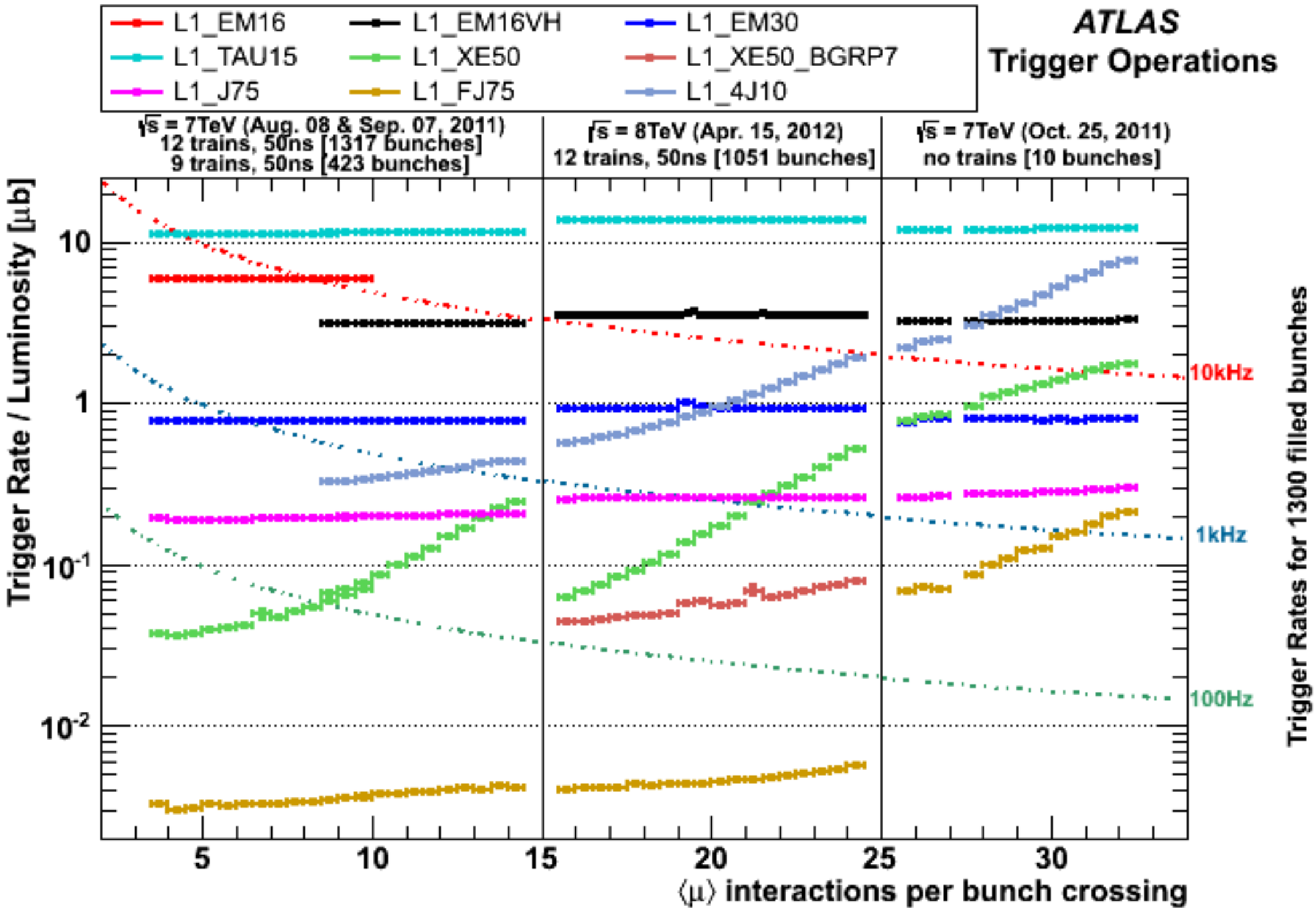
Fig Ref.

PRIORITIES @ 3E34

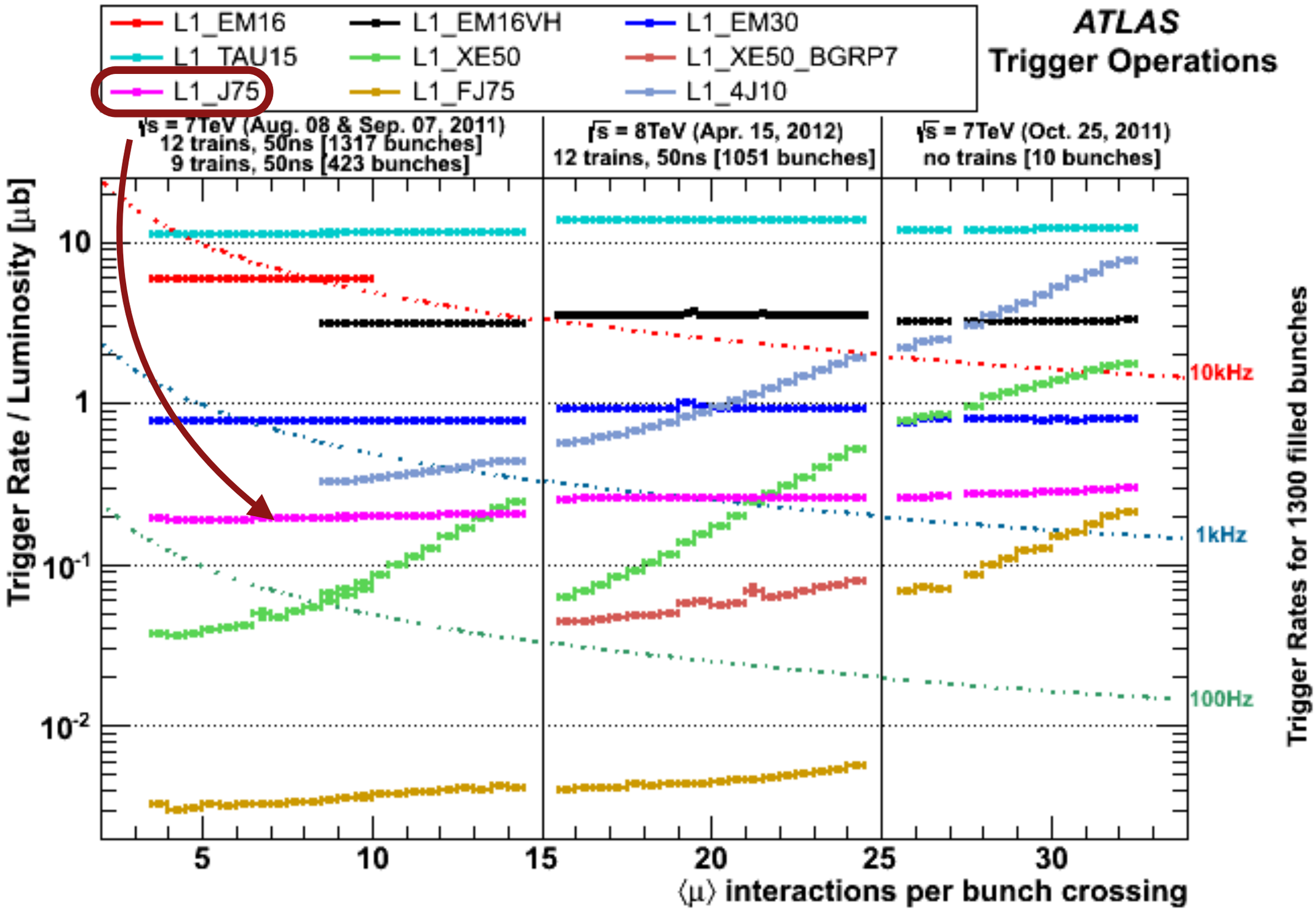
new hardware optimized

Run 1 unoptimized	Offline p_T Threshold [GeV]	Rate [kHz]	Run 2 optimized	Offline p_T Threshold [GeV]	Rate [kHz]	Run 3	Offline p_T Threshold [GeV]	Rate [kHz]
EM18VH	25	130	EM30VHI	38	14	EM25VHR	32	14
EM30	37	61	EM80	100	2.5	EM80	100	2.5
2EM10	2x17	168	2EM15VHI	2x22	2.9	2EM12VHR	2x19	5.0
EM total		**270**			**18**			**20**
MU15	25	150	MU20	25	28	MU20	25	15
2MU10	2x12	14	2MU11	2x12	4.0	2MU11	2x12	4.0
Muon total		**164**			**32**			**19**
EM10VH_MU6	17,6	22	EM15VH_MU10	22,12	3.0	EM10VHR_MU10	17,12	3.0
			EM10H_2MU6	17,2x6	2.5	EM10HR_2MU6	17,2x6	1.0
TAU40	100	52	TAU80V	180	4.7	TAU80VR	180	3.2
			2TAU50V	2x110	3.8	2TAU40VR	2x100	3.9
2TAU11I_TAU15	30,40	147	2TAU20VI_3J20	2x50,60	5.2	2TAU15VR_3J15	2x40,50	8.1
2TAU11I_EM14VH	30,21	60	2TAU20VI_EM18VHI_3J18	50,25,60	2.8	2TAU15VR_EM13HR_3J13	40,20,50	3.3
			TAU15VI_MU15	40,20	3.8	TAU11VR_MU11	35,12	6.4
TAU15_XE35	40,80	63	TAU20VI_XE40_3J20	50,90,60	4.4	TAU15VR_XE40_3J15	40,90,50	5.0
Tau total		**238**			**20**			**25**
J75	200	34	J100	200	7.0	J100	200	7.0
4J15	4x55	87	4J25	4x60	3.3	4J25	4x60	3.3
			J75_XE40	150,150	8.3	J75_XE40	150,150	8.3
XE40	120	157	XE90	250	10	XE70	200	13
Jet/E_T^{miss} total[a]		**306**			**25**			**25**
Topological triggers		**-**			**~5**			**~20**
Total		**~800**			**~100**			**~100**

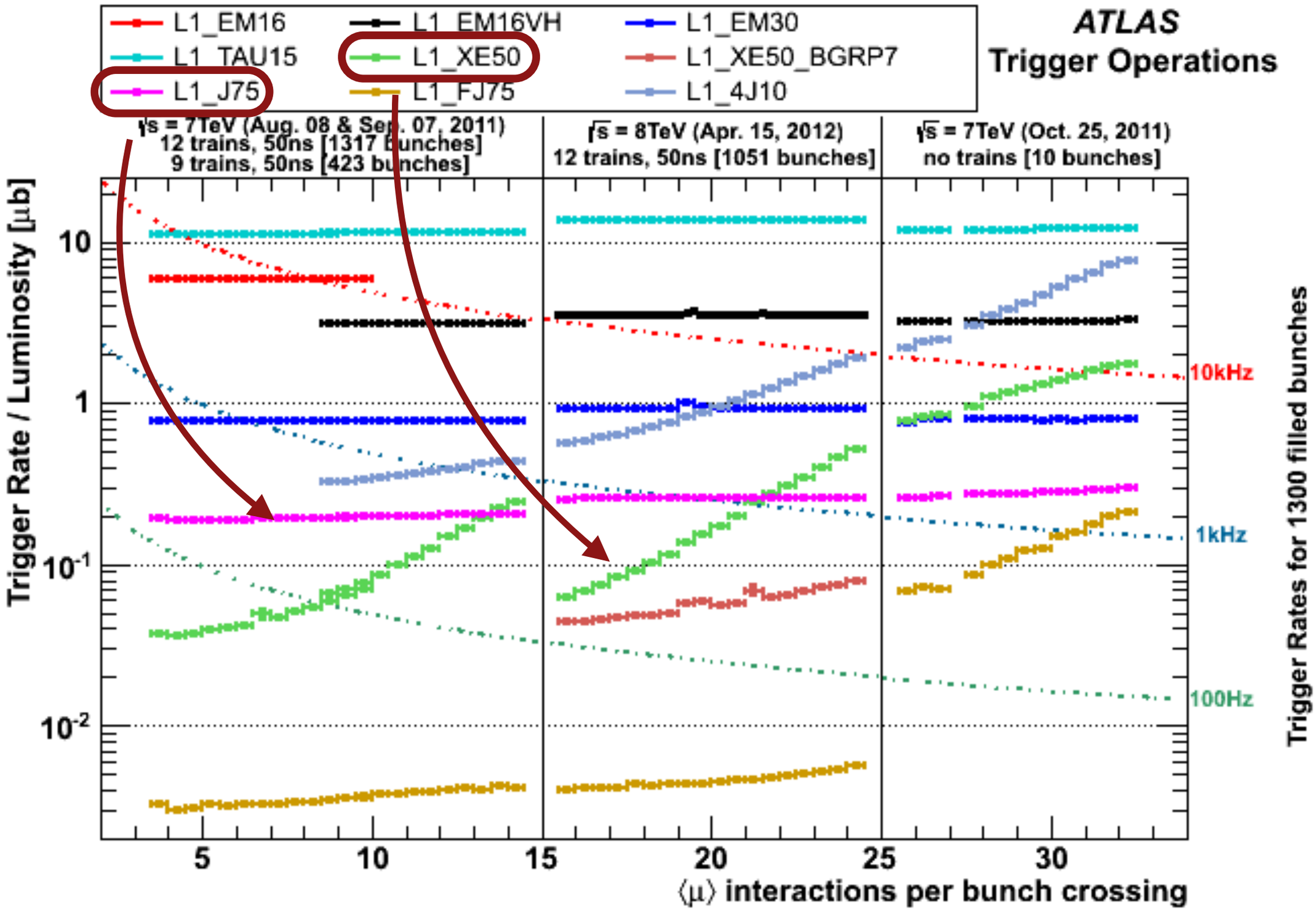
PILE-UP DEPENDENCE



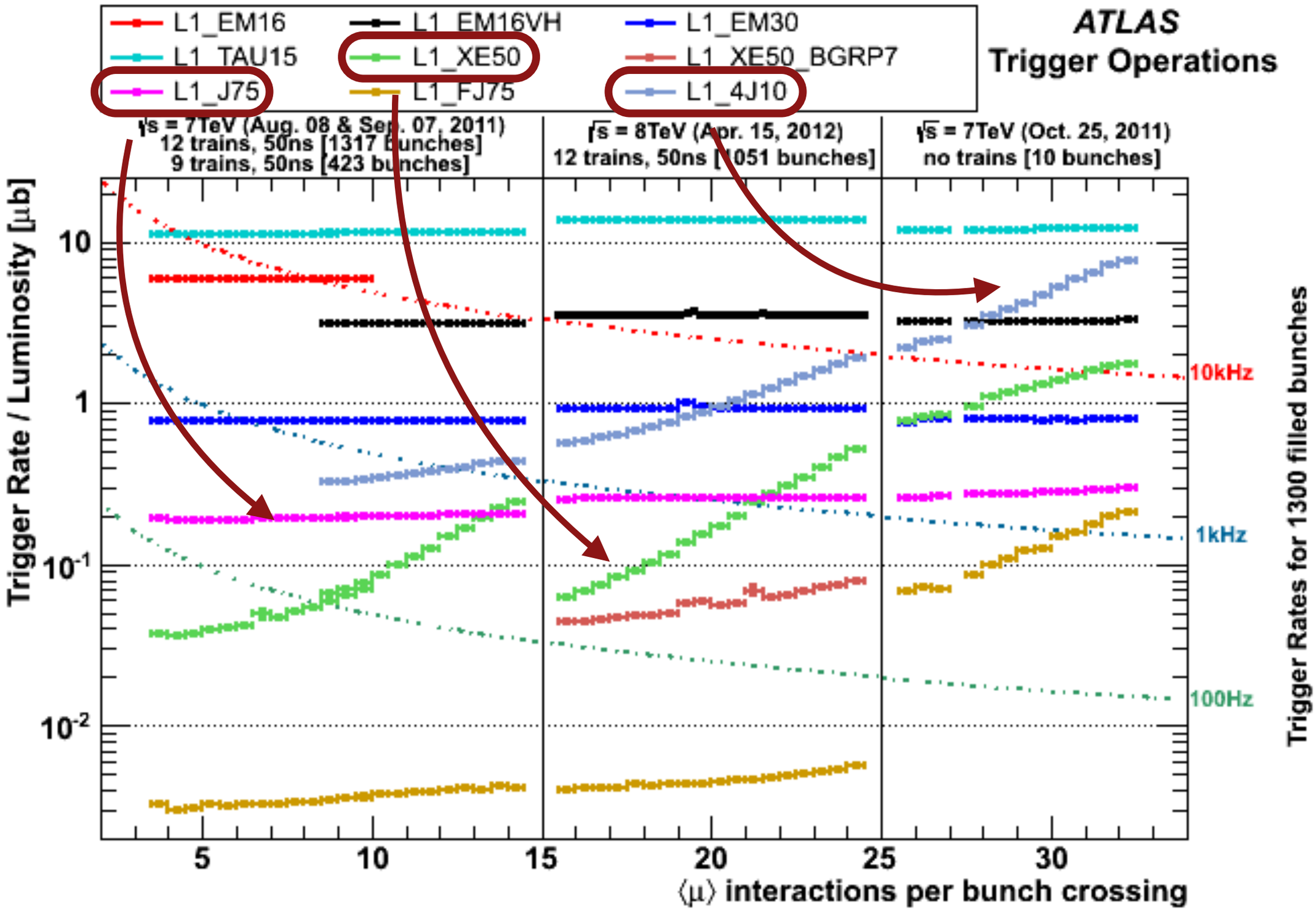
PILE-UP DEPENDENCE



PILE-UP DEPENDENCE

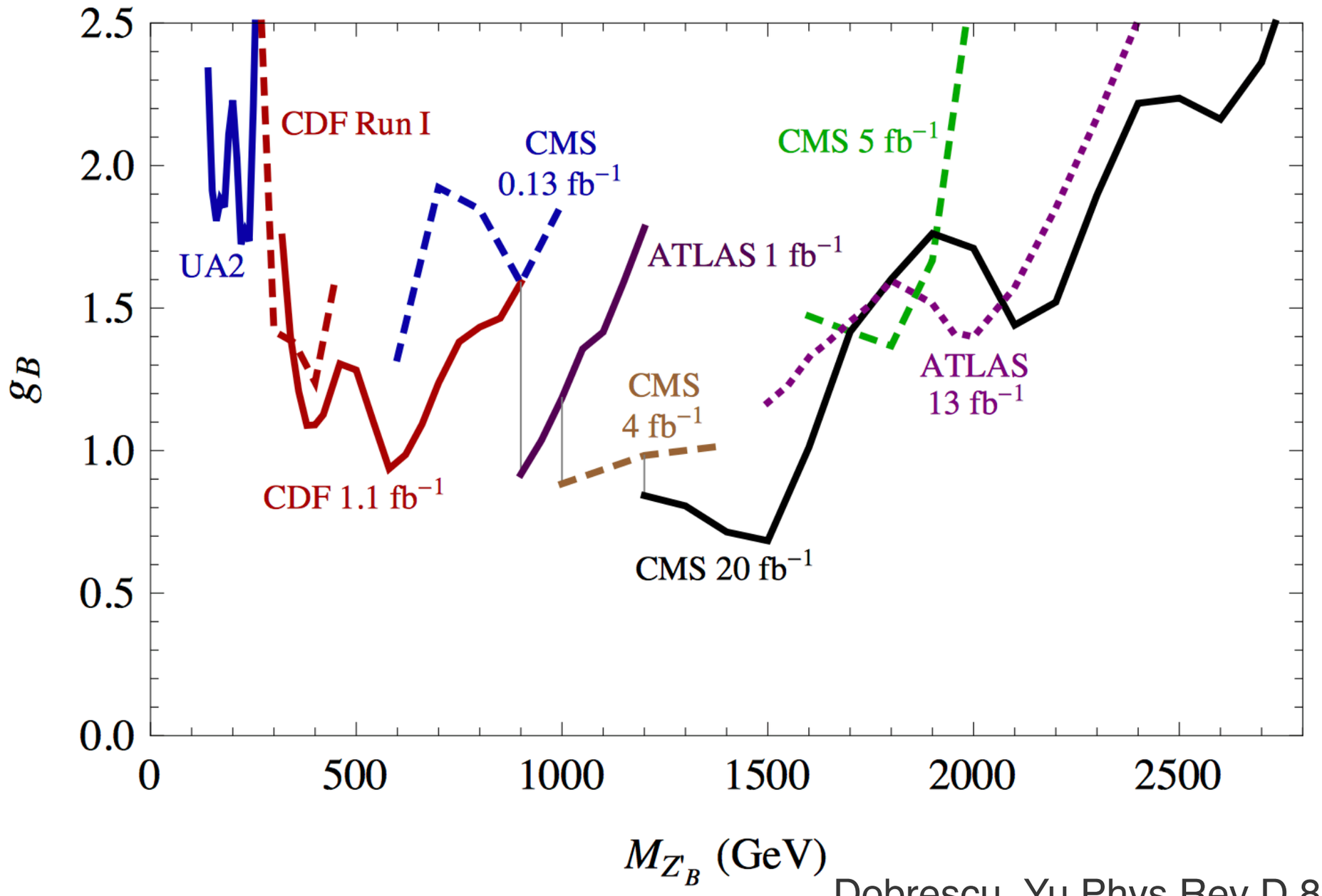


PILE-UP DEPENDENCE



TRIGGER-LEVEL ANALYSIS

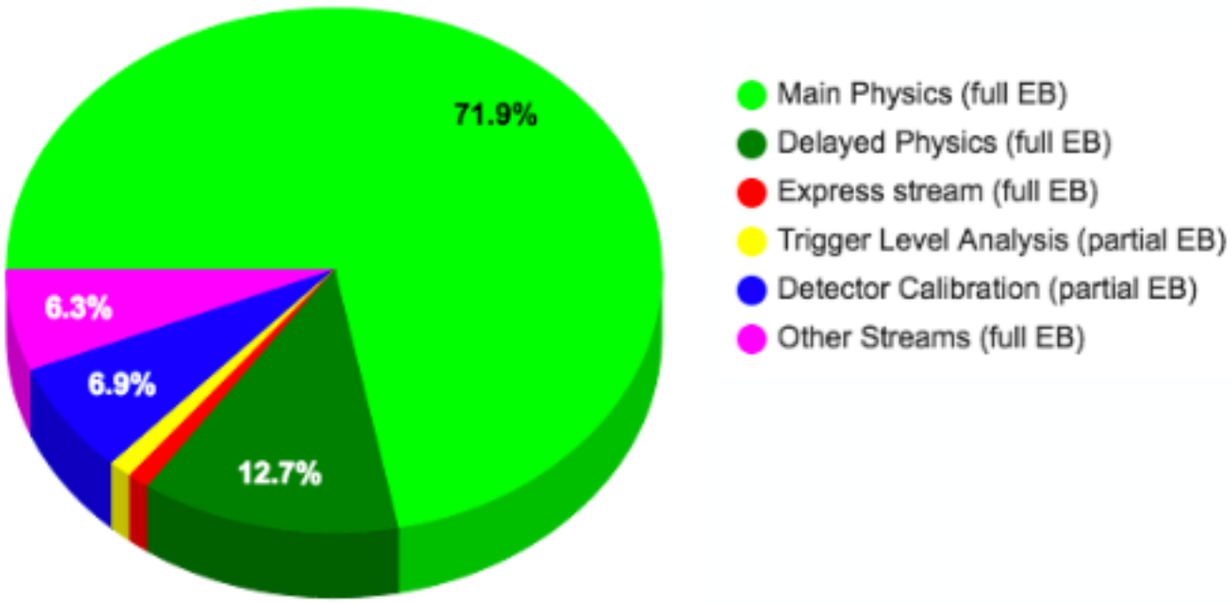
- Some searches (e.g. dijet resonances), limited by trigger prescale, applied due to readout bandwidth limitations

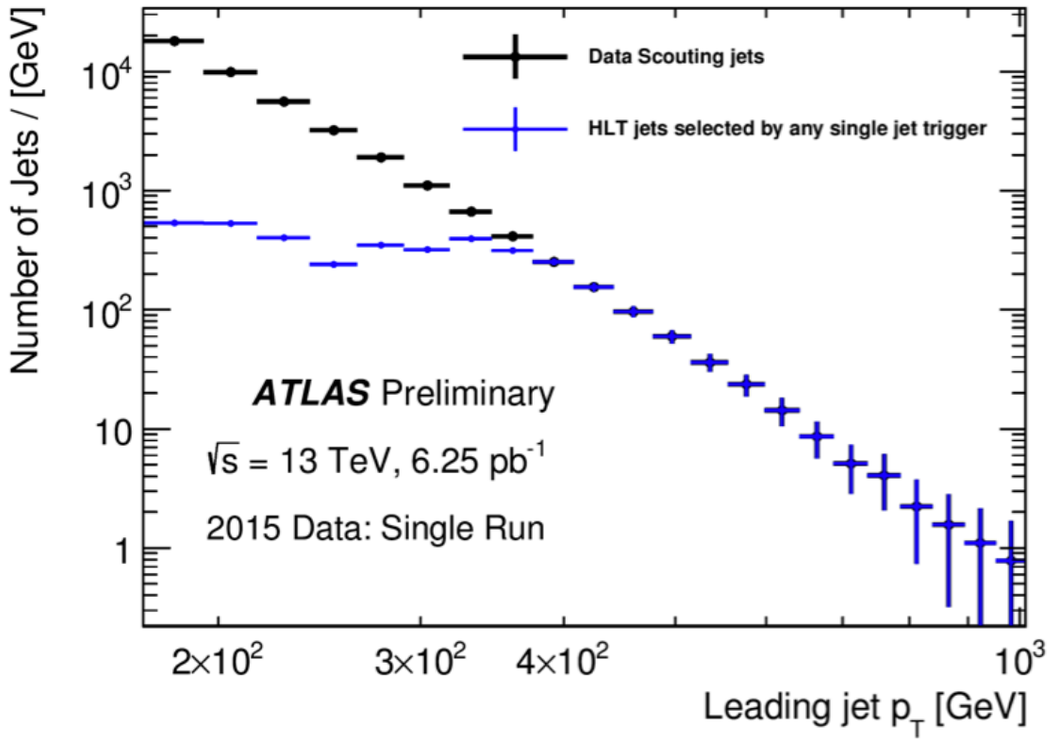


Dobrescu, Yu Phys Rev D 88 035021 (2013)

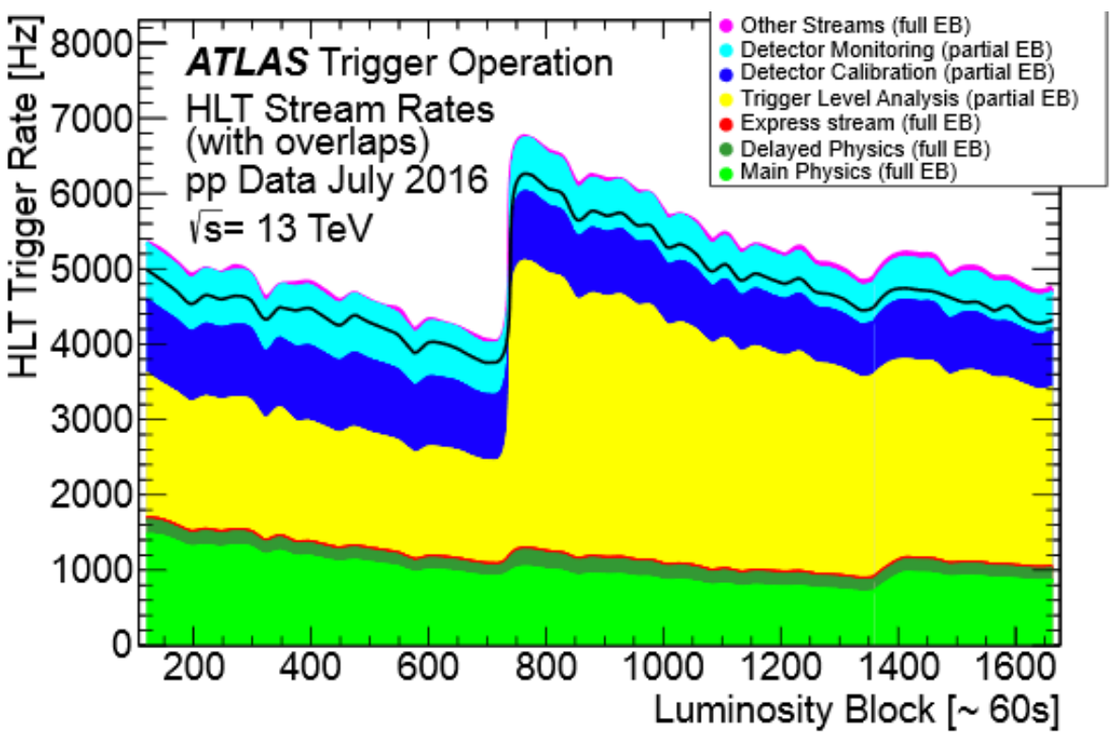
TRIGGER-LEVEL ANALYSIS

- What if we only used the data that we needed? E.g. Jets



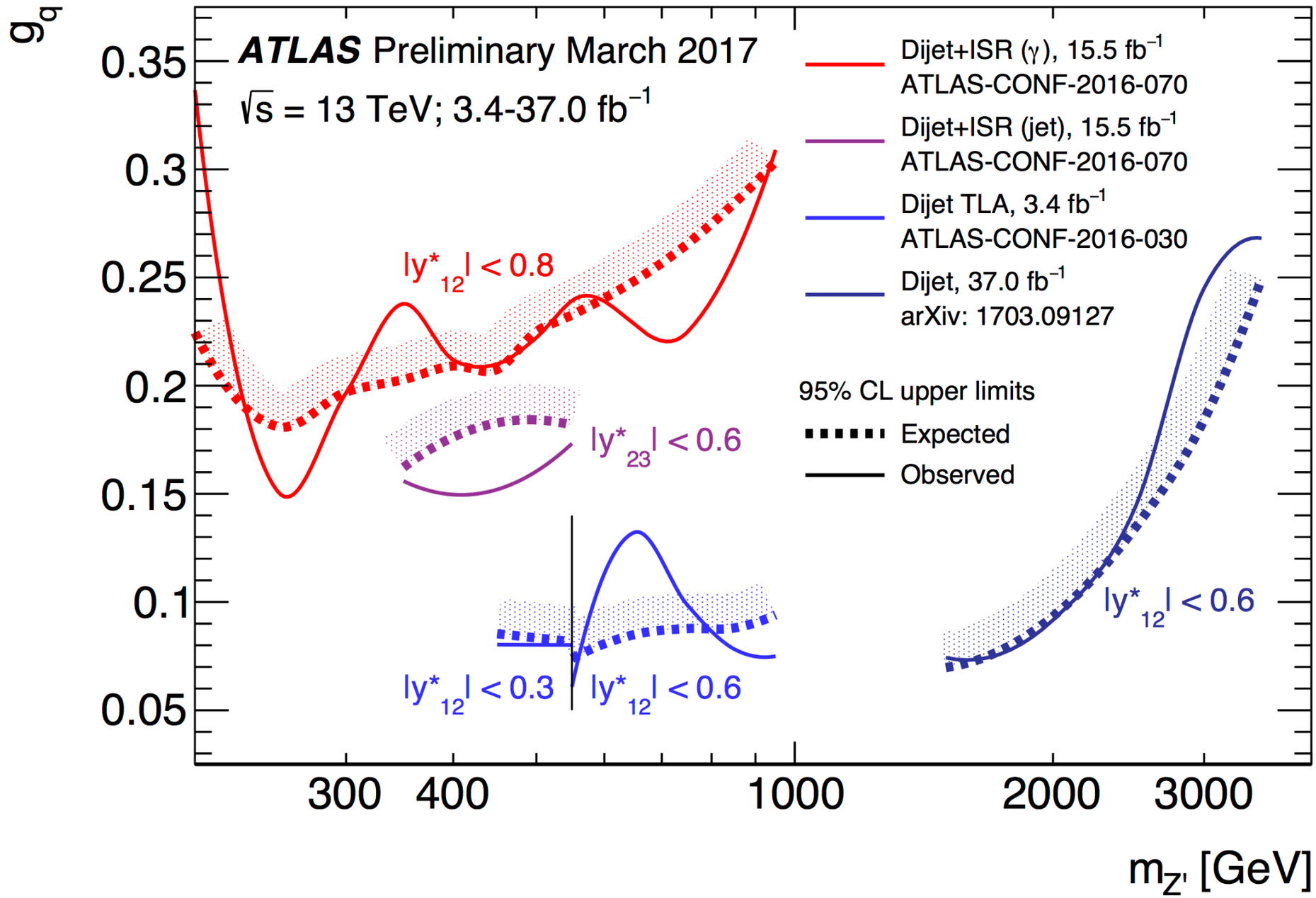


- Their are trade-offs:
  - Worse resolution, less experimental handles for understanding the data



TRIGGER-LEVEL ANALYSIS

- But the pay off can be large!



DATA PARKING

- Another fundamental limitation of our system is how fast our **offline** farms can process data.

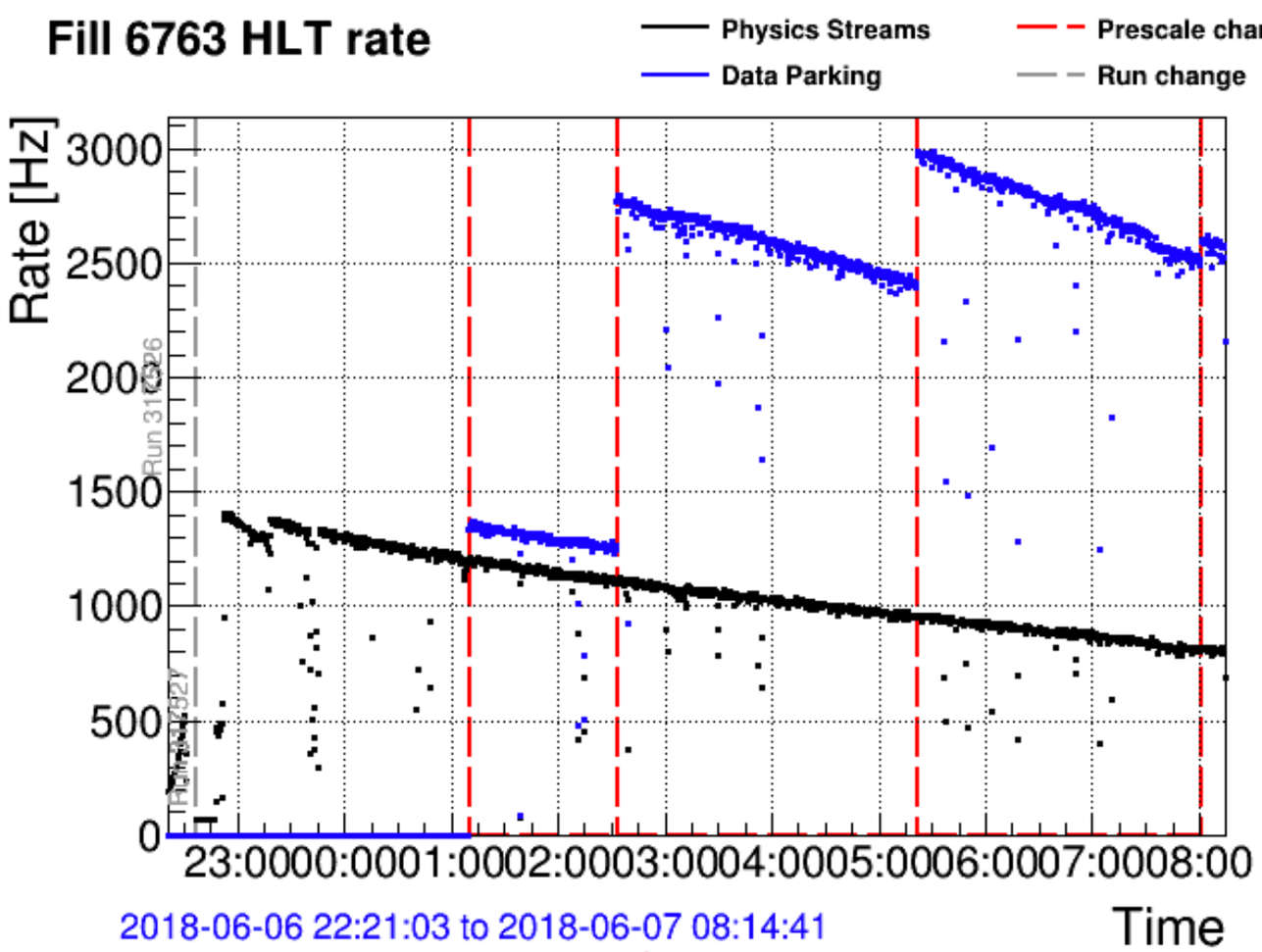
- CMS introduced data parking, or delayed processing, to store data for processing later, during downtimes: hadronic processes, B-physics are primary consumers

Trigger Selection for Data Parking	Main Physics Motivation	Average Rate (Hz) over typical LHC fill	Tighter / complementary version in the "core" trigger menu
M_{jj}>650 GeV , $\|\Delta\eta_{jj}\|$>3.5	Generic final state produced via Vector Boson Fusion (VBF)	130	QuadJet75_55_38_20: 1 b-jet + 2 "VBF" jets
At least 4 jets with p_T>50 GeV (QuadJet50)	Pair production of stops → top (hadronic decay) + neutralino in models with small mass splitting between stop and neutralino	75	QuadJet60 + DiJet20 OR QuadJet70
R^2*M_R>45 GeV + R^2>0.09	Extend SUSY hadronic searches with "razor" variables (M_R,R^2): compressed mass spectra and light stop searches	20	R^2*M_R>55 GeV + R^2>0.09 + M_R>150 GeV

DATA PARKING

- Another fundamental limitation of our system is how fast our **offline** farms can process data.

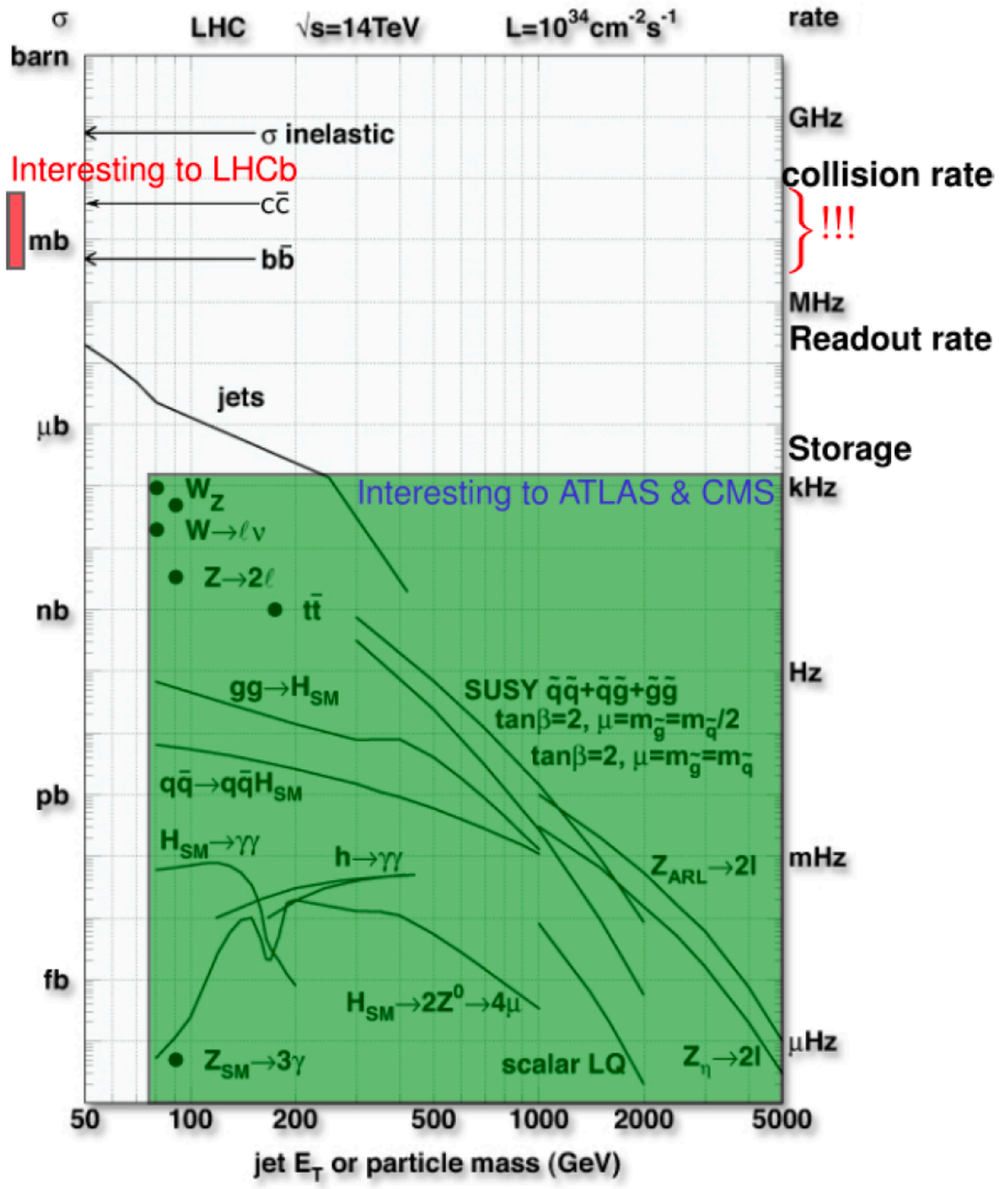
- CMS introduced data parking, or delayed processing, to store data for processing later, during downtimes: hadronic processes, B-physics are primary consumers



LOOKING TO THE FUTURE

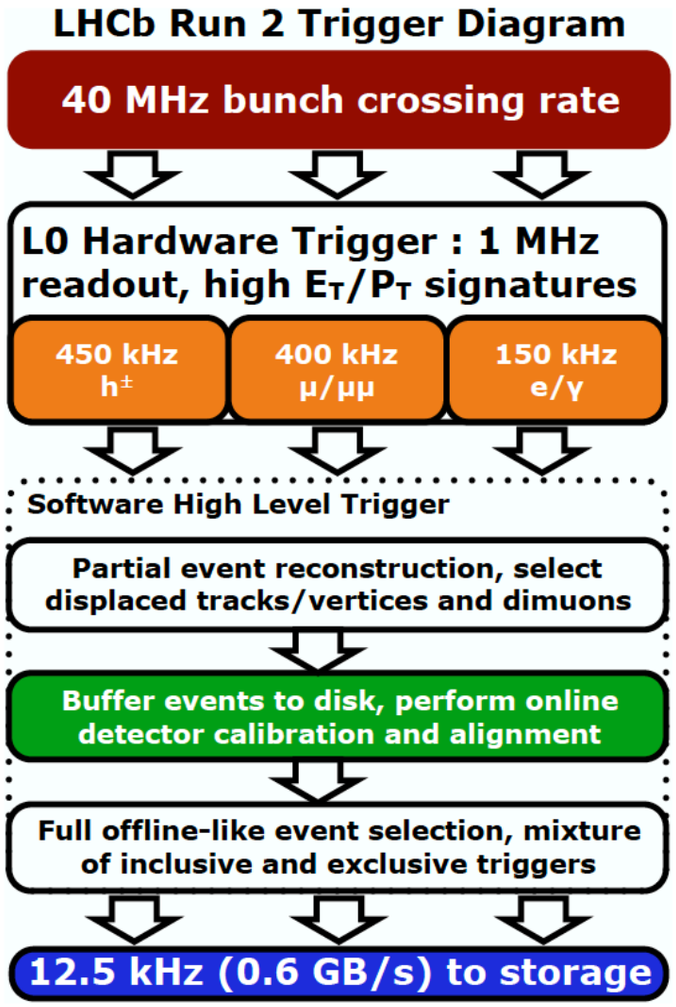
LHCB: THE TRIGGERLESS FUTURE?

- The LHCb "problem": to trigger in a signal rich environment with ***high efficiency for rare*** processes and ***high purity for high rate*** processes

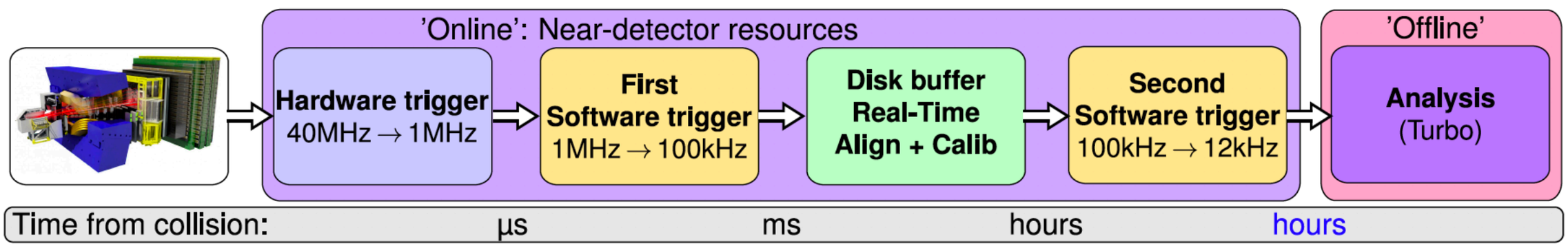


- Details: see this super nice talk by Conor Fitzpatrick — all these slides derive from there

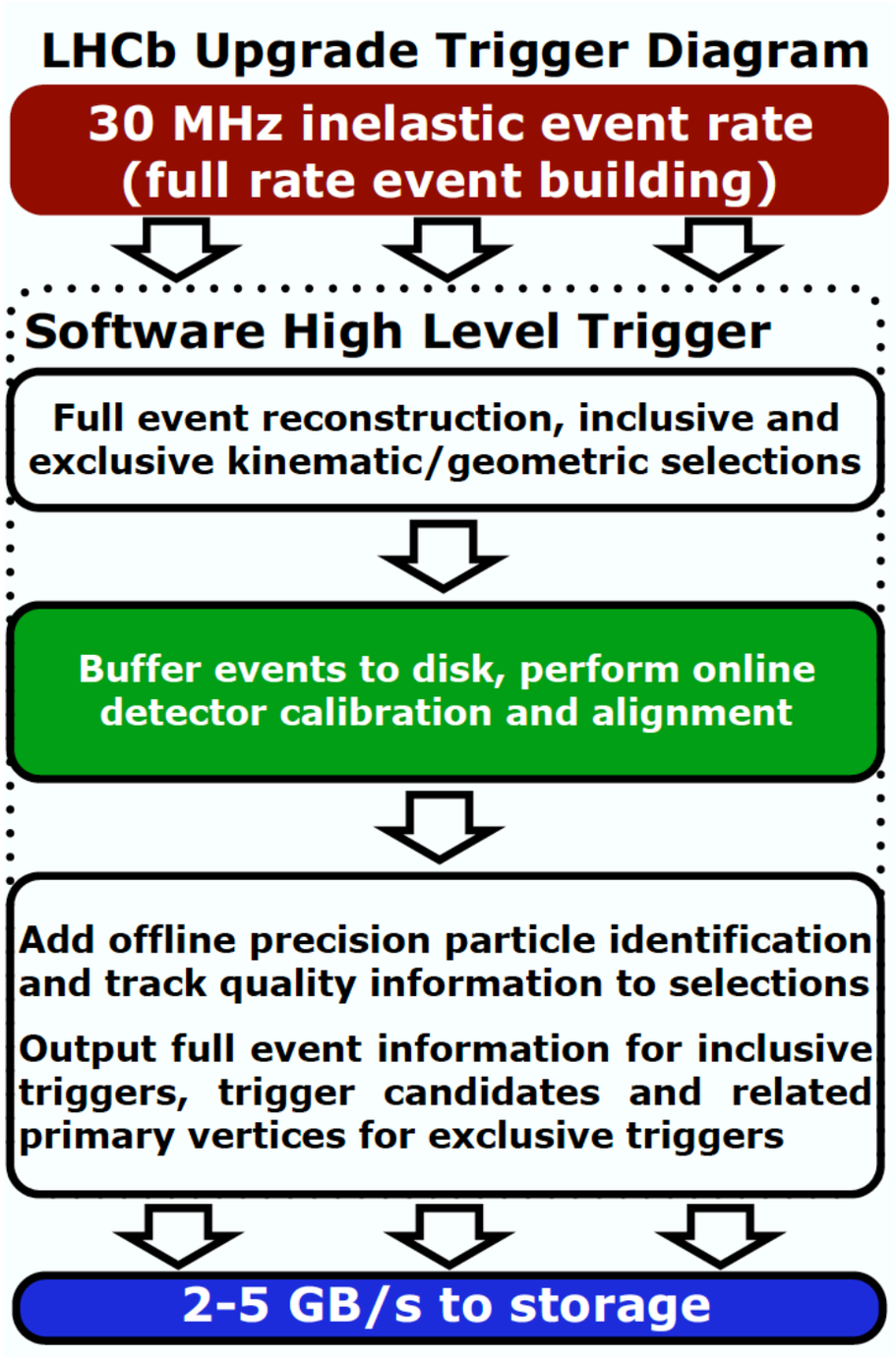
LHCB: THE TRIGGERLESS FUTURE?



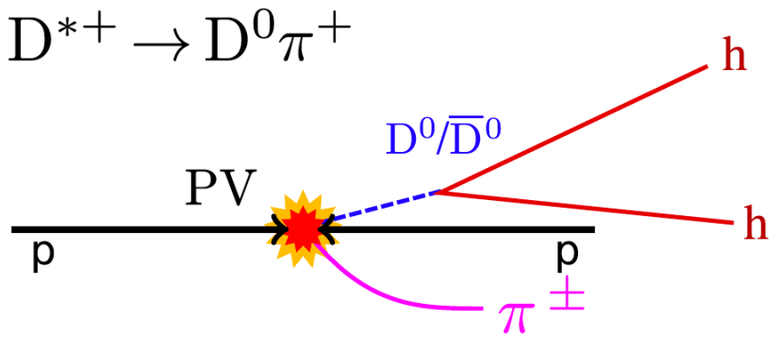
- High bandwidth readout from L1 (small events)
- Data buffered on disk for full HLT processing (~2 weeks timescale)



LHCB: THE TRIGGERLESS FUTURE?

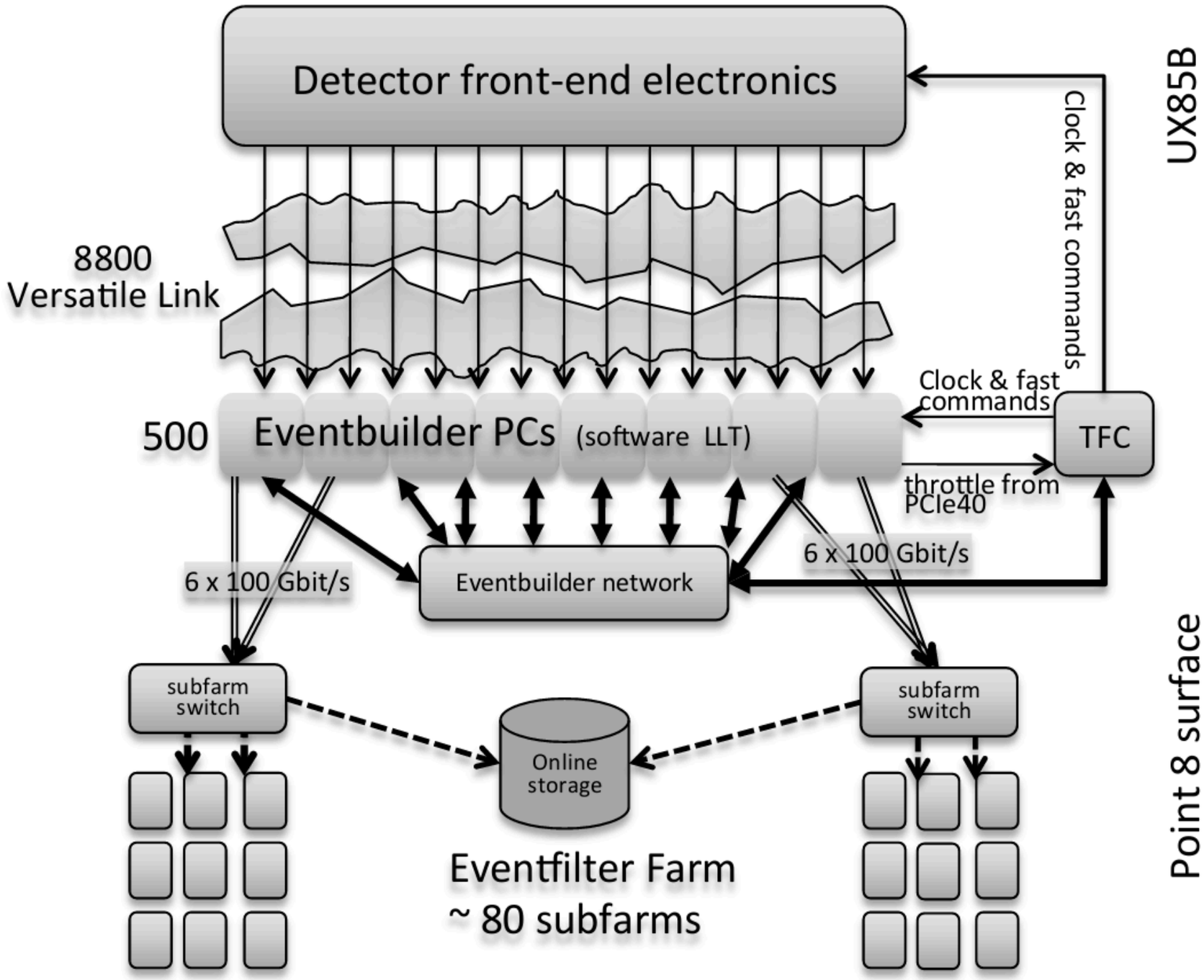


- In Run III LHCb will take 5x higher luminosity
  - Events are basically all signal
- Detector and network upgrades allow full 30MHz readout to disk in Run III (4TB/s)



- Example: Charm mixing[7]
  - Cabbibo favoured $D^0 \to K^-\pi^+$ is 300 $\times$ more abundant than DCS $D^0 \to K^+\pi^-$
  - Want to keep 100% of the 'interesting' DCS mode, but prescale the CF mode
  - Cannot be done using simple 'trigger' criteria
  - Full reconstruction + Particle ID in the trigger needed to make this possible

LHCB: THE TRIGGERLESS FUTURE?

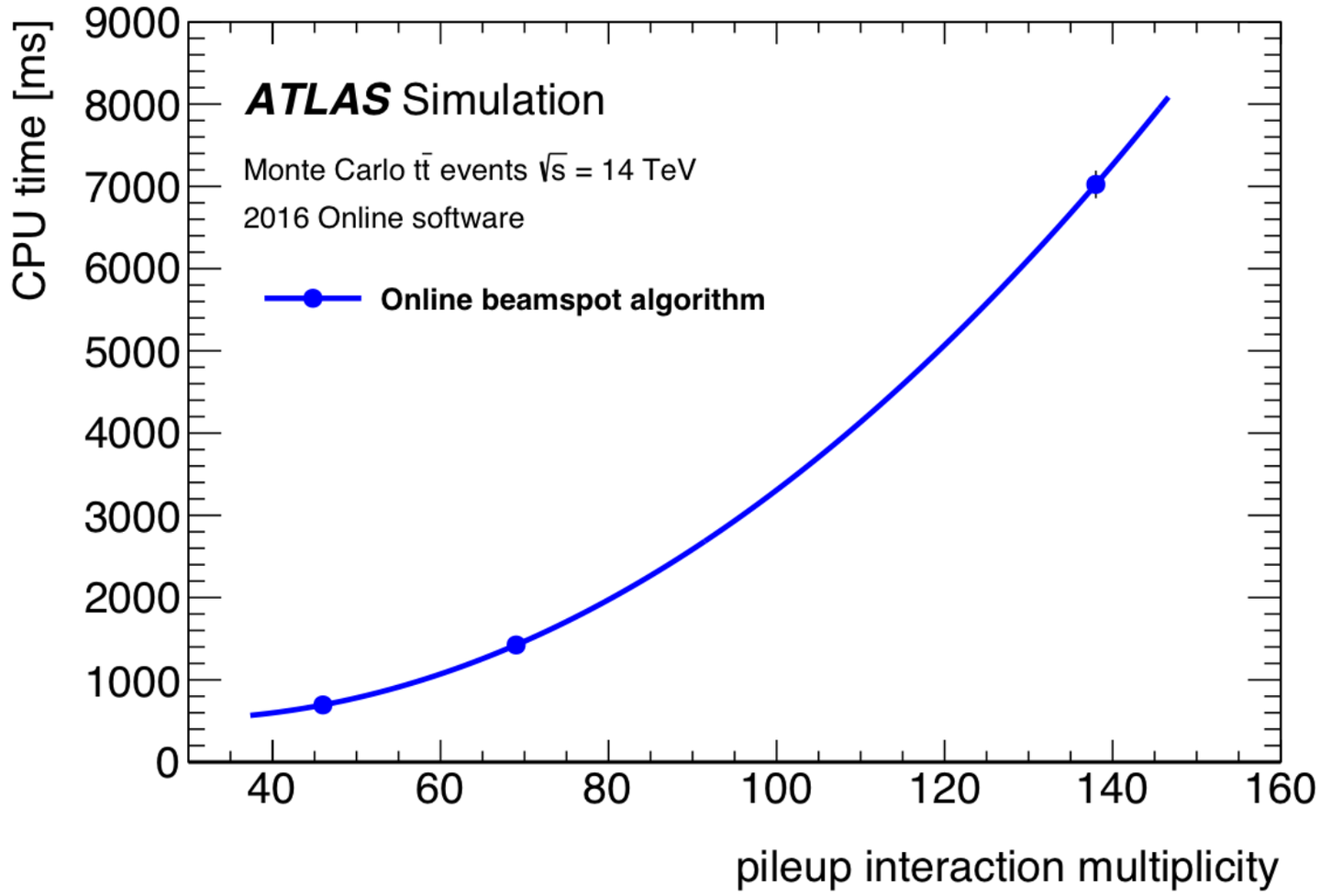


WHY IS THIS NOT POSSIBLE FOR ATLAS & CMS?

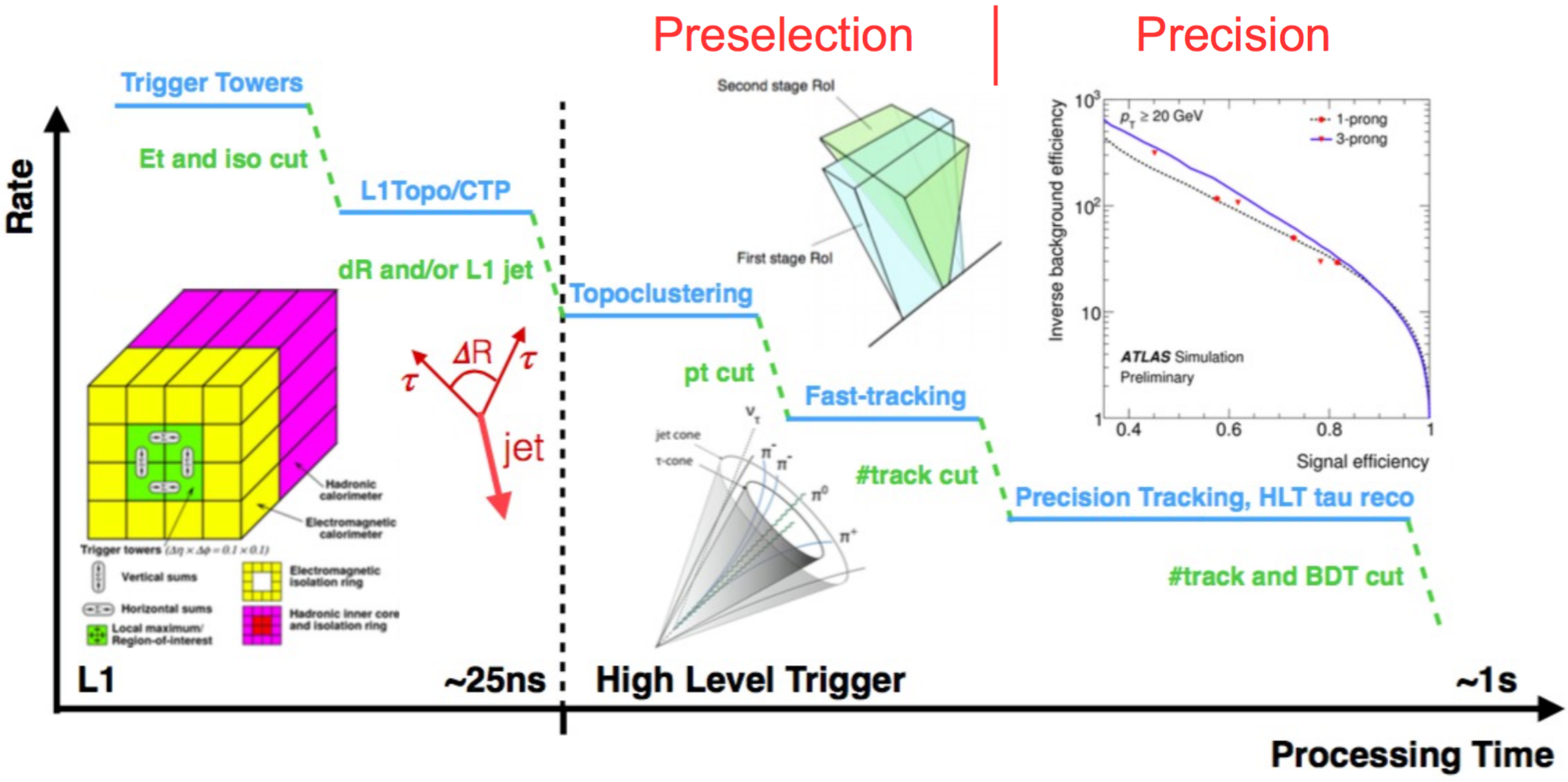
- Detector readout bandwidths still limited:
  - 40 TB/s is too much data to record — power, cooling, etc for transmission would be a problem!
- ATLAS & CMS are not signal rich environments:
  - We really don’t want most of the data and these giant networks are expensive!
- But, due to the flexibility and ability to emulate offline reconstruction, expect more and more reliance on SW triggering/ processing

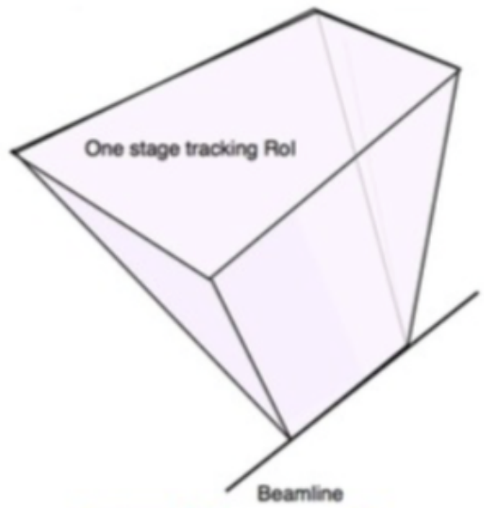
FULL DETECTOR TRACK RECONSTRUCTION

- CPU & data routing constraints limit the amount of information used from tracking in HLT



EXAMPLE USES: TAUS



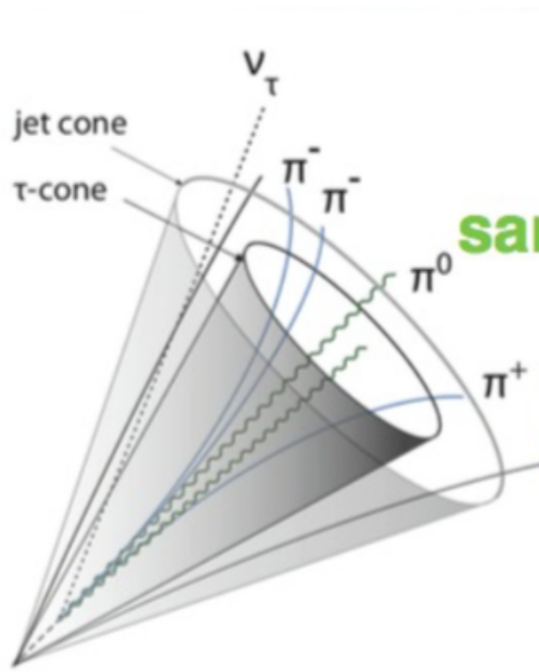


Rate

FTK tracks and vertex

Topoclustering

#track cut



same vertex

pt cut (with 1p/3p TES*)

Precision Tracking, HLT tau reco*

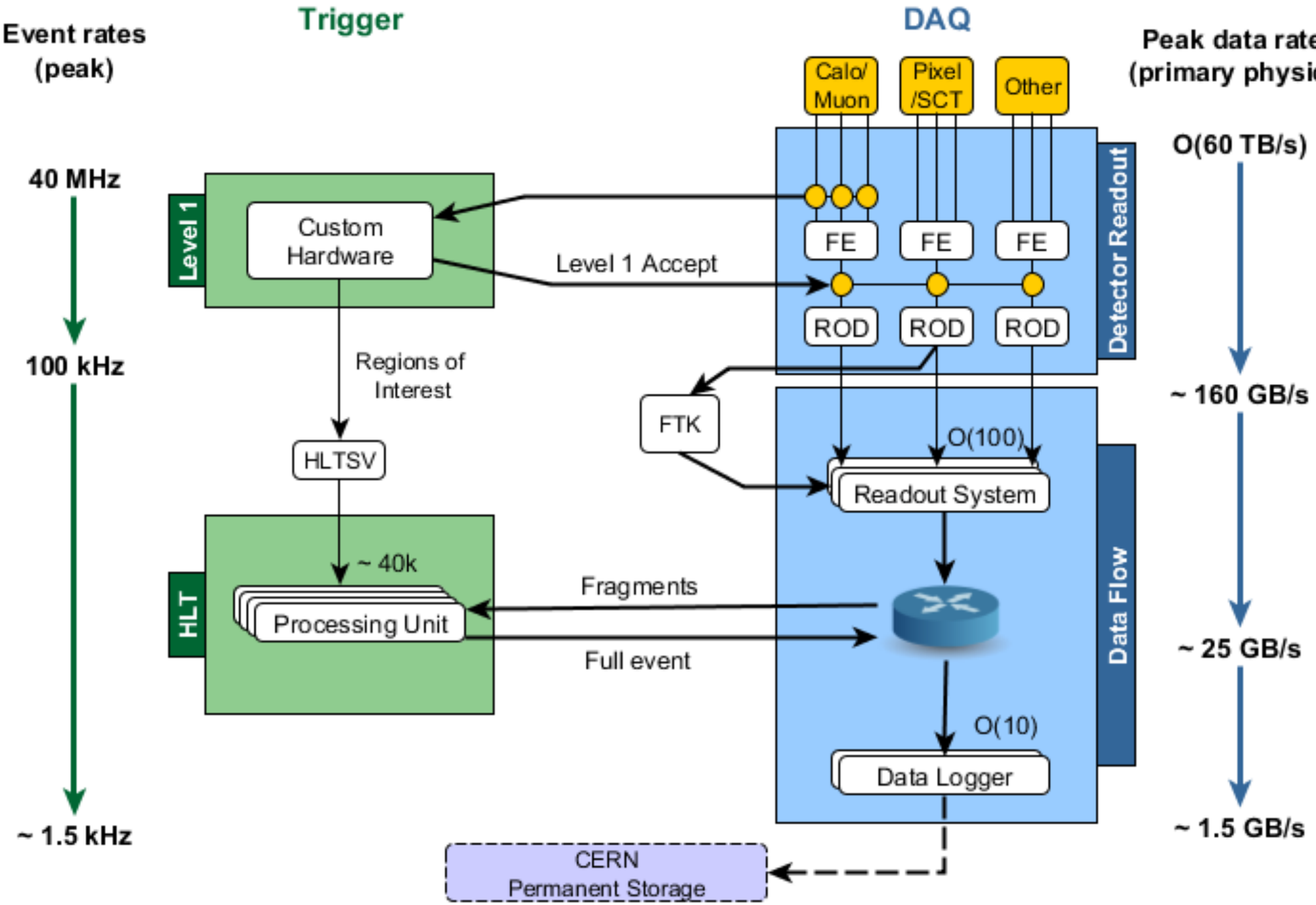
#track and BDT cut

High Level Trigger

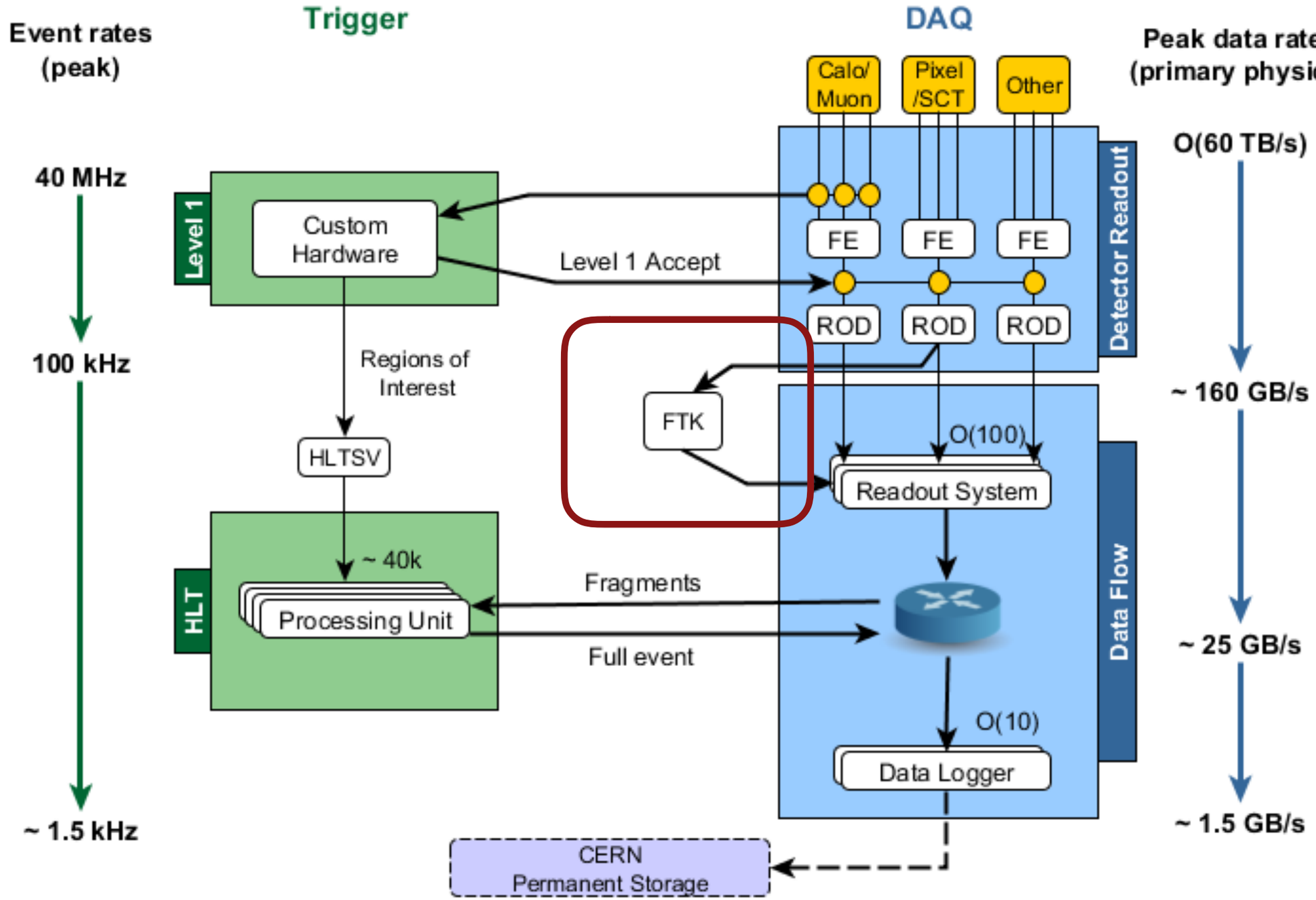
~1s

Processing Time

HARDWARE BASED TRACK FINDERS



HARDWARE BASED TRACK FINDERS



HARDWARE BASED TRACK FINDERS

- Use fast algorithms in hardware to reconstruct charged particles

- Divide detector into slices

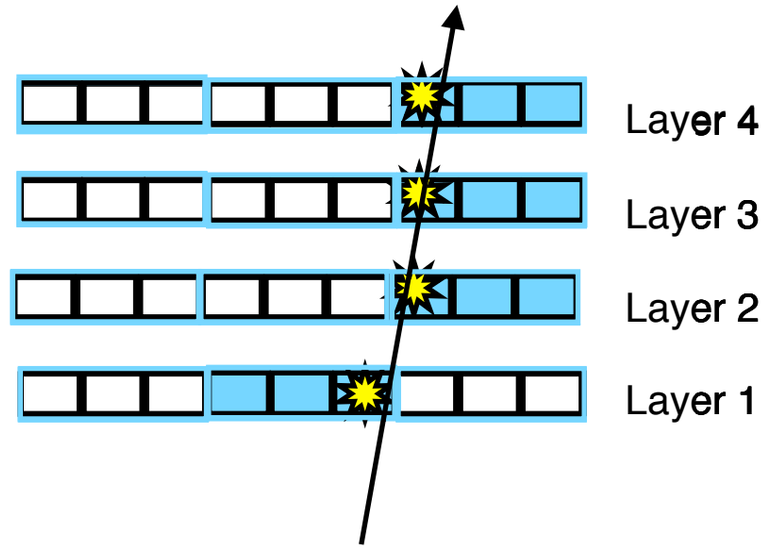
- Play bingo with the hits!

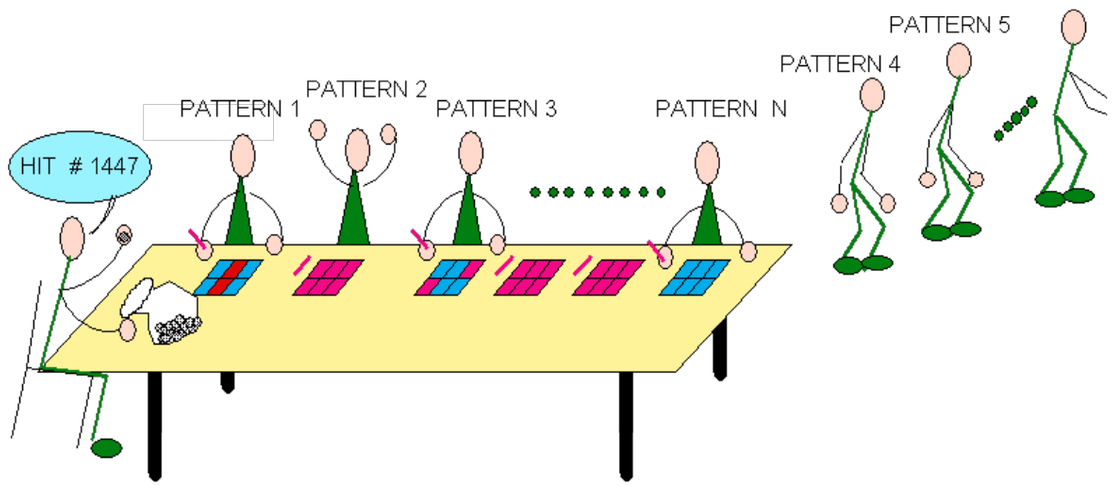
  - 1B simultaneous comparisons

  - 1 track fit / 5ps

HARDWARE BASED TRACK FINDERS

- Use fast algorithms in hardware to reconstruct charged particles
- Divide detector into slices
- Play bingo with the hits!
  - 1B simultaneous comparisons
  - 1 track fit / 5ps





HARDWARE BASED TRACK FINDERS

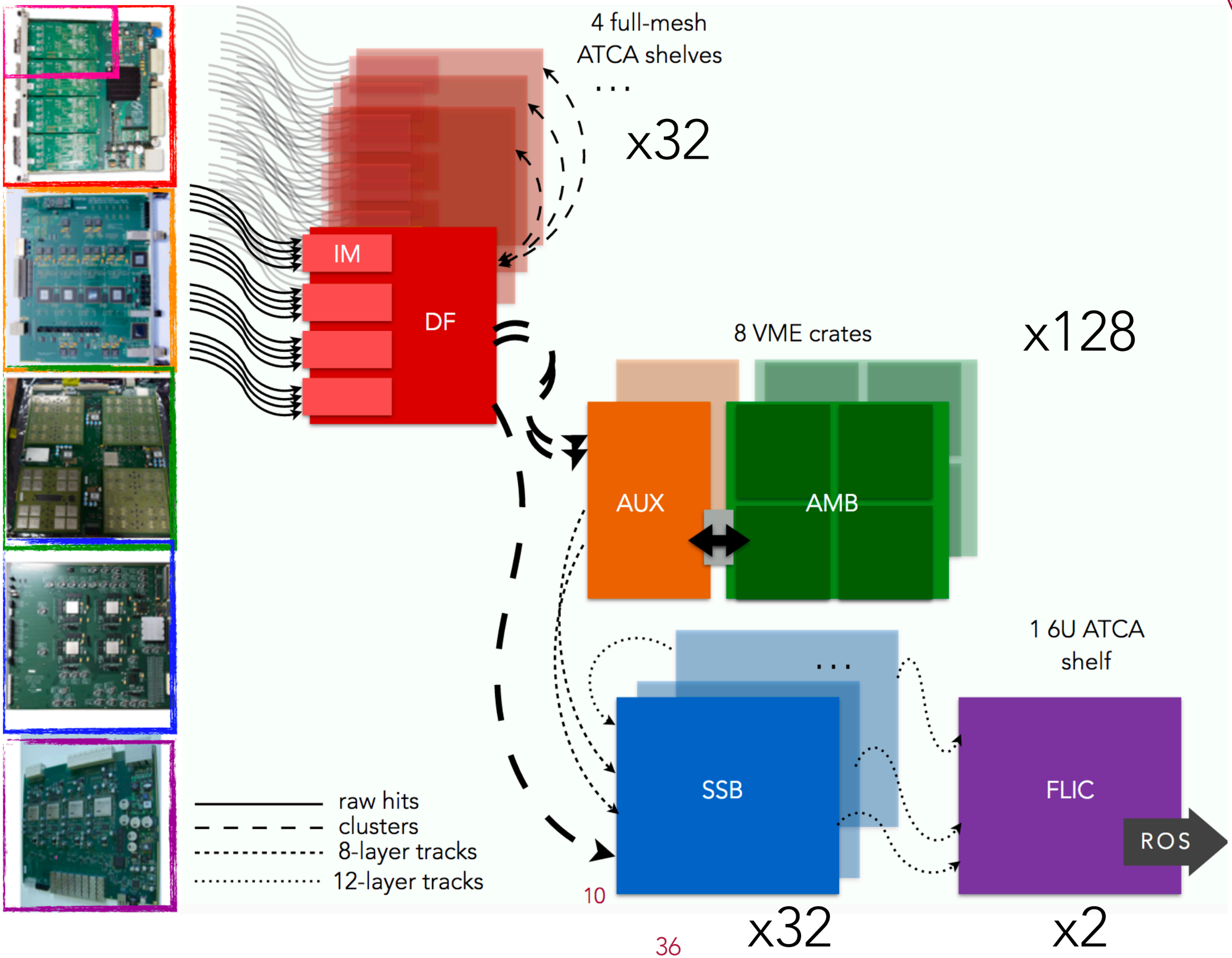
- Use fast algorithms in hardware to reconstruct charged particles

- Divide detector into slices

- Play bingo with the hits!

  - 1B simultaneous comparisons

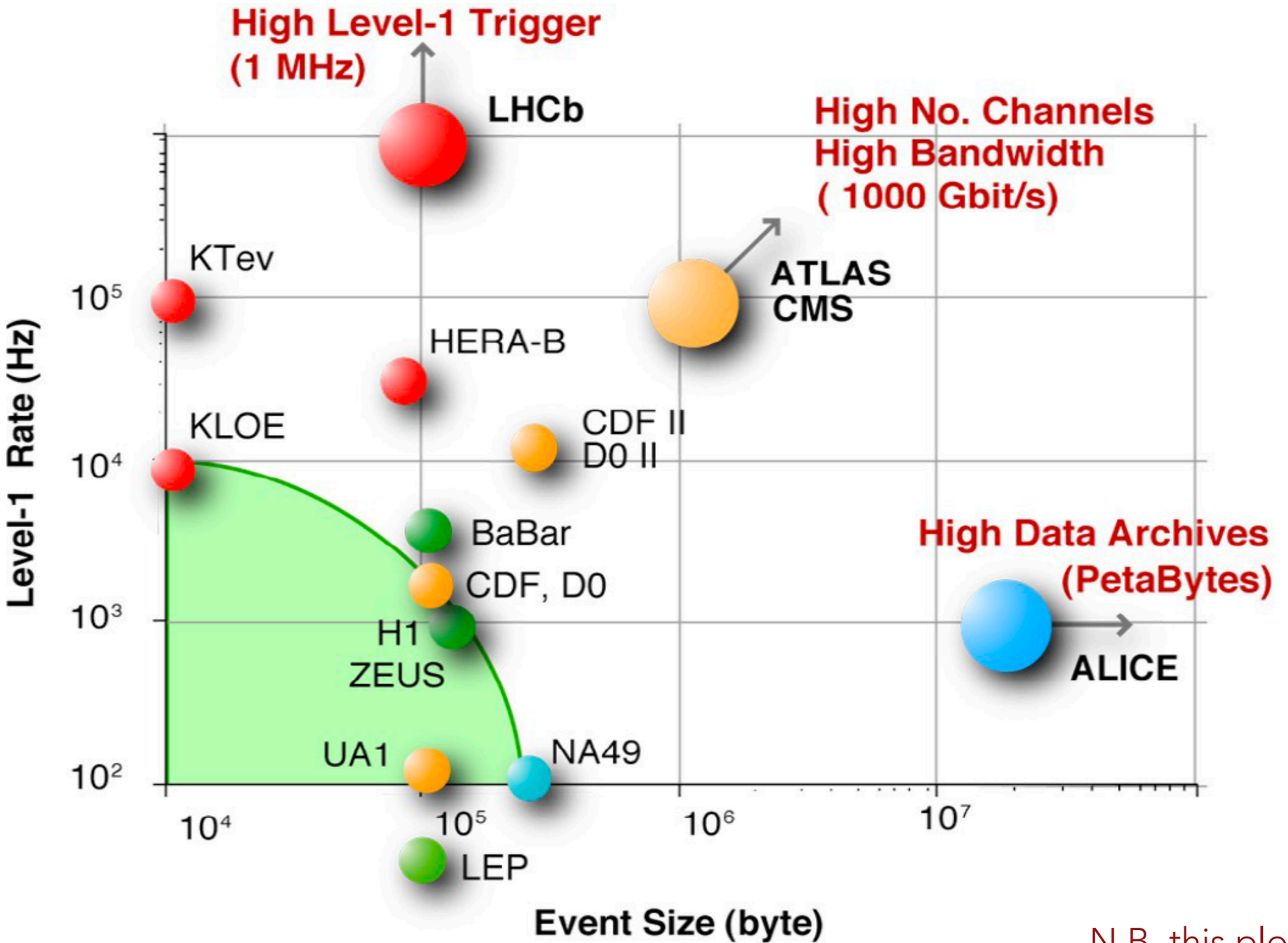
  - 1 track fit / 5ps


4 full-mesh
ATCA shelves
...
x32
IM
DF
8 VME crates
x128
AUX
AMB
1 6U ATCA
shelf
...
SSB
FLIC
ROS
raw hits
clusters
8-layer tracks
12-layer tracks
10
x32
x2

TRIGGER & DAQ INNOVATIONS FOR HL-LHC AND ELSEWHERE

- Track triggers for ATLAS & CMS at Level 1
- Machine learning in the first-level trigger
- Current GPU processing for tracking in ALICE
- Many more — check the Phase II TDRs!

SUMMARY: THE TDAQ PHASE SPACE



N.B. this plot shows up everywhere I can I can't find a reference for it….beware.

SUMMARY

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)

- A high performing system optimizes the various system bottlenecks for the physics that we want to study

  - Really fun interplay of hardware, software, networking and algorithmic development!

- Attend the ISOTDAQ or EDIT schools to learn more! And read your experiment's detector papers and upgrade TDRs

EXTRA MATERIAL

Stanford
University

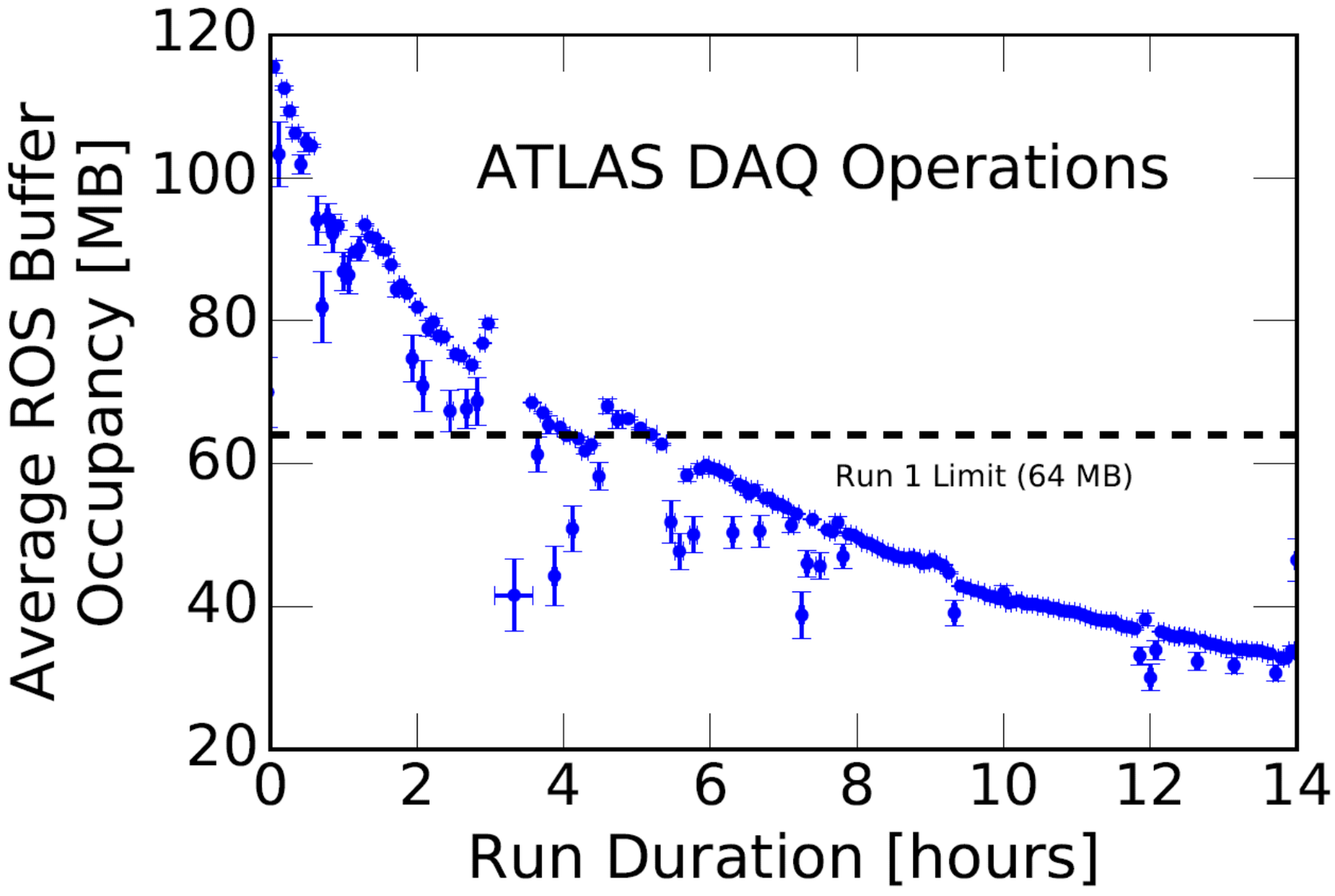
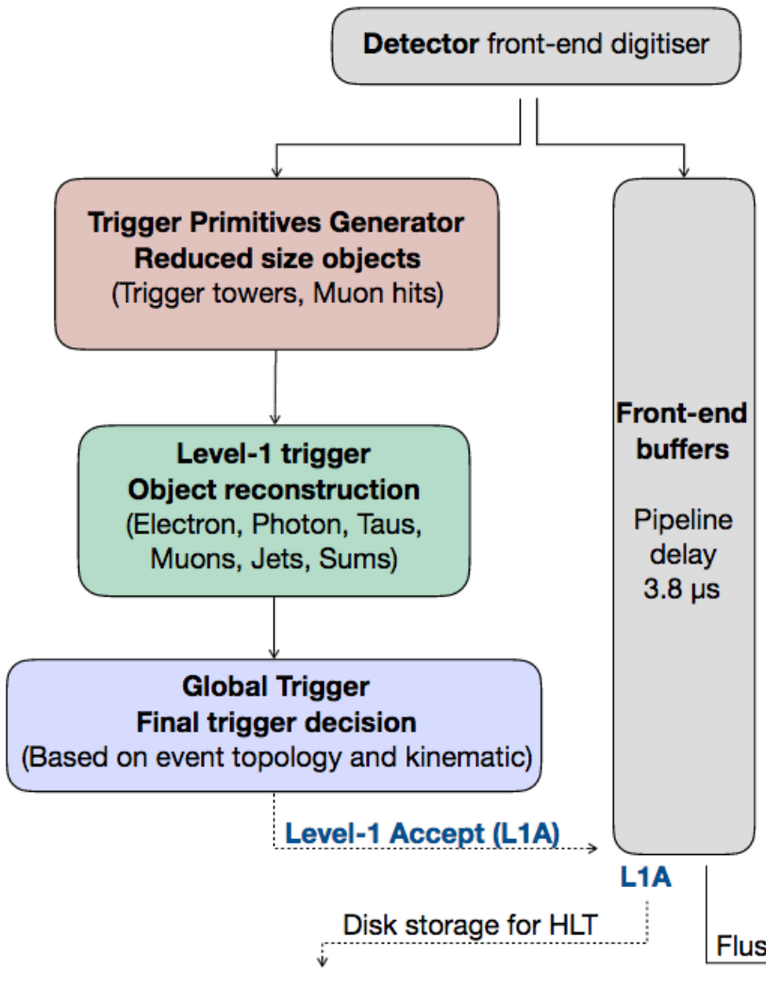

ATLAS DAQ Operations
Run 1 Limit (64 MB)
Average ROS Buffer Occupancy [MB]
Run Duration [hours]
120
100
80
60
40
20
0
2
4
6
8
10
12
14

Fig. Ref

- https://indico.cern.ch/event/659612/contributions/2836315/attachments/1593071/2521964/201802_Bortignon_TDII_PueblaMexico_31Jan_2.pdf

The CMS level-1 trigger path



- **Detector** signals duplicated at front-end
- **Front-end buffers** store full event waiting for trigger decision
- **Trigger primitive generators** produce reduced size objects
- **Level-1 processors** reconstruct **physics objects** from trigger primitives
- **Global trigger** takes **final decision** and sends it to buffers for **disk storage or flush**

9

CMS L1 TRIGGER

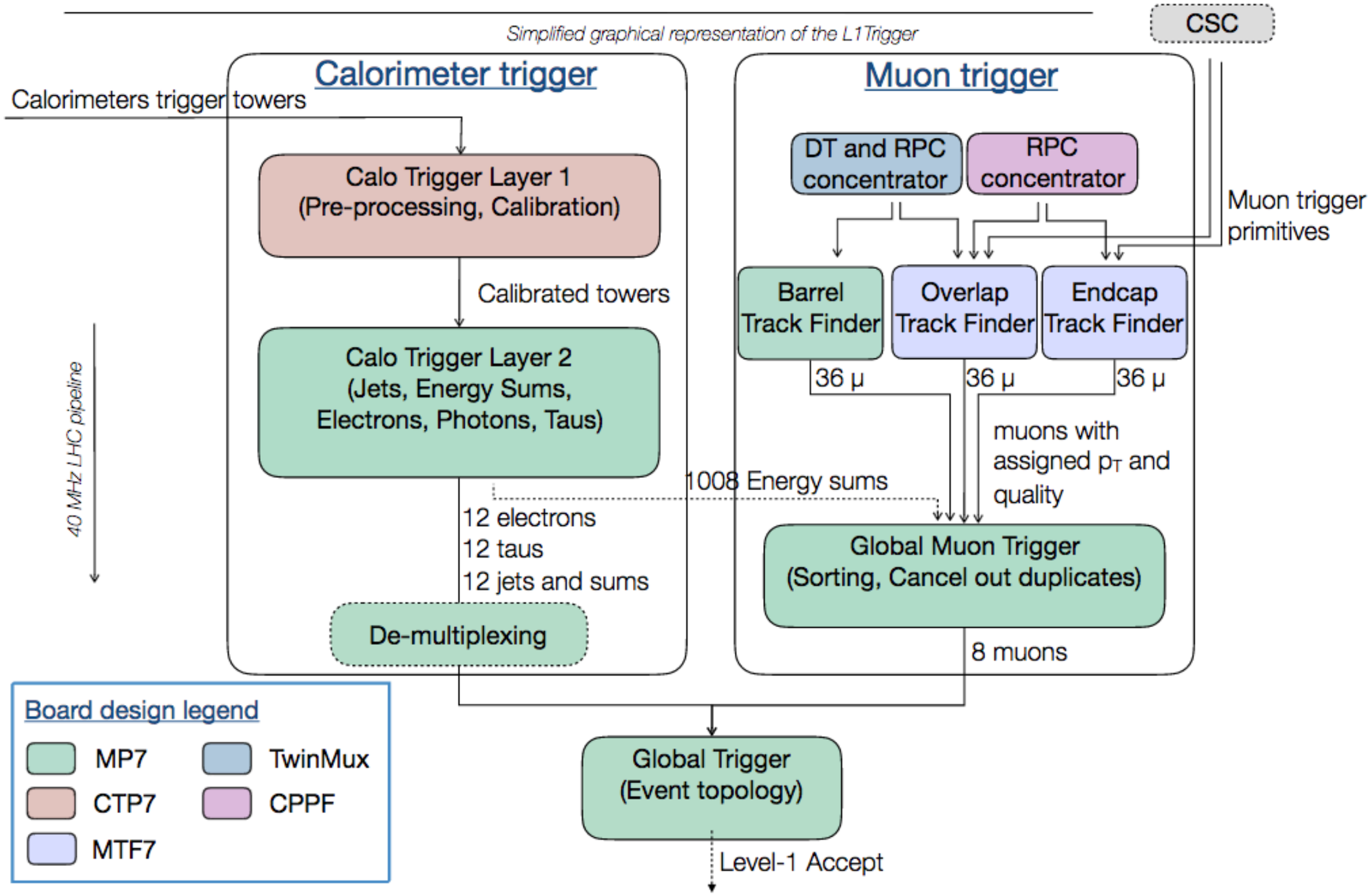
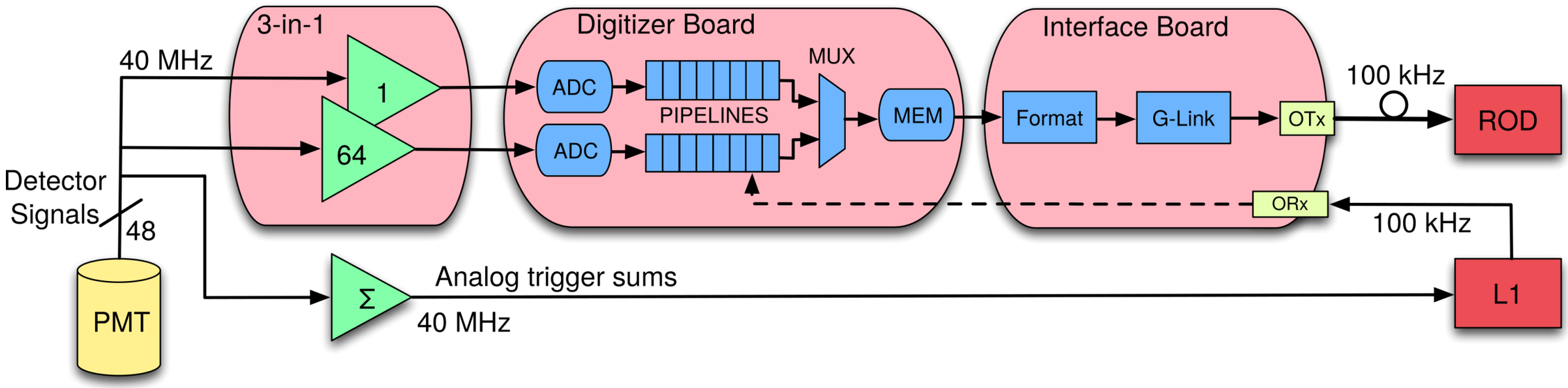


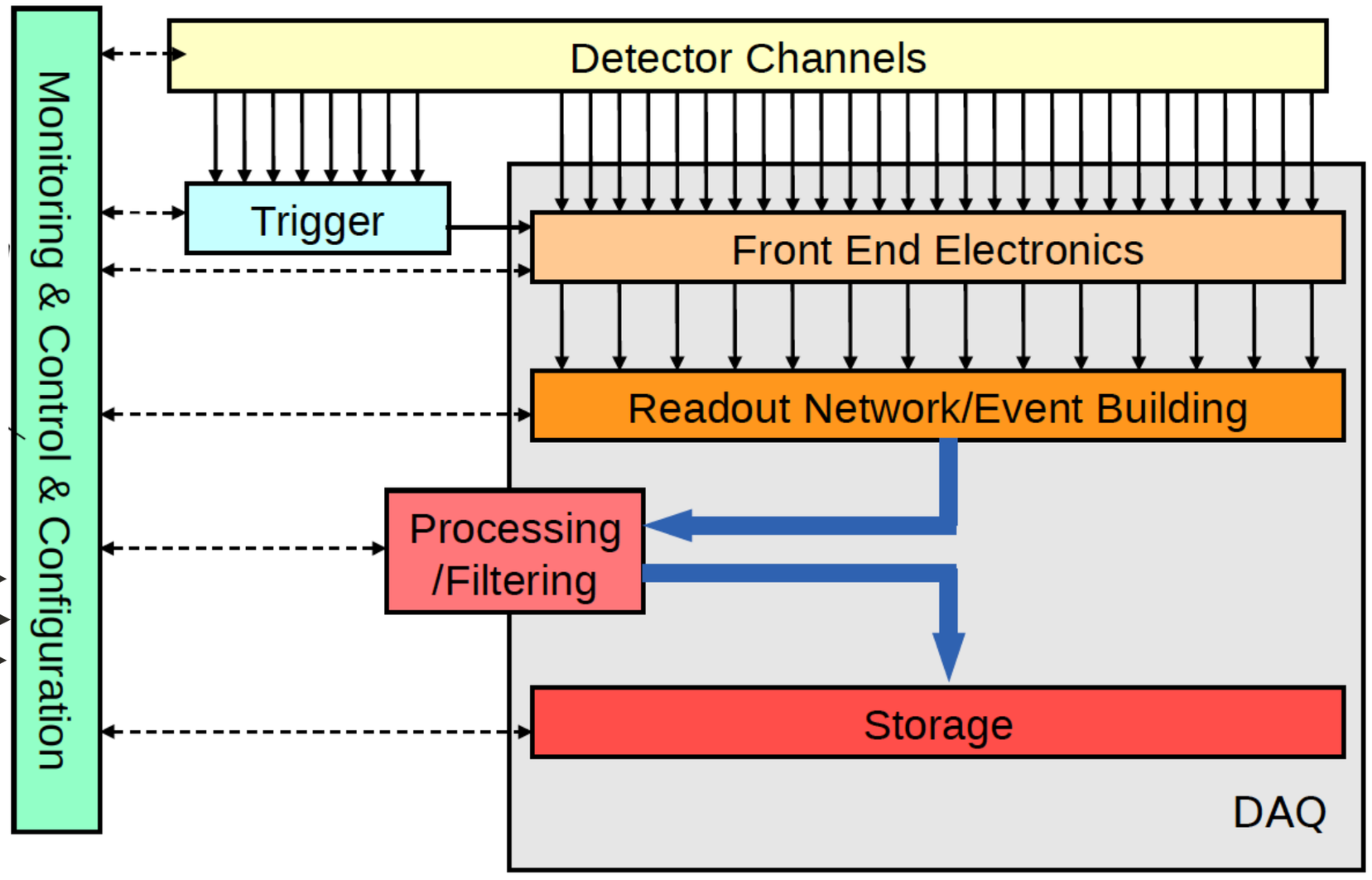
Fig. Ref

EXAMPLE:
ATLAS TILE DIGITIZER CHAIN



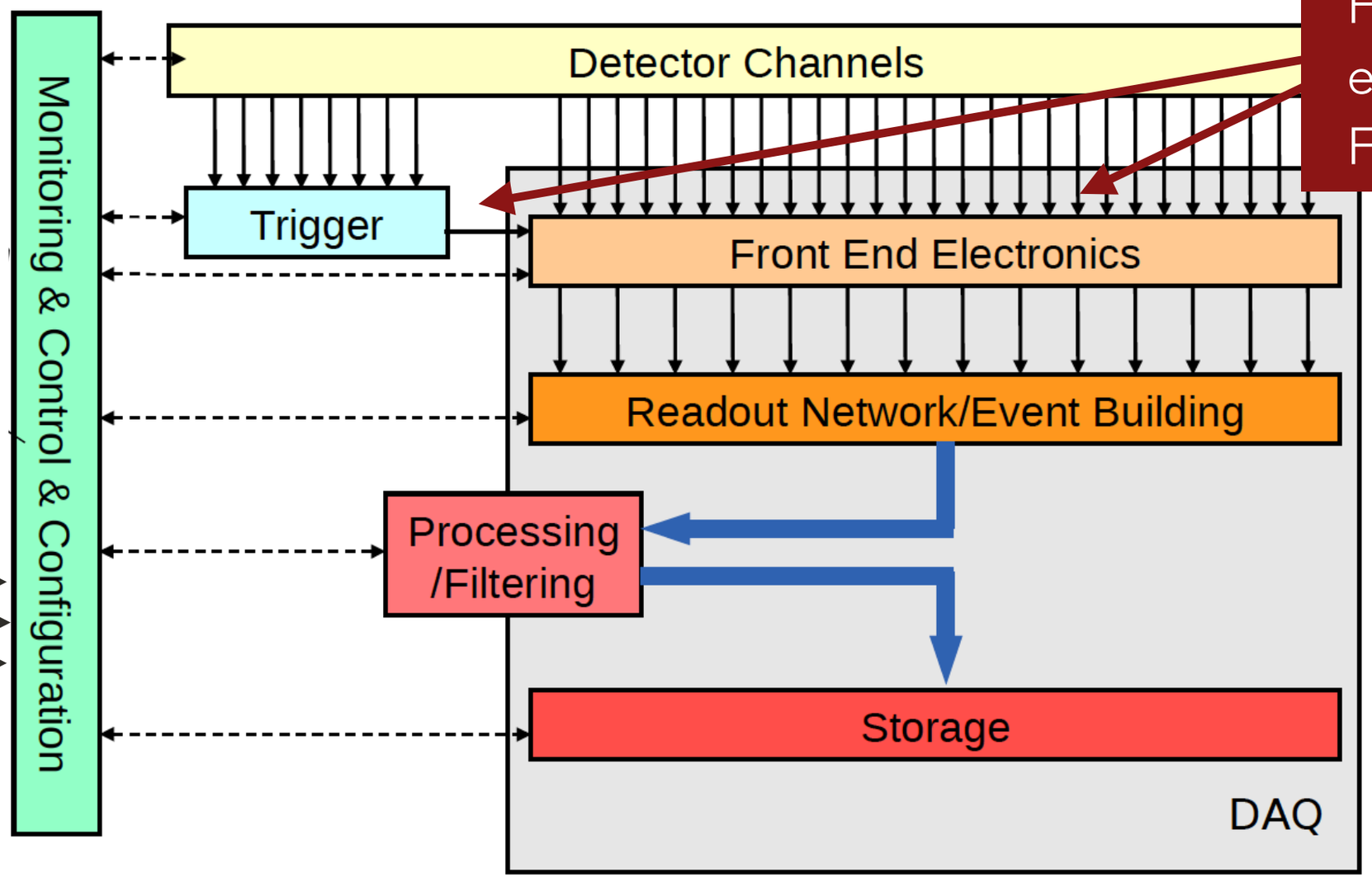
TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



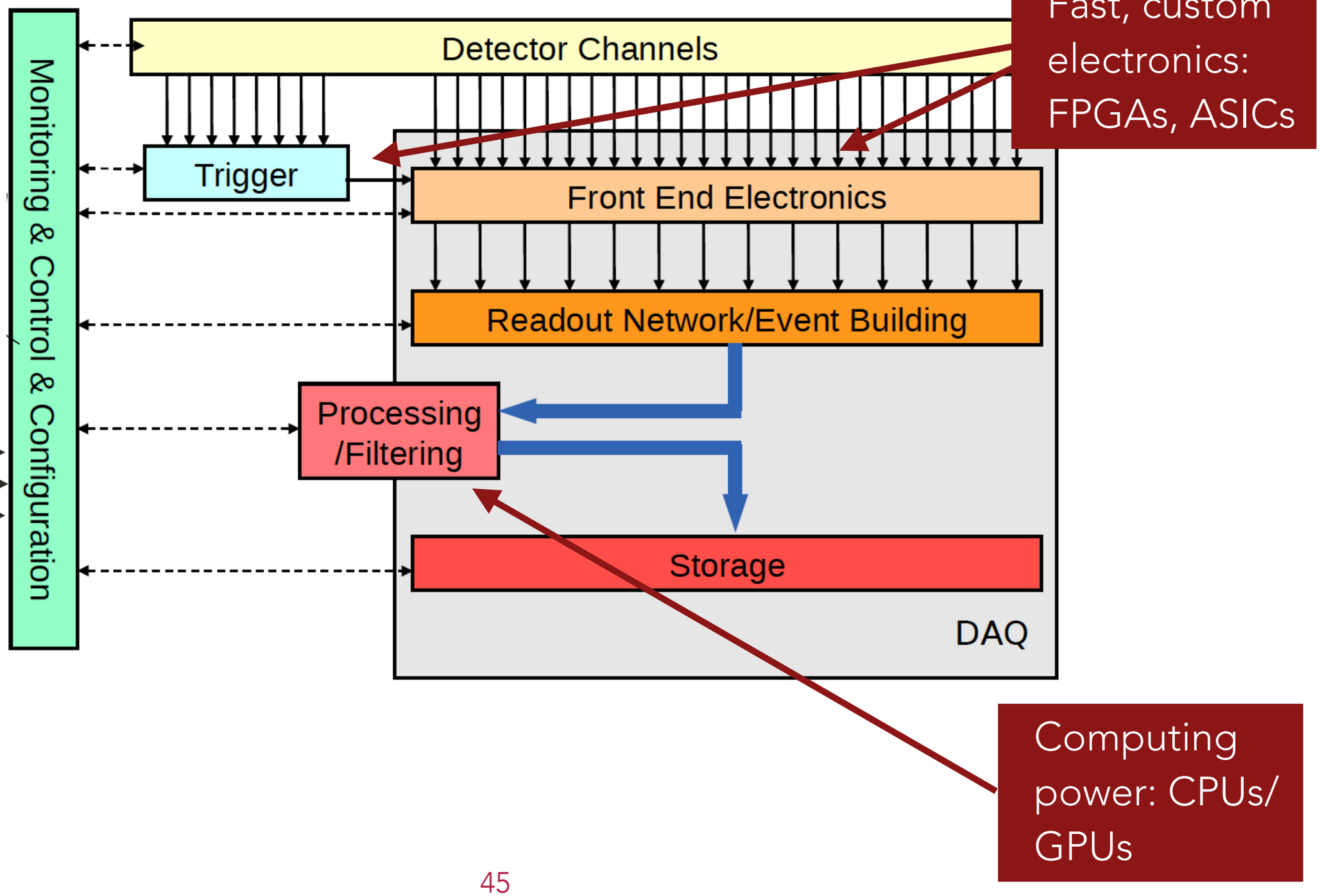
TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



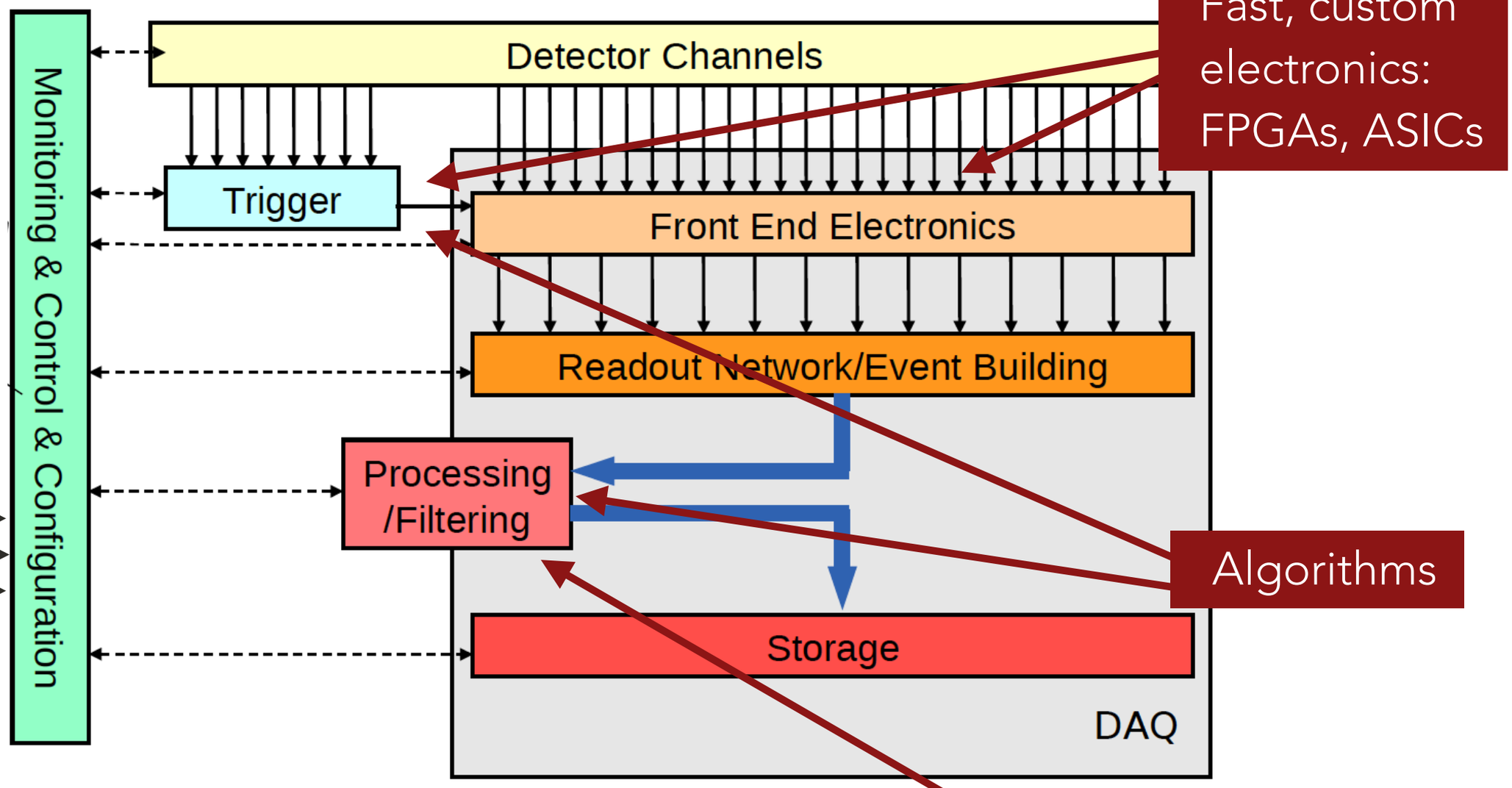
TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



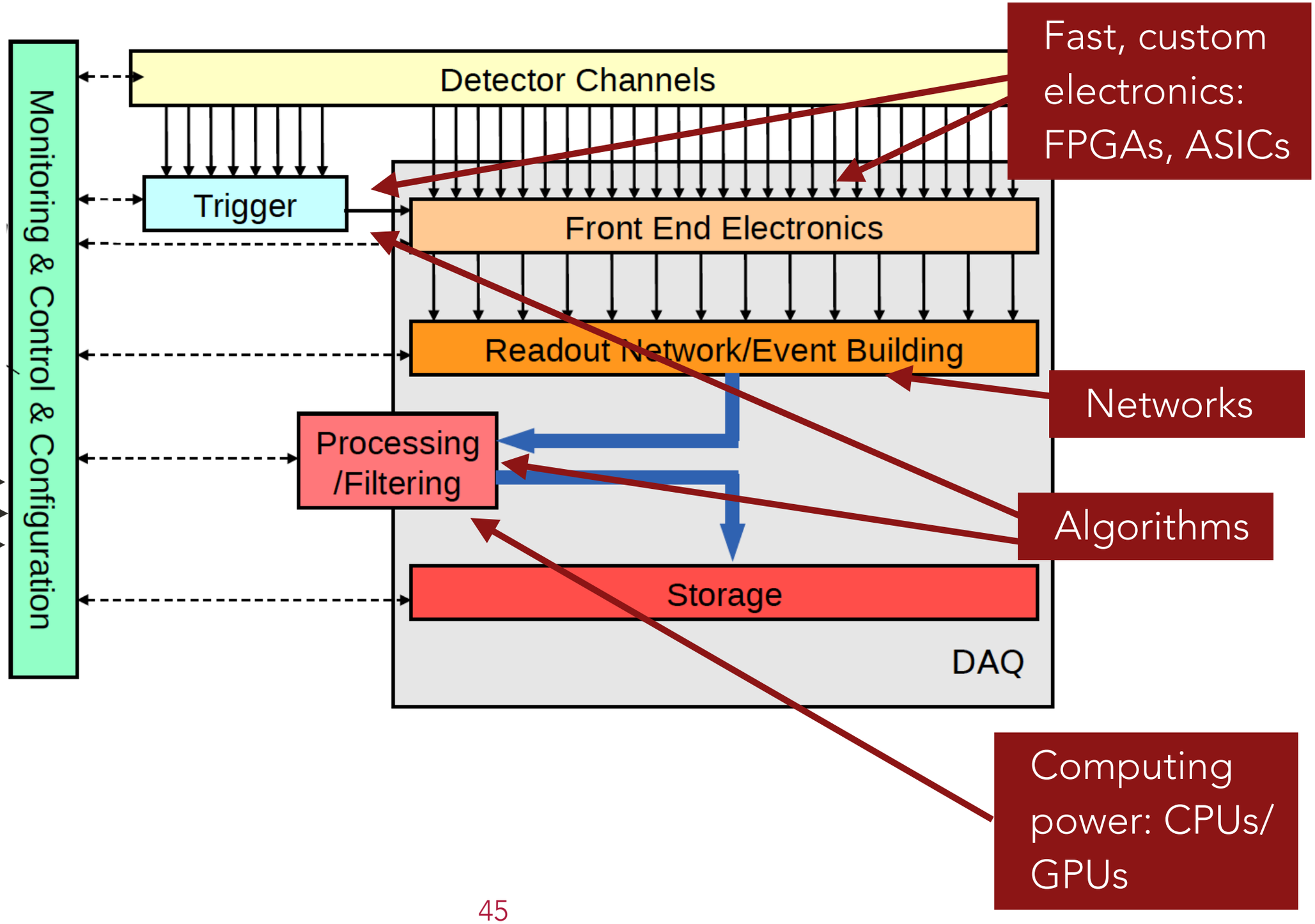
TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



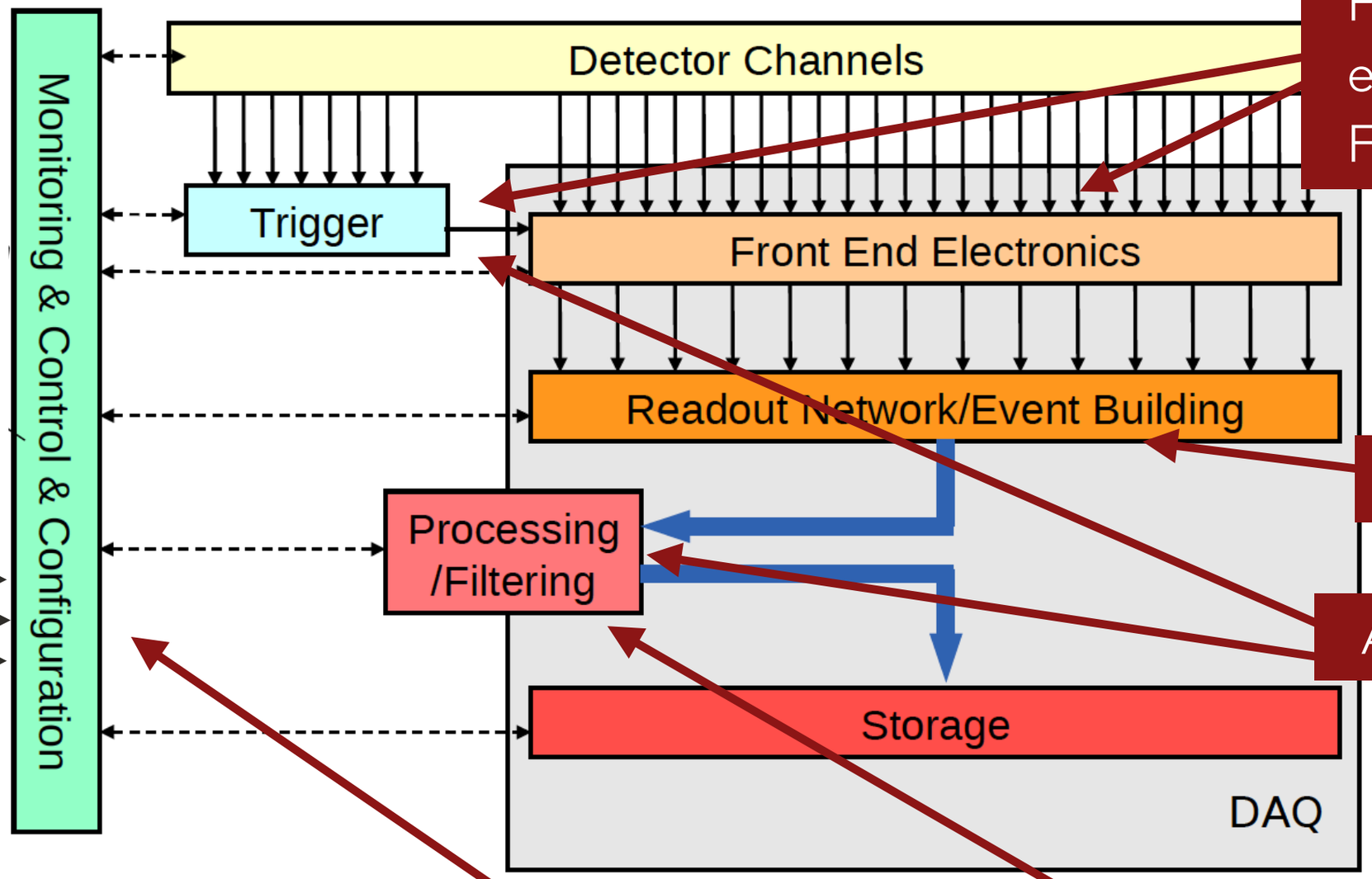
TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



Fast, custom electronics: FPGAs, ASICs

Networks

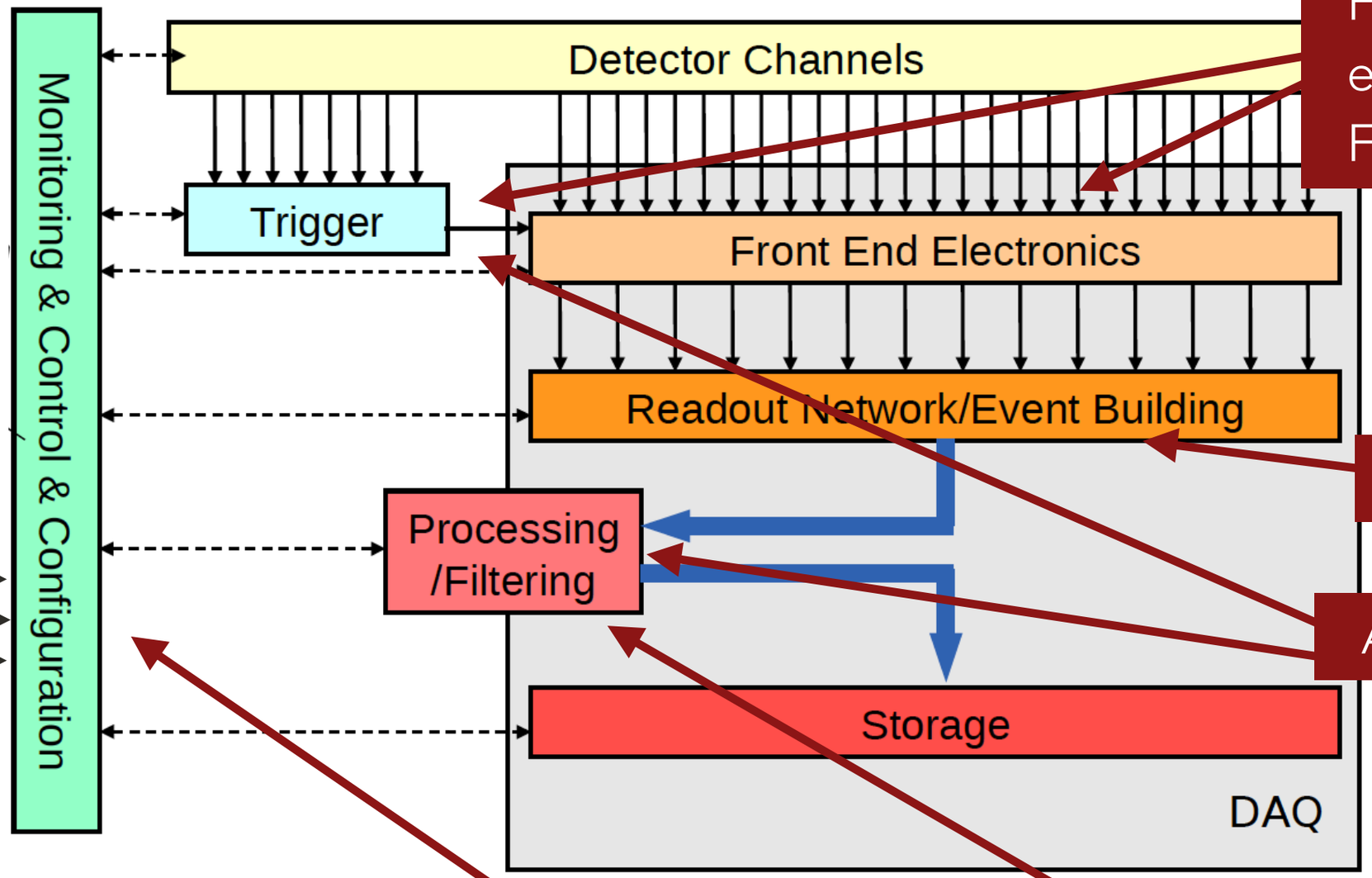
Algorithms

Computing power: CPUs/ GPUs

Software & hardware; dynamic control

TDAQ COMPONENTS

- Trigger & Data Acquisition comprise the systems for deciding which data to record (Trigger) and getting it off the detectors to storage for analysis (DAQ)



Fast, custom electronics: FPGAs, ASICs

Networks

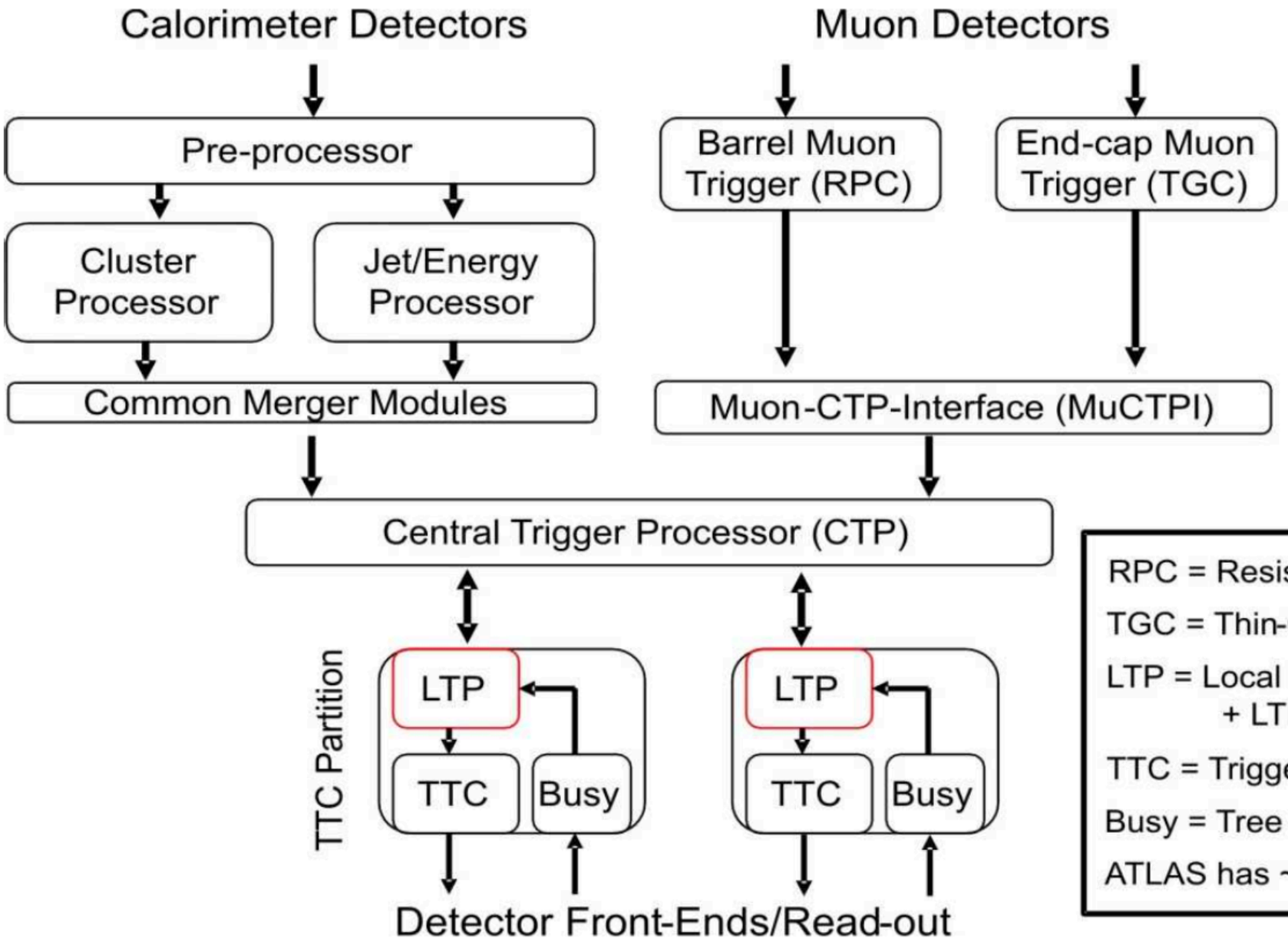
Algorithms

People!

Software & hardware; dynamic control

Computing power: CPUs/ GPUs

ATLAS LEVEL 1 TRIGGER SYSTEM



RPC = Resistive-Plate Chamber

TGC = Thin-Gap Plate Chamber

LTP = Local Trigger Processor + LTP interface

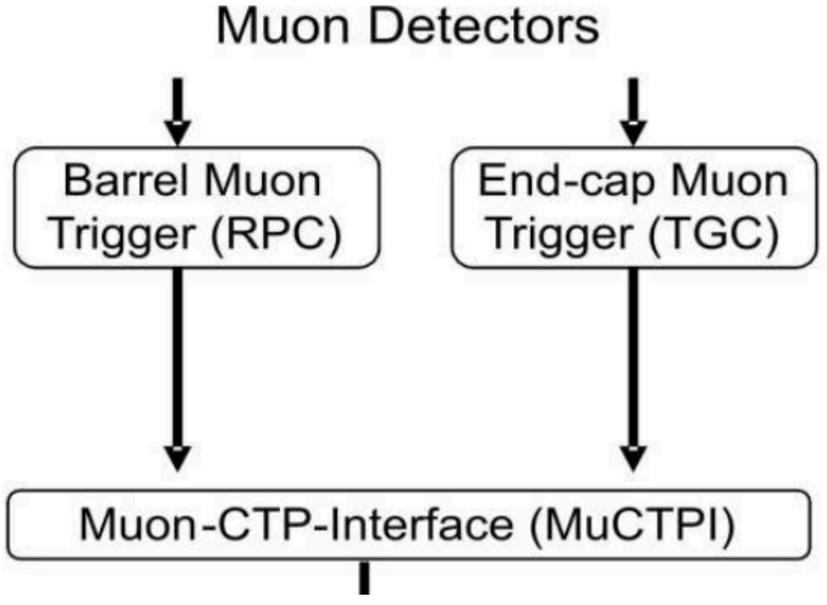
TTC = Trigger Timing & Control

Busy = Tree of ROD_Busy modules

ATLAS has ~40 TTC partitions

Fig. Ref

ATLAS LEVEL 1 TRIGGER SYSTEM



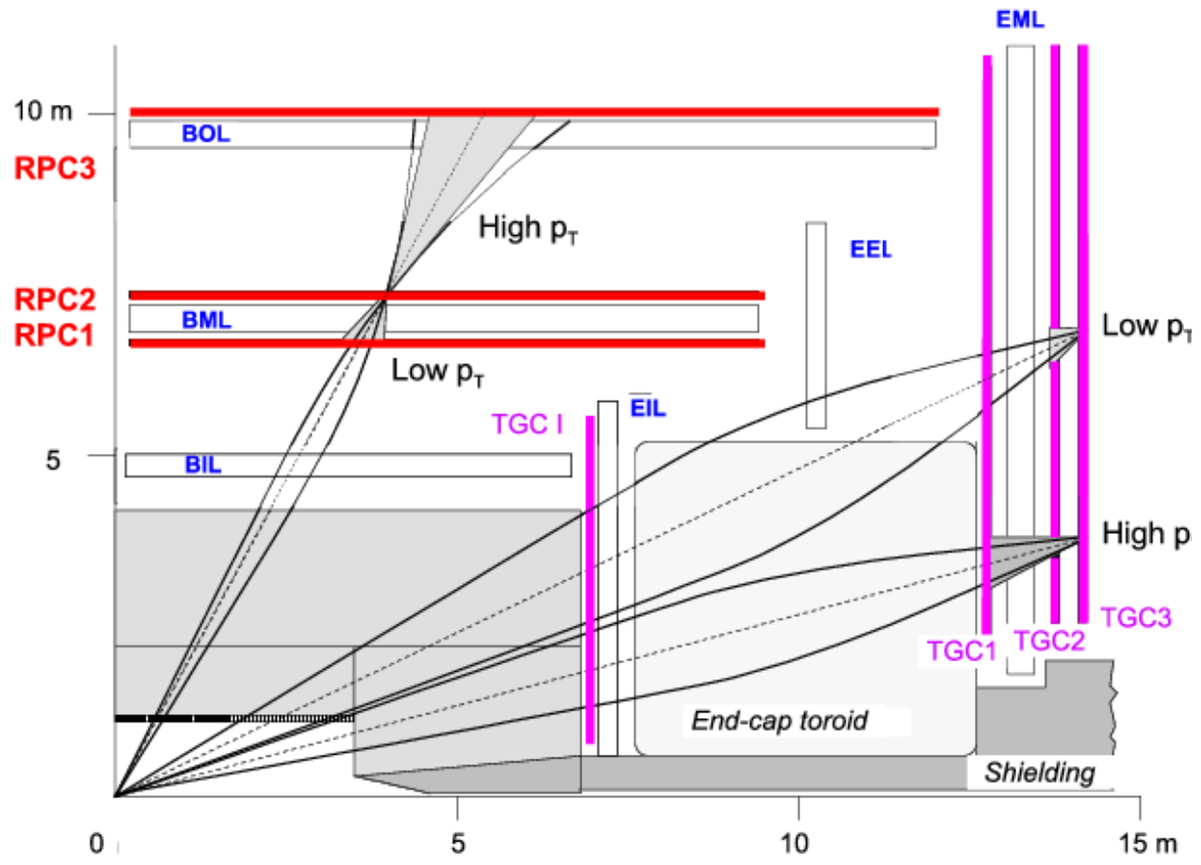


Fig. Ref

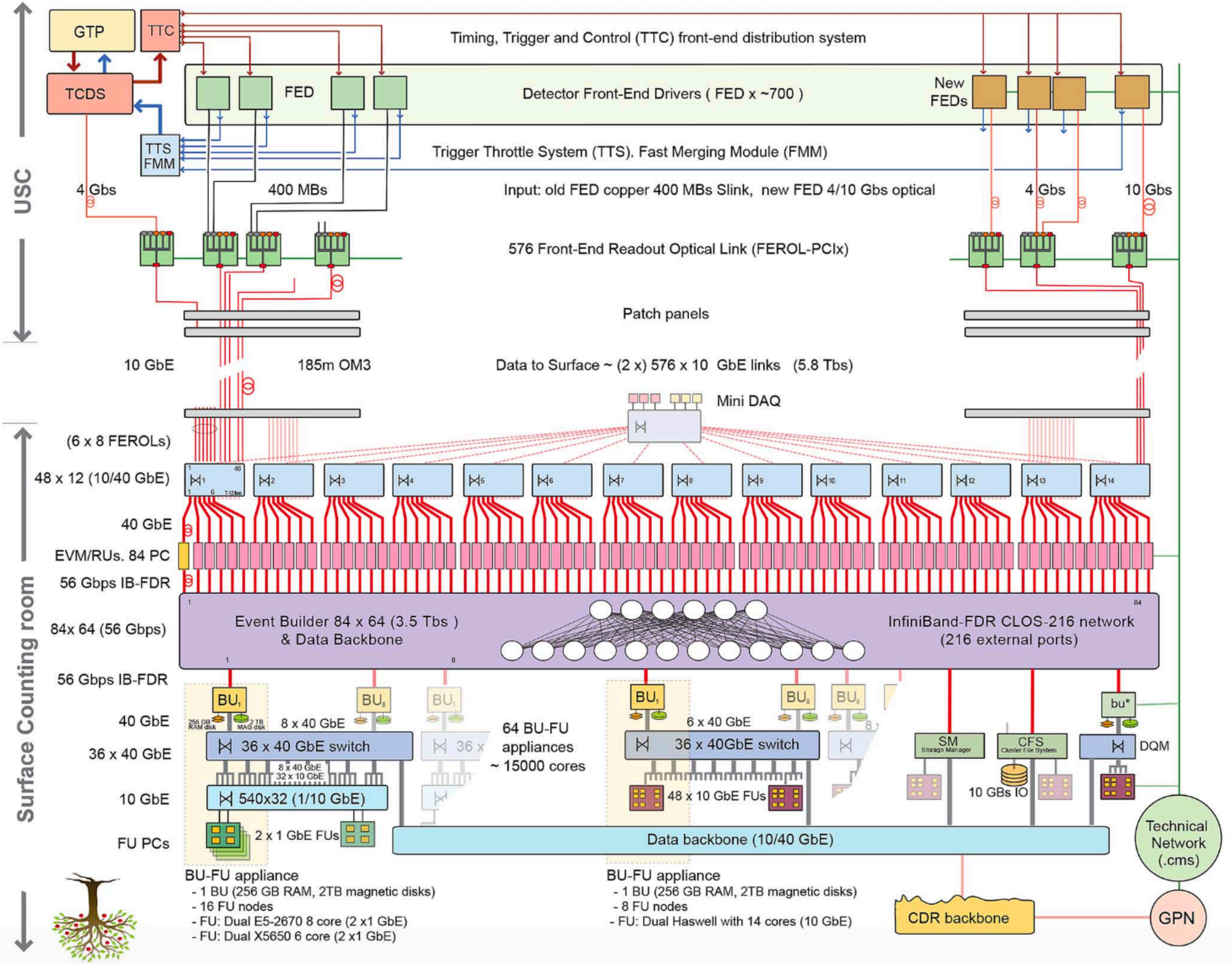

USC
Surface Counting room
GTP
TTC
TCDS
TTS
FMM
FED
Timing, Trigger and Control (TTC) front-end distribution system
Detector Front-End Drivers (FED x ~700)
New
FEDs
Trigger Throttle System (TTS). Fast Merging Module (FMM)
4 Gbs
400 MBs
Input: old FED copper 400 MBs Slink, new FED 4/10 Gbs optical
4 Gbs
10 Gbs
576 Front-End Readout Optical Link (FEROL-PCIx)
Patch panels
10 GbE
185m OM3
Data to Surface ~ (2 x) 576 x 10 GbE links (5.8 Tbs)
Mini DAQ
(6 x 8 FEROLs)
48 x 12 (10/40 GbE)
40 GbE
EVM/RUs. 84 PC
56 Gbps IB-FDR
84x 64 (56 Gbps)
Event Builder 84 x 64 (3.5 Tbs)
& Data Backbone
InfiniBand-FDR CLOS-216 network
(216 external ports)
56 Gbps IB-FDR
40 GbE
36 x 40 GbE
10 GbE
FU PCs
BU1
BU8
256 GB RAM disk
2 TB MAG disk
8 x 40 GbE
36 x 40 GbE switch
8 x 40 GbE
32 x 10 GbE
540x32 (1/10 GbE)
2 x 1 GbE FUs
64 BU-FU
appliances
~ 15000 cores
6 x 40 GbE
36 x 40GbE switch
48 x 10 GbE FUs
SM
Storage Manager
CFS
Cluster File System
10 GBs IO
bu*
DQM
Data backbone (10/40 GbE)
Technical
Network
(.cms)
GPN
CDR backbone
BU-FU appliance
- 1 BU (256 GB RAM, 2TB magnetic disks)
- 16 FU nodes
- FU: Dual E5-2670 8 core (2 x1 GbE)
- FU: Dual X5650 6 core (2 x1 GbE)
BU-FU appliance
- 1 BU (256 GB RAM, 2TB magnetic disks)
- 8 FU nodes
- FU: Dual Haswell with 14 cores (10 GbE)

Fig. Ref