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An AVX512 Extention to OpenQCD

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We publish an extension of openQCD-1.6 with AVX512 vector instructions using Intel intrinsics. Recent Intel processors support extended instruction sets with operations on 512-bit wide vectors, increasing both the capacity for simultaneous floating point operations and of register memory. Optimal use of the new capabilities requires a reorganisation of data and floating point operations into these wider vector units. We report on the implementation and performance of the AVX512 OpenQCD extension on clusters using Intel Knights Landing and Xeon Scalable (Skylake) CPUs. In complete HMC trajectories with physically relevant parameters we observe a performance increase of 5% to 10%.

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