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Lattice QCD on upcoming ARM architectures

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We present our experiences porting Lattice QCD code to upcoming ARM processor architectures, which will be used for future supercomputers such as QPACE 4 (University of Regensburg, Germany) and Post-K (RIKEN, Japan). These processors will support the ARM Scalable Vector Extension (SVE). SVE allows to design processor cores providing significantly higher performance compared to the cores available today.

SVE is a novel extension of the ARM instruction set architecture. It supports a vector-length agnostic (VLA) programming model that, in contrast to the traditional fixed-size SIMD instruction approach, can adapt to different vector length at run-time. The necessary hardware support for VLA helps for parallelizing applications at vector instruction level.

In this poster we present results from enabling LQCD applications SVE. More specifically, we ported the "Grid" library, which is a LQCD library optimized for processor architectures that feature wide SIMD instructions. Code correctness has been verified using emulators.

We collaborate with ARM in order to evaluate and develop key aspects of an efficient SVE toolchain, which includes SVE compiler and code profiler technology. First processors supporting SVE are expected to become available in 2020.

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