

Single-Phase Electronics

David Christian

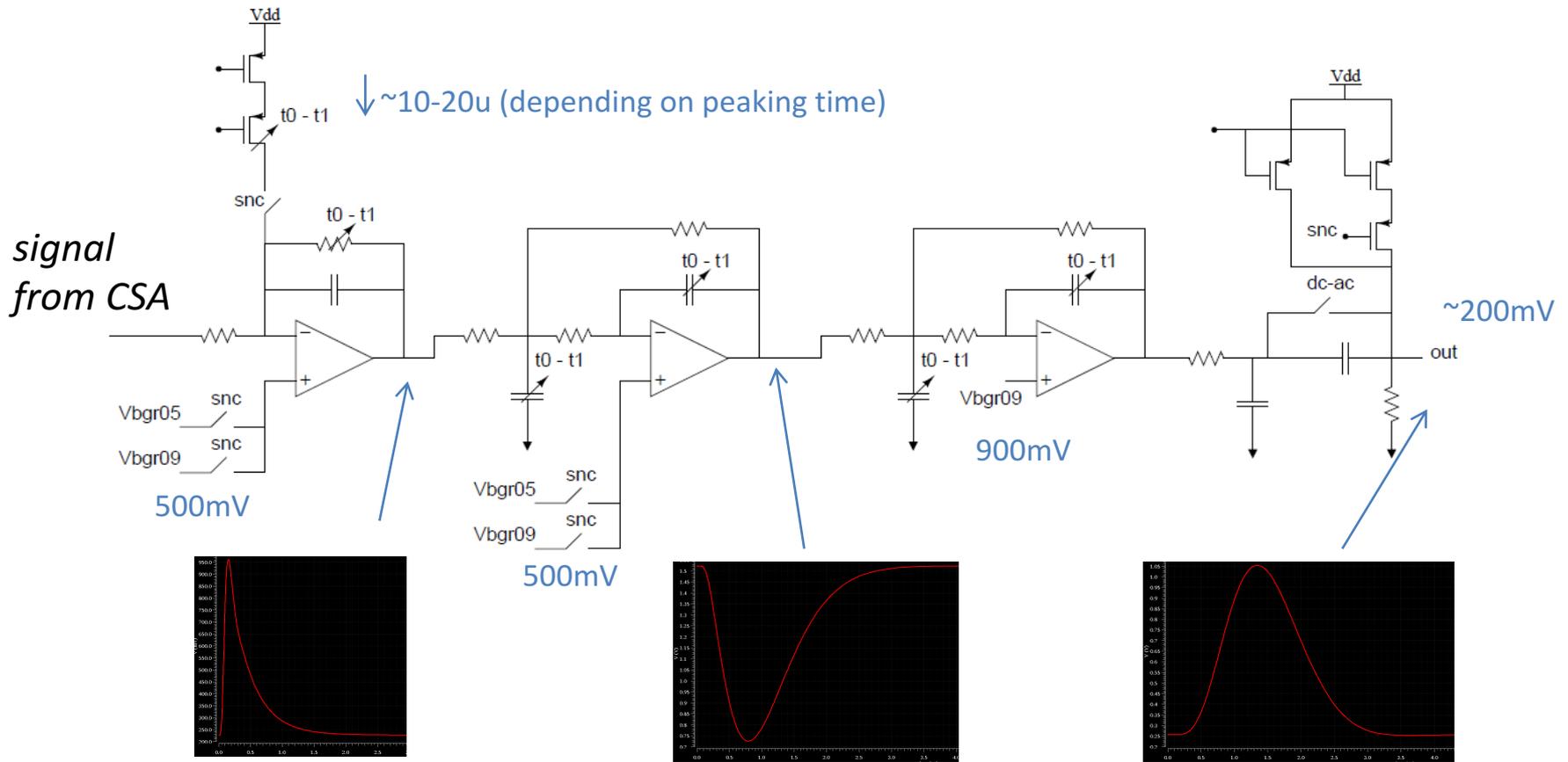
Strategy

- Top Priority is finishing ASIC development:
 - Minor modifications planned to FE ASIC (BNL)
 - Developing a pipelined ADC (LBNL-FNAL-BNL collaboration)
 - Submission in June.
 - Developing COLDATA (FNAL)
 - Submission in June.
 - Supporting adaptation to DUNE of the SLAC “Cryo” ASIC specified originally for nEXO (SLAC).
 - Submission in February.
 - Testing an ADC developed at Columbia U. for ATLAS
 - Monitoring SBND cold tests of a commercial ADC
- The timeline for these developments as well as a description of the types of tests that will be done is contained in a strategy document (DUNE-doc-6658).
- The process we will follow to choose which of these developments to continue is documented (DUNE-doc-7156).

ASIC Status: LArASIC

- 180nm CMOS
- LArASIC uses 1.8V and operates either with a 900 mV baseline (for induction wires) or a 200 mV baseline (for collection wires)
- The 200 mV baseline is sensitive to strain caused by CTE mismatch between the plastic package and the silicon.
- A design modification to make the 200 mV baseline insensitive to strain has recently been completed.
- We expect to submit in late March.
- We are also planning to add a differential stage to the output to better match the new ADC ASIC; this version will be submitted late in FY18 or early in FY19.

Collection mode – DC analysis – original FE



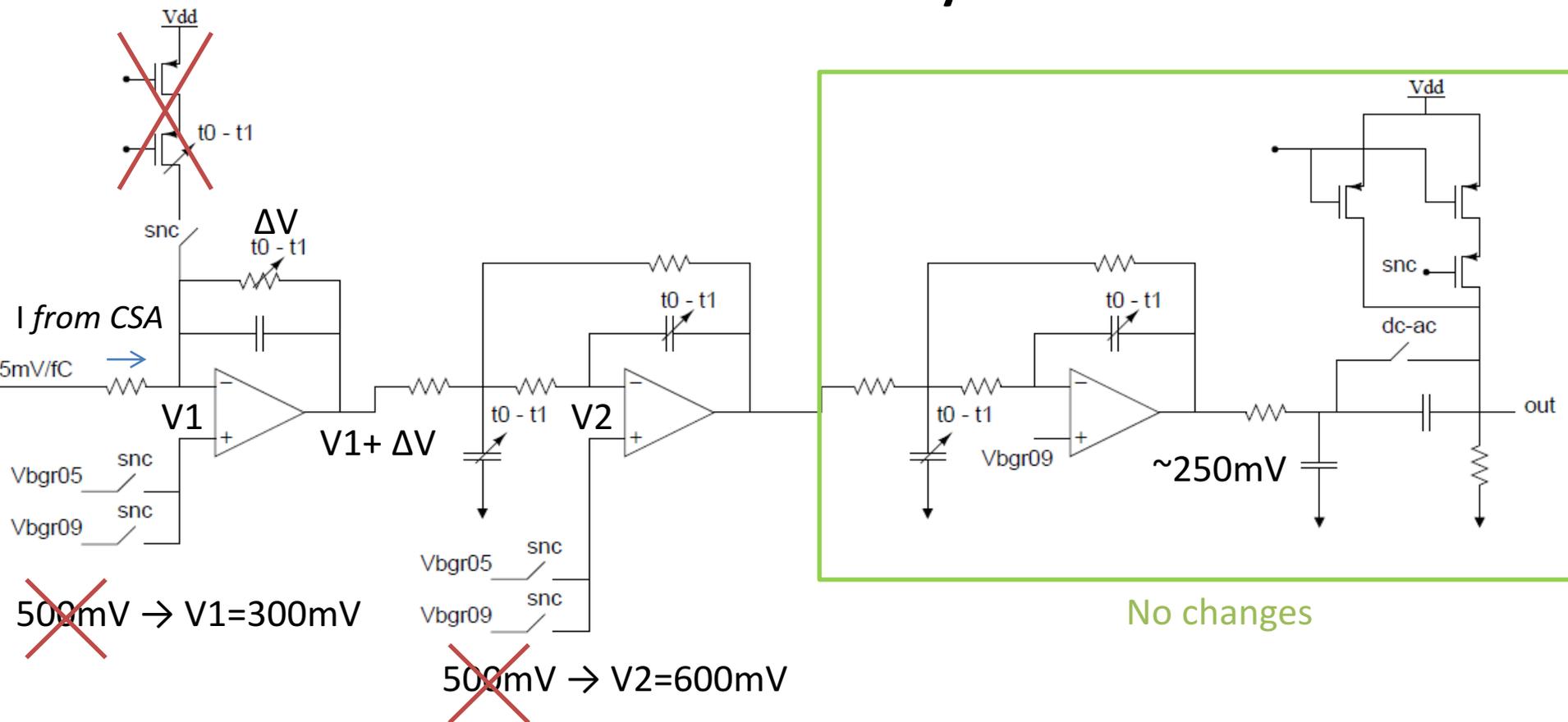
Original FE shows non-uniformity in baseline value – only in collection mode – due to packaging

Baseline doesn't show issues regarding non-uniformity in induction mode



Modify DC circuits for collection mode – making similar to the induction mode - maintaining the same (DC) operating points of the original one

Collection mode – DC analysis – new FE



- New DC bias points – V1 and V2 – in order to keep the same DC levels in the analog chain
- Simulations (corner analysis, Monte Carlo & parasitic) have been conducted to make sure the new configuration doesn't affect performances – compared to the original design.
- Stability of Amplifiers due to the variations of bias points – no changes in the active components in order to minimize risks

Collection mode – simulated channel response

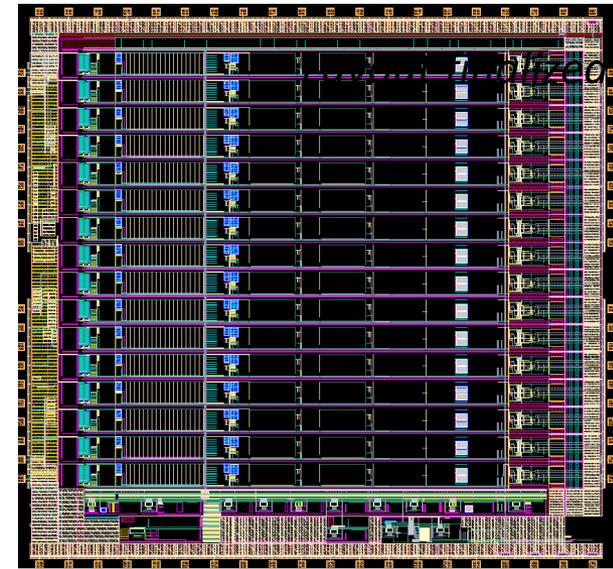
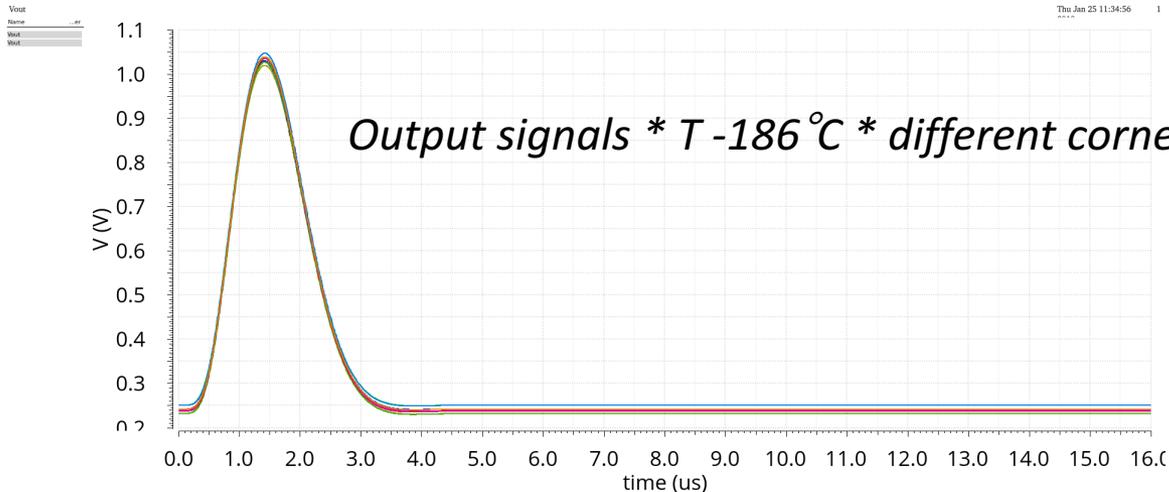
OLD FE

DC output signals

NEW FE

27	248m	256m	266m
-186	238m	244m	250m
-196	237m	242m	247m
T [°C]/Vdd [V]	1.7	1.8	1.9

27	241m	250m	260m
-186	234m	239m	244m
-196	231m	236m	241m
T [°C]/Vdd [V]	1.7	1.8	1.9



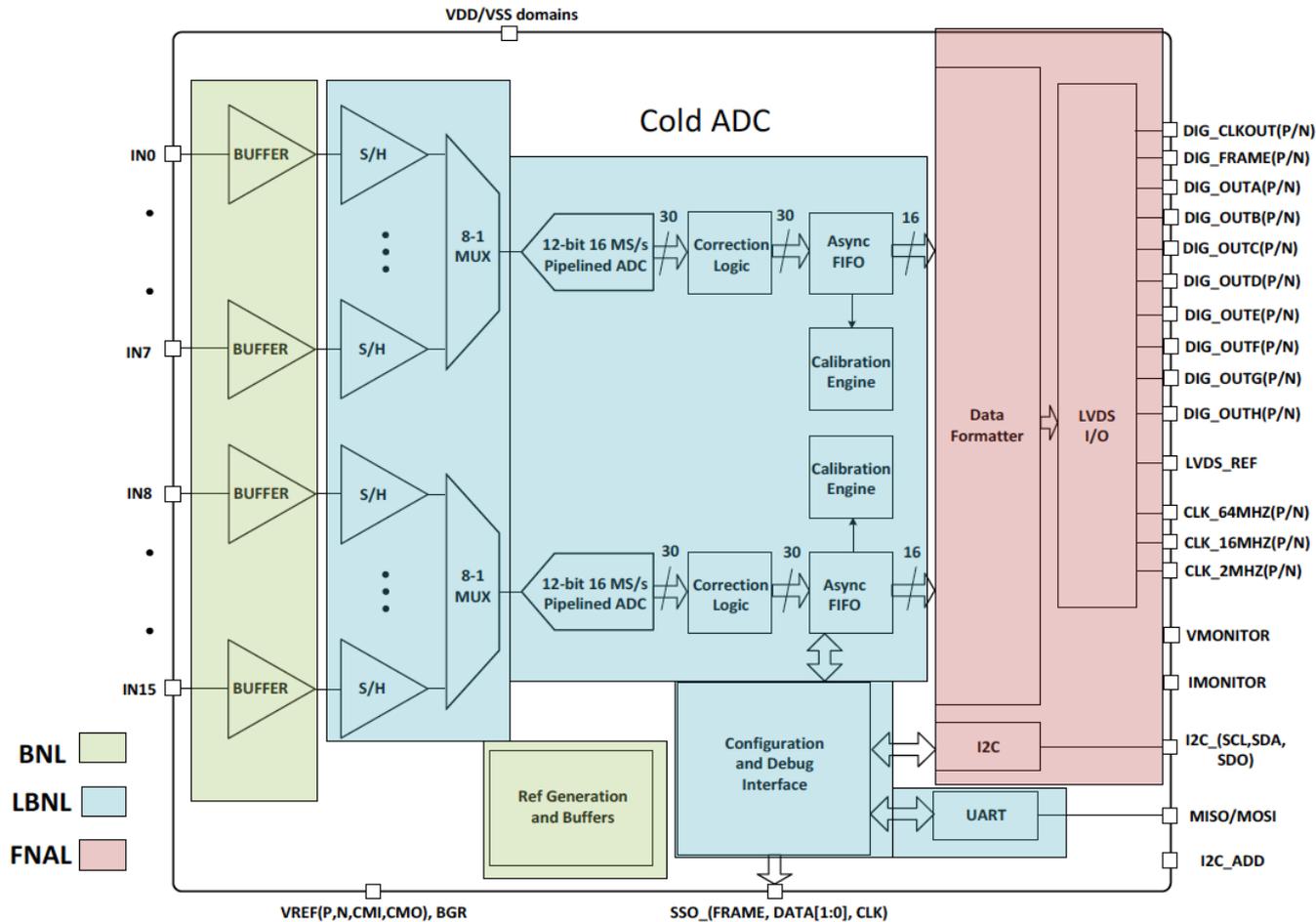
- Schematics and layout design of FE ASIC revision are complete.
- Post-layout simulation is being finalized

ASIC Status: Cold ADC

- The lead engineer is Carl Grace (LBL).
- The new design is a calibrated pipelined ADC.
- BNL designers are responsible for the interface with LArASIC and for reference voltages and currents.
- LBL designers are responsible for the ADC core.
- FNAL designers are responsible for the interface to the COLDATA, and for layout and integration.
- 65nm CMOS (sharing models and standard cell library with COLDATA)
- The design is progressing well.
- We anticipate submission in June.

BNL-LBNL-FNAL Collaboration (see DUNE-doc-5825)

Design Responsibilities



Key Cold ADC Specs

Specification	Value	Units	Note
Number of channels	16 (single-ended or differential)		
Sampling Rate	2	MS/s	Channel rate
Aggregate Output Data Rate	512	Mb/s	8 LVDS pairs at 64 Mb/s each
Noise	175	μ V-rms	< 1/2 LARASIC noise w/ margin
ADC Resolution	12	bits	
ADC Linearity	+/- 0.5	LSB	@ 12-bit level
ENOB	10.5	bits	SNDR \approx 65 dB
Input Range	0 – 1.6	V	

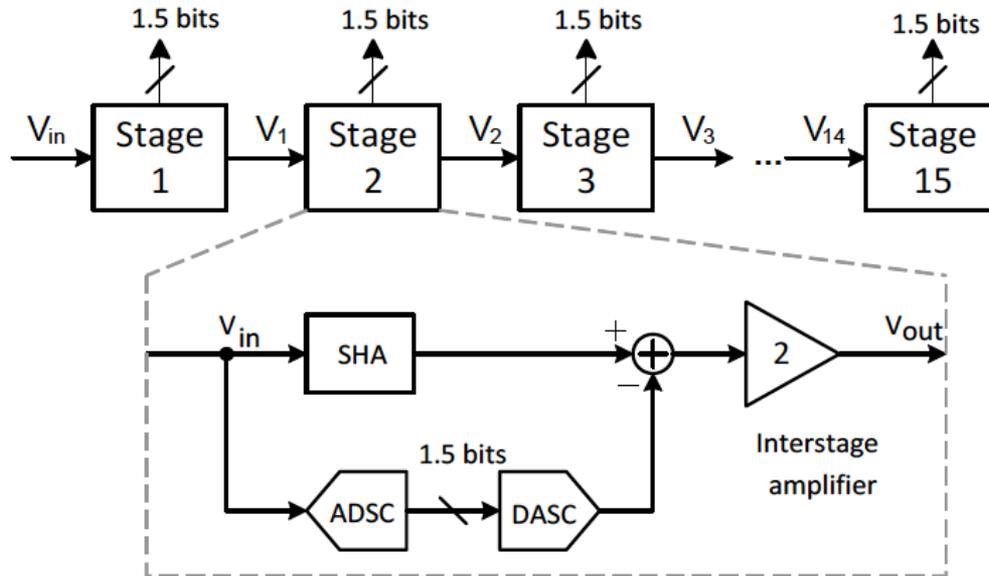
Noise Partitioning

- What generates noise in the Cold ADC ASIC?

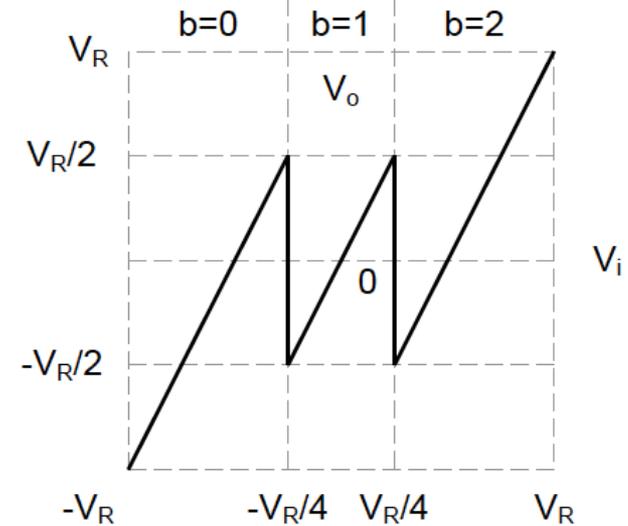
Block	Noise [$\mu\text{V-rms}$]	% total noise
ADC	160	64
SHA	80	21
Buffer	50	8
Reference	50	8
Total	175	100

ADC Top Level

Pipelined ADC



ADC block diagram

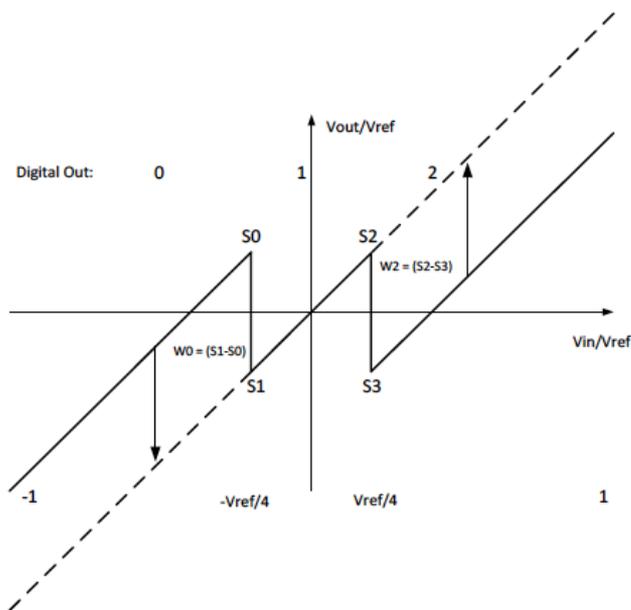


ADC stage transfer characteristic

Pipelined ADC capable of about 10-bits or so of raw accuracy (limited by cap mismatch and op amp finite gain)

Calibration Concept (cont.)

- Use proven Soenen – Karanicolas algorithm → converts unknown radix (depends on component matching and finite open-loop gain) to base-2
- Technique based on fact that missing codes in ADC transfer characteristic can be corrected as long as all decision levels present
- Set input to decision level, force decision 1 & 0, drive difference to 0



Decision	Weight	Measurement
0	w_0	$S_1 - S_0$
1	0	N/A
2	w_2	$S_2 - S_3$

$$\frac{ADC_{out}}{V_{ref}} = \sum_{j=0}^{k-1} w_{u(j)} j$$

Design Risk Mitigation

BLOCK	WORK-AROUND
Buffer	Bypass (directly connect LARASIC to ADC)
ADC References	Bypass (use external references)
Bandgap Reference	Bypass (use external BGR and/or external references)
Calibration Algorithm	Calibrate off-line and load gain estimates into register file
Correction Logic	Use uncalibrated (traditional) ADC output
Digital Interface to colData	Route ADC data through SSO (can still evaluate ADC performance)
Configuration Interface	Read and Write with either I2C or UART
ADC Gain Boosting	Include gain booster kill switch

Simulation Results

Calibration algorithm is highly successful at suppressing distortion.

# stages calibrated	DNL [LSB]	INL [LSB]	SNDR [dB]	SFDR [dB]	ENOB [bits]
0	-1	4.1	55.5	62.1	9.4
4	-0.55	-0.56	66.3	85.5	11.0
8	-0.18	-0.23	67.7	88.7	11.1

Following Slides:

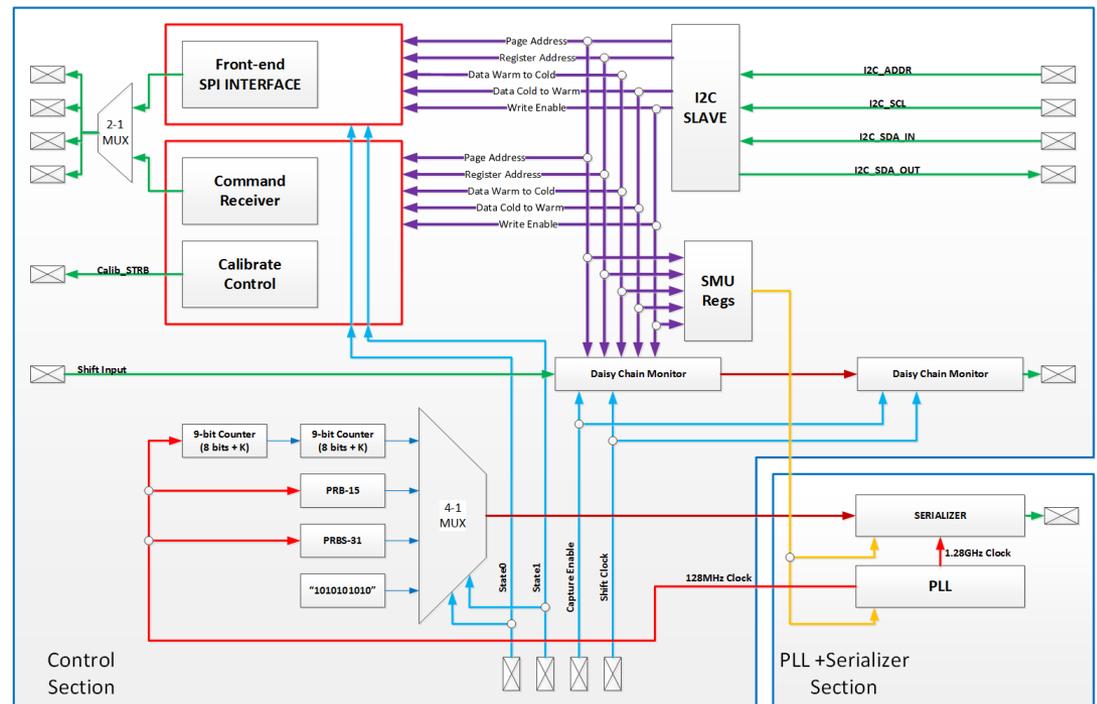
- Algorithm implemented in SystemVerilog RTL
- Same ADC parameters (except opamp gain reduced)
- All analog circuits (including non-idealities) also implemented using SystemVerilog real-number behavioral models
- System is evaluated at lower level of abstraction

ASIC Status: COLDATA

- Digital design of interface to the new cold ADC is essentially complete.
- Work is beginning on the pad frame.
- The only significant block remaining is the line drivers required to drive long cables (will include pre-emphasis).
- We expect to submit the chip in June.

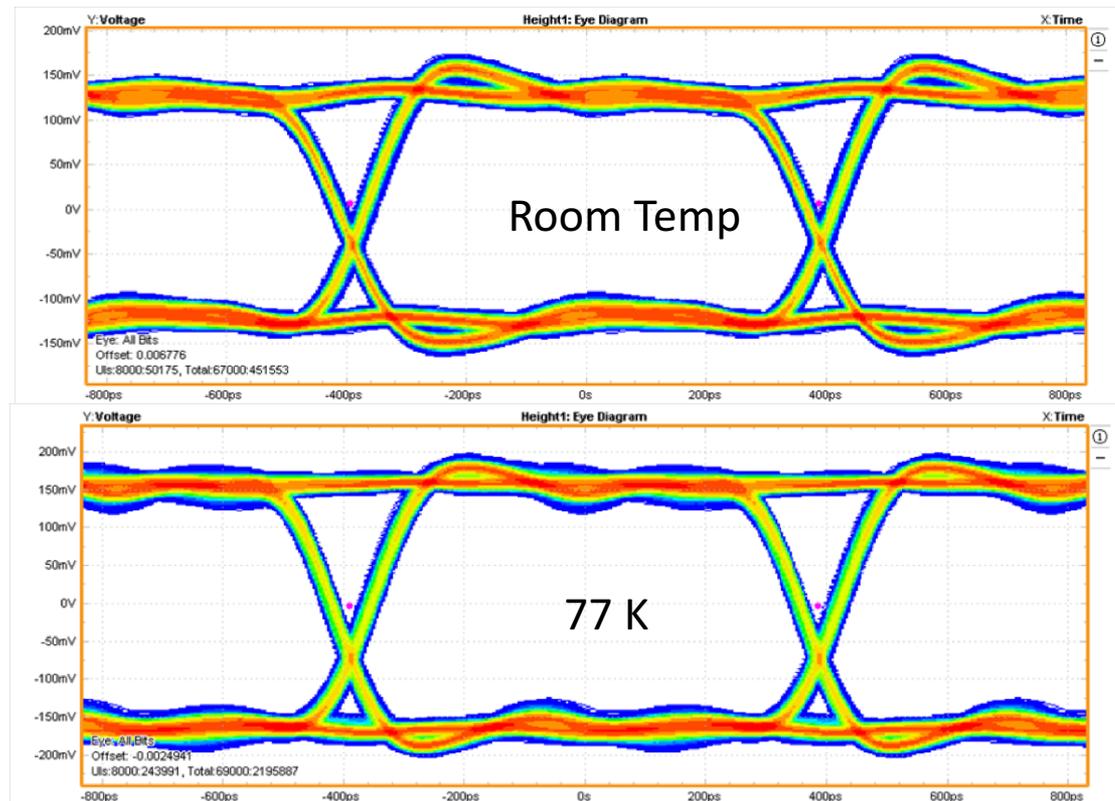
ASIC Status: COLDATA Prototype-1 (CDP1)

- 65nm CMOS.
- Fermilab-SMU collaboration.
- SMU = PLL & Serializer.
- Design uses models of transistors at LAr temperature developed at FNAL and a library of standard cells using those models developed Penn & FNAL.
- All elements except the PLL & Serializer were synthesized from RTL using the library (PLL uses TSMC library).
- Chip was submitted summer '17
- Tested fall '17
- Everything works as designed.

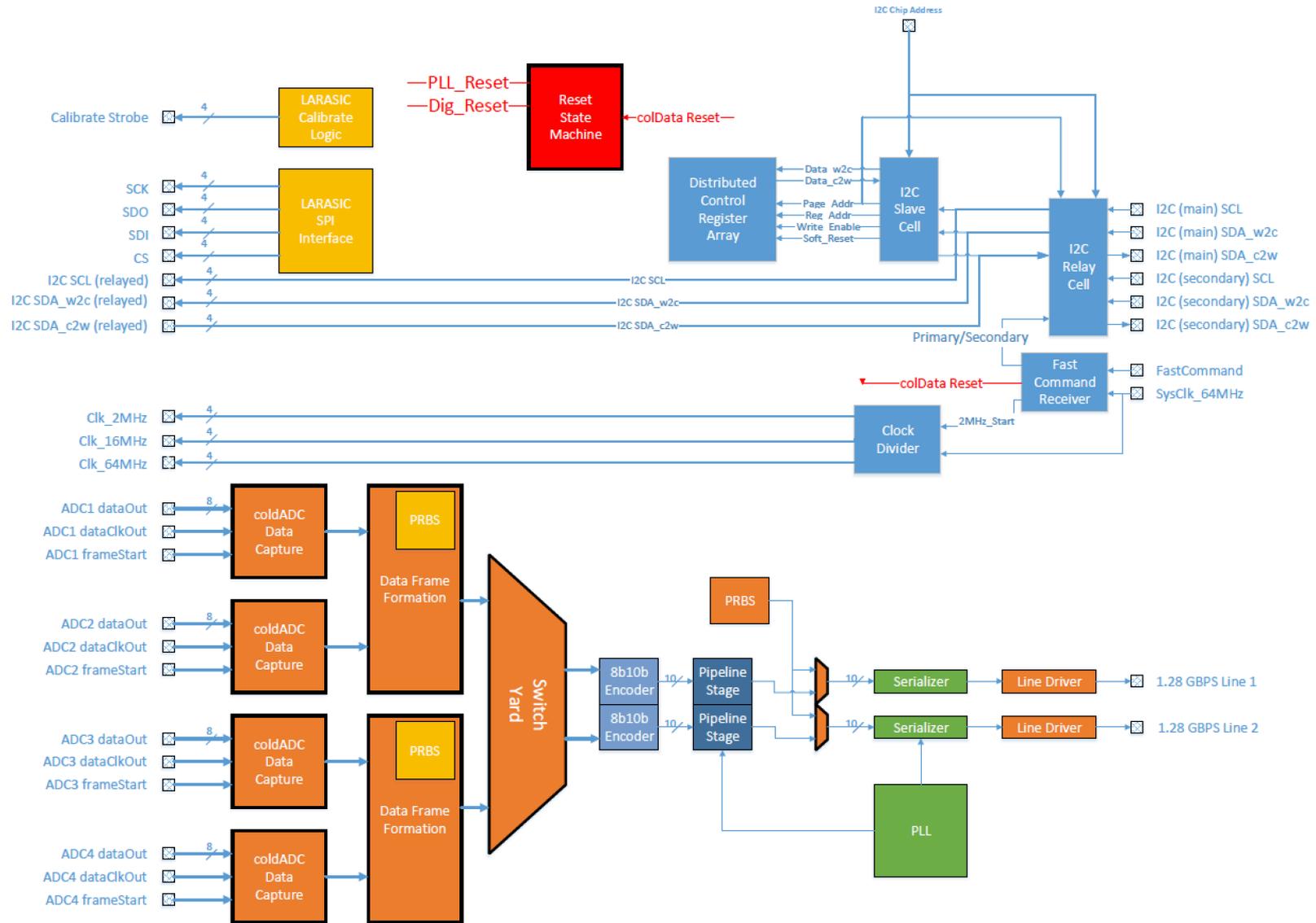


CDP1 PLL and serializer test results

- PLL works well both at room temperature and cold.
- Eye diagrams look very good – PRBS31 pseudo random bit pattern shown. (measured with a Tek DSA 72004C).
- More detail is at DUNE-doc-3063.



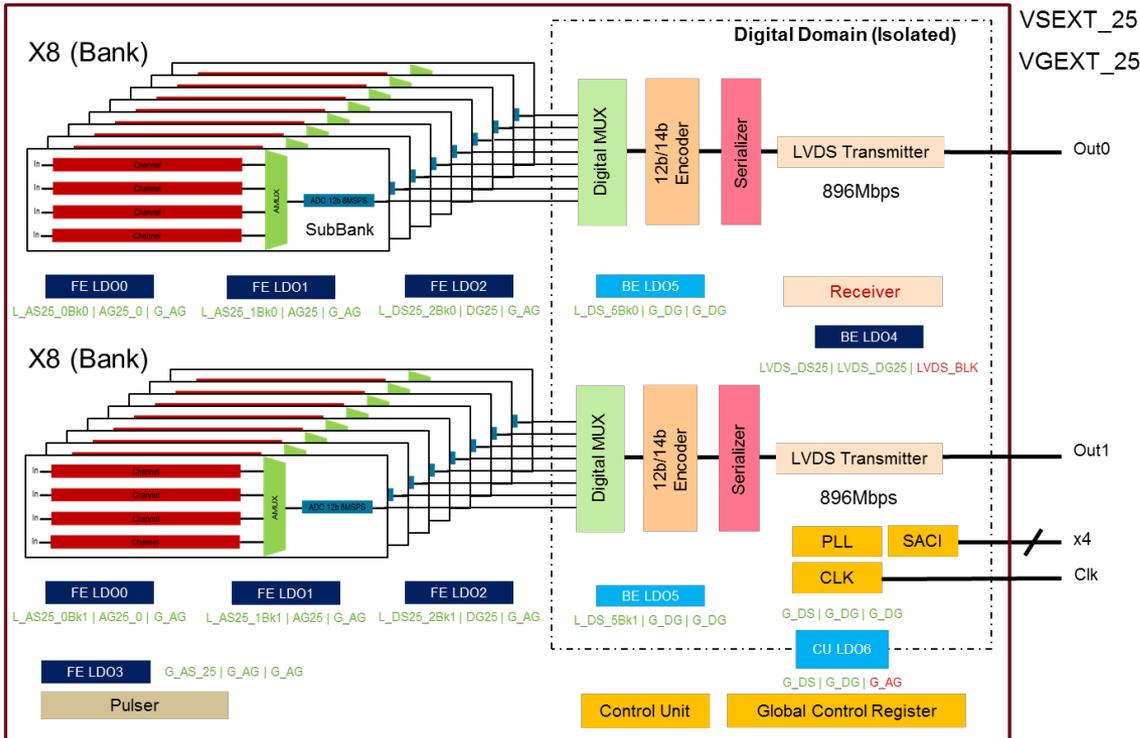
COLDATA Block Diagram



ASIC Status: Cryo

- 130 nm CMOS
- Specified for nEXO LXe (pad readout) TPC
- Design is well advanced
 - (including a version optimized for DUNE)
- Almost ready for submission (early March?).

Cryo Block Diagram



Features

- 64 channels divided in 2 32-channel sections with a single data output
- Distributed supply regulation on-chip
- 4x1 multiplexing of channels into a single ADC
- 8MSPS 12b SAR ADC (2 MSPS/ch)
- 12b/14b custom data encoding
- Serialization and LVDS data transmission at 896Mbps
- Digital domain isolated in DNW
- Dedicated slow control unit (SACI) and global registers to control functions and operative points (digitally assisted operation of analog sections)

DUNE Specifications	
Input capacitance	~ 200pF
Bandwidth	5 th Order Bessel Filter Programmable Peaking Time: 0.8us, 1.6us, 2.4us, 4.8us
Noise	~500e-
Multiple gains	1x, 0.5x, 0.25x, 0.125x
Dynamic Range	12bit
Sampling Frequency	2MSPS

Cryo Status (as of January 29)

- Technology Characterization (130nm CMOS) - done
- Cryogenic models – done
- Front-end channel implementation - done
 - Baseline architectural implementation completed
 - Antialiasing filter implementation completed
 - Noise studies completed
- ADC design - done
 - Architectural design (including buffers) completed
- LDO design - done
 - Architectural design completed
- Back-end implementation - done
 - (SACI / PLL / Encoders / Serializers / Transmitters)

Work in progress

- Biasing circuit and reference voltage generation
- Full integration of analog blocks and digital blocks
 - Further optimization might be required on analog and digital blocks
 - LDO noise optimization to be completed after full front-end simulation
- Layout of analog and digital section in progress

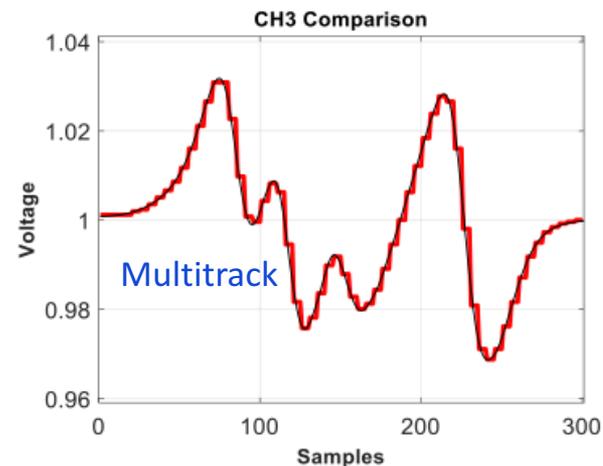
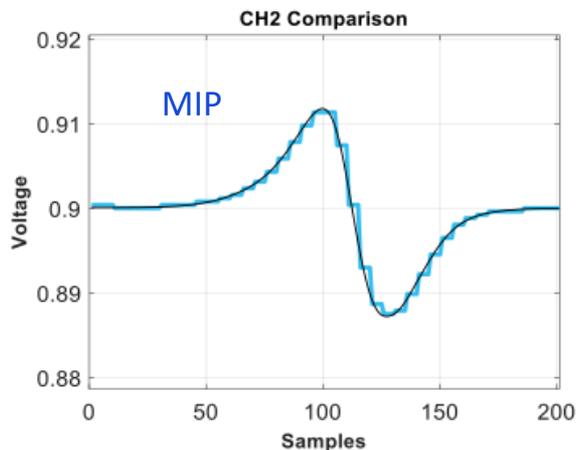
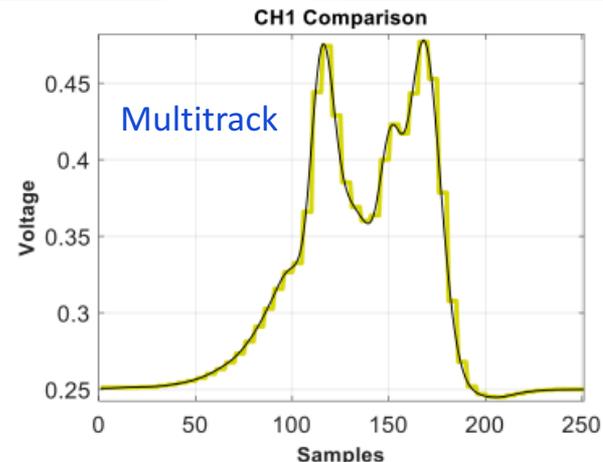
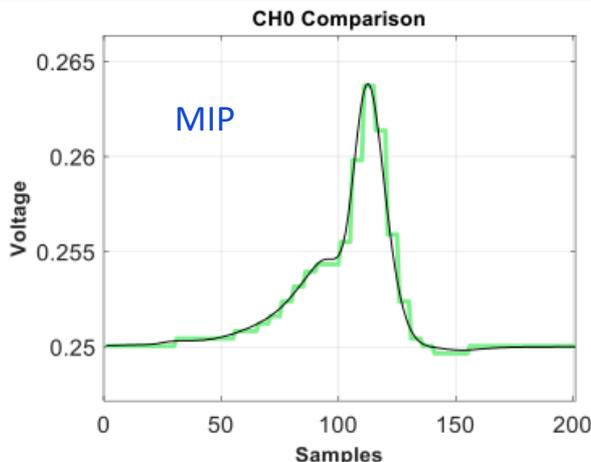
Simulation Results: Figures (2) (Angelo Dragone 2/12/18)

SLAC

- **Input / Output Comparison**

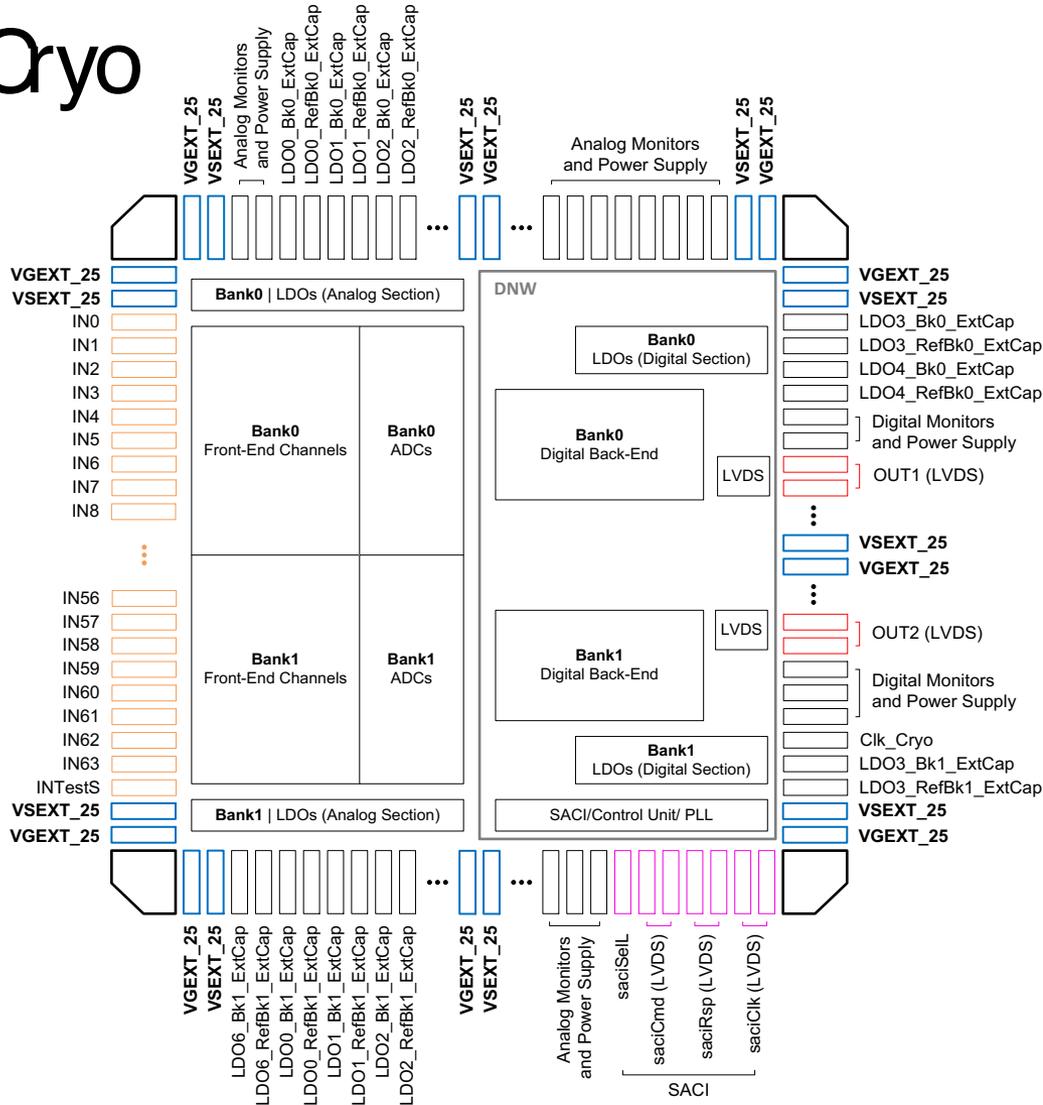
- ADC output signal is multiplied by the $LSB = 1.6V/2^{12}$ (decimal representation)
- Offset (V_{refn} from ADC) is added to the converted signal

ADC response to sample waveforms from LArSoft



Cryo Floor Plan and (Simplified) Pin Configuration

Cryo



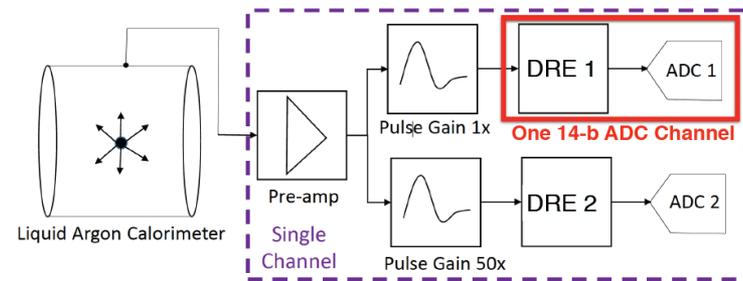
Description

- Minimal design
 - Only external Si caps are required
 - Only one power supply domain (2.5V)
- Left side:
 - Dedicated pins to input signals
 - 2.5V power supply pins
- Right side:
 - Output signals
 - Compensation caps for LDOs (digital)
 - Digital monitors
 - Clk signal
 - 2.5V power supply pins
- Top side:
 - Compensation caps for LDOs (analog)
 - Analog monitors
 - 2.5V power supply pins
- Bottom side:
 - Compensation caps for LDOs (analog)
 - Analog monitors
 - SACI control signals
 - 2.5V power supply pins
- Estimated Area to be defined

^{1,2} Internal digital/analog signals (debugging purpose)

Cold ADC Tests @ Columbia (slides from Georgia Karagiorgi)

- **ADC chip developed for ATLAS**
- **Previous (130nm) and upgrade (65nm) version**
- **ADC specs (65 nm)**
 - 12-bit pipeline SAR ADC
 - (DRE with internal x4 gain for 14-bit)
 - >10-bit resolution
 - 40 MSPS
 - Low power, radiation hard



- [Cold operation aside] characteristics ~match DUNE ADC specifications
- → Interested in characterizing **ADC performance in cold**

Planned tests @ Columbia

We are
getting
started
on this

- **Stage 1: Establishing basic functionality in cold** ←
- Stage 2: Exploring stability for extended operation in cold
- Stage 3: [If Stages 1 & 2 successful] Long-term operation stability tests, most likely at BNL

- Stages 1 & 2 are scope of signed FNAL/Columbia SOW for DUNE.

Current status

- Starting to set up for Stage 1 tests.
- Test board nominally works with 25MHz clock. Being modified for 2MHz sampling. (Aiming for 10MHz plus downsampling.)

SBND COTS ADC Option (slides from Hucheng Chen)

Progress Report of Lifetime Study of Commercial-Off-The-Shelf ADC for SBND TPC Readout

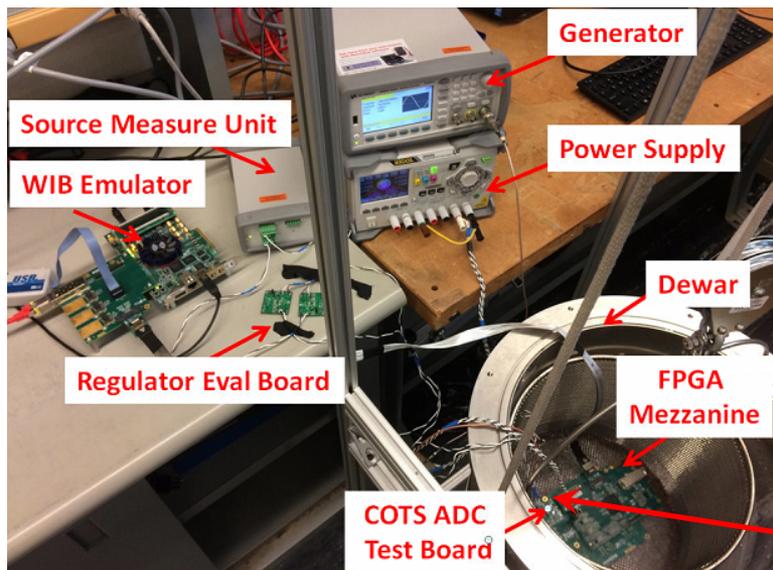
H. Chen, S. Gao, V. Radeka & J. Zhang

February 13, 2018

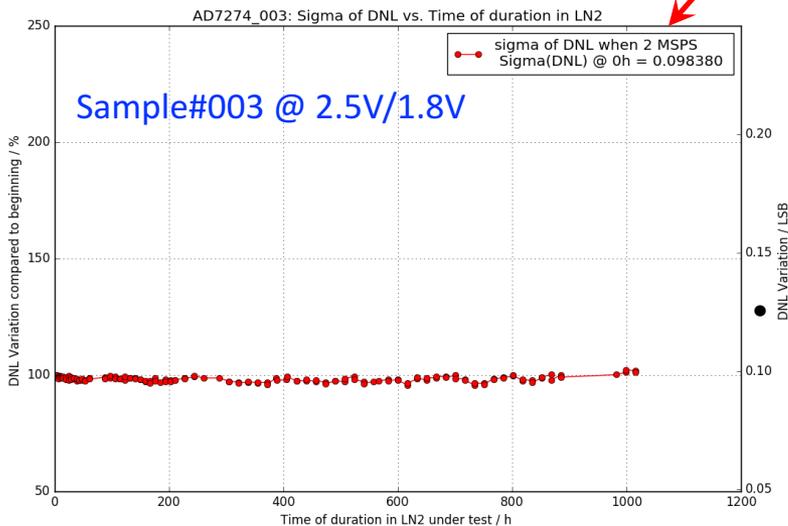
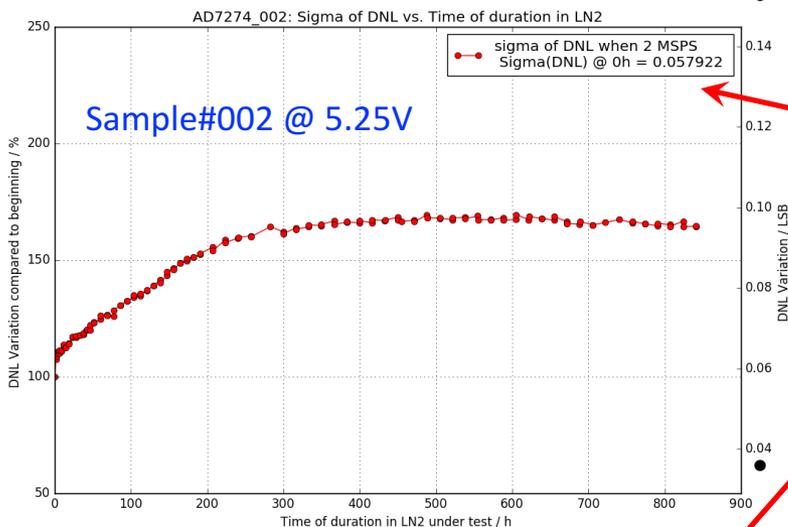
Abstract

This write-up is to document the preliminary test results of lifetime study of COTS (Commercial-Off-The-Shelf) ADC (Analog-to-Digital Converter) which is currently being considered as one option for the TPC readout of SBND experiment. The COTS ADC lifetime study in cryogenic operation includes two phases, the exploratory phase and the validation phase. This report will summarize the observations of ADI AD7274 lifetime study in the exploratory phase. It is planned to have this document further augmented with test results in the validation phase when the lifetime study is concluded.

- The COTS ADC work **benefits the future program**, which serves as a potential backup for DUNE far detector
 - COTS ADC lifetime study procedure has been developed
 - Cold qualification techniques are useful for future Dark Matter and Neutrino experiments
- Lifetime study of COTS ADC will take place in two different phases
 - Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is **Preparation phase**
 - The first phase is **Exploratory phase**
 - The second phase is **Validation phase**
- COTS ADC candidates with 100% cold yield identified
 - TI ADS7049-Q1: 180nm CMOS TI foundry
 - TI ADS7883: 500nm CMOS TI foundry
 - **ADI AD7274**: 350nm CMOS TSMC foundry
- **AD7274** is the main focus of lifetime study
 - Preparation phase completed in September 2017



SBND COTS ADC Lifetime Study



- **Exploratory** Phase completed in January 2018

- Stress test of two fresh AD7274 samples ($V_{DD}=V_{REF}=5.5V$ and $5.25V$)
 - Current variation is $< 10\%$, increase of sigma of DNL distribution ($>50\%$) is observed after **700+** hours
 - However, the performance of stressed chips look nearly as good as chips run at the nominal voltage in the cold.
- Cold test of one AD7274 sample with nominal voltage ($V_{DD}=2.5V$, $V_{REF}=1.8V$)
 - Current variation is $< 3\%$, change of sigma of DNL distribution is $< 5\%$ after **850+** hours

• Preliminary lifetime of COTS ADC extrapolated from past study would be more than 10^8 years

- The slope of **lifetime** vs $1/V_{ds}$ is independent of the **technology** node (from 180, 130 to 65 nm) and of the **foundry** (TSMC, Global ...).
- For all three nodes the lifetime is extended by an order of magnitude if V_{dd} (V_{ds}) is reduced by $\sim 6\%$.

- **Validation** phase is ongoing with two more AD7274 samples

- Plan to wrap up validation phase and conclude decision making process by early March
- Aim is to publish this study so that the community can replicate it in the future

Cryogenic Test System – DUNE-doc-4787

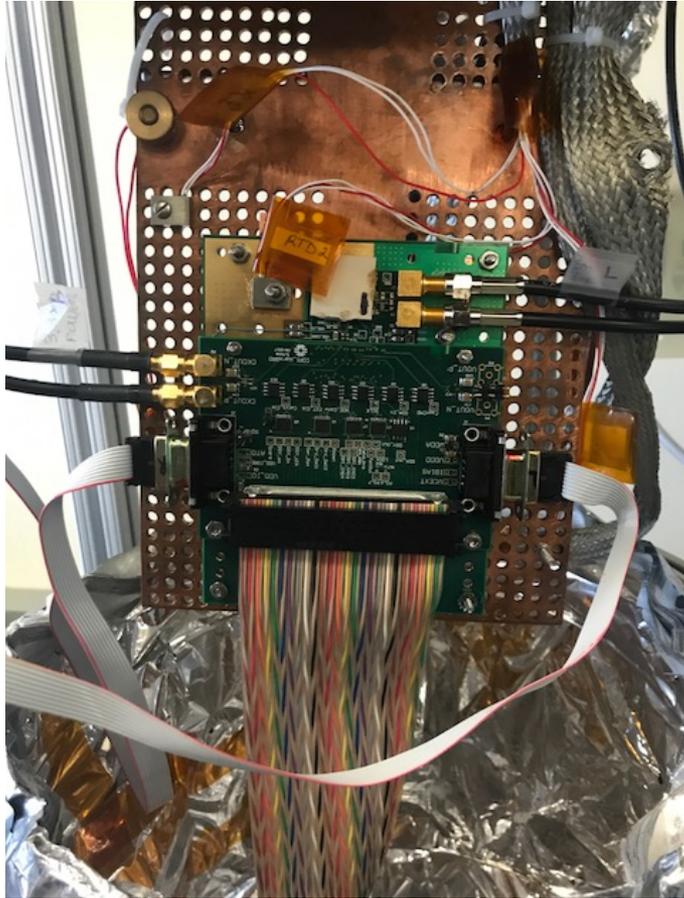
- Designed by Carl Bromberg & Dean Shooltz (MSU) for use in ProtoDUNE QC.
- Modifications required after BNL safety review.
- Now in use for ProtoDUNE.
- 6 systems being built to support DUNE R&D.



The overall process is to take a Device Under Test (DUT) through the following steps:

- (1) Room temperature insertion of the DUT into the system
- (2) Purging with heated gaseous nitrogen to drive away moisture
- (3) Cooling the DUT with gaseous nitrogen
- (4) Immersion of the DUT in liquid nitrogen
- (5) Testing the DUT while immersed in liquid nitrogen
- (6) Draining away the liquid nitrogen
- (7) Warming the DUT with heated gaseous nitrogen
- (8) Removal of the DUT from the system

FNAL ASIC Group Cryo Cooler



Copper plate cooled by cold finger; board with twist-n-flat cable is ~100 degrees warmer.

