Single-Phase Electronics

David Christian

Consortium Membership and Organization

- Almost exclusively US institutions
  - BNL, Boston U., CERN, U. Chicago, U. Cincinnati, Colorado State U., U. Florida, FNAL, U. Hawaii, Iowa State U., LBNL, LSU, MSU, U. Penn, SLAC,SUNY Stony Brook, UC Irvine, UC Davis
  - Consortium Leader: David Christian (FNAL)
  - Technical Lead: Marco Verzocchi (FNAL)
  - Technical Proposal Editor: Michael Mooney (Colorado State U.)

Scope

- Inside the cryostat:
  - Front End Mother Boards (FEMBs) in “cold boxes.”
  - Associated power and signal cables
  - Bias cables for APA planes, electron diverters, and field cage termination electrodes
- On top of the cryostat:
  - Spool pieces that mount on cryostat feedthroughs
  - Warm interface feedthrough (PCB) and associated strain relief
  - Warm electronics crates (mounted on spool piece flange & mated to feedthrough PCB)
  - Warm interface boards
  - Power and timing cards
  - Warm power and bias cables
  - Bias voltage crates and power supplies (& some of the cable trays on top of the cyrostat)

Requirements

DUNE-doc-6419: 1 page intended to capture the requirements that drive our design.

	Requirement	Goal	Explanation	Comments
Front-End Noise	<1000 e- for an induction wire	<<600 e-	The noise requirement is derived from pattern recognition requirements. These are difficult to estimate since pattern recognition algorithms are still evolving. If one considers only the signal to noise ratio in individual ADC samples and requires a ratio of 5/1 or better based on a naive analysis of track finding, this yields a figure of ~1000 e- for induction wires (which are longer than the collection wires and see smaller signals than the collection wires). However, it is clear that lower noise would enable better pattern recognition & better two-track separation. Excellent two-track separation is vital to achieving the best possible vertex resolution (which is fundamentally limited by anode wire spacing). ProtoDUNE measurements indicate that noise <600 e- is achievable. Even lower noise is required for reconstruction to take best advantage of signals from gammas from excited nuclei (from neutron scattering, for example) and extremely low noise is required for reconstruction of neutrino events from some astronomical sources. The goal should be to keep the noise level as low as reasonably achievable (ALARA).	This is a requirement on total system noise. The design goal will be for the noise to be almost entirely due to random noise in the front end. A front end gain must be specified in order to derive a specification for ADC effective noise (in microvolts).
Front end peaking time	1 us	Adjustable	This requirement is driven by the need for optimal vertex resolution, which is determined by single track resolution and the power to separate two or more tracks which are close to one another. These are in turn determined primarily by the choice of anode wire spacing, anode-to-cathode spacing, bias voltages, and the distance between anode planes (as well as the lifetime of drifting electrons). Given the spacing between anode planes of just under 5 mm, a peaking time of 1 us is optimal for two-track separation.	Longer shaping time may be desirable for non-accelerator physics if lower noise can be achieved with longer shaping time.
Front end output baseline	Settable		The front end must accommodate mostly unipolar signals from charge collection wires and bipolar signals from induction wire signals	
ADC Sampling Frequency	2 Msps		Chosen to match the 1us shaping time (approximate Nyquist requirement)	
Maximum signal for no saturation	530,000 e-		Corresponds approximately to the charge deposited by one stopping proton and two more highly ionizing protons, all assumed to have trajectories at 45 degrees with respect to the beam axis. Chosen so that saturation will occur in less than ~10% of beam related events.	The largest signals will be associated with the primary vertex in events with many protons produced at the primary and in events when the trajectory of a particle is parallel to a wire so that the charge from a long path length arrives within a short time period.
Dynamic range	3000::1	4070::1	Given by the ratio between (the maximum signal for no saturation) and ~1/2 of the noise level.	The choice of IC technology for the FE determines the possible voltage swing of the output. This implies that the gain of the FE determines the maximum signal for no saturation. The smallest signal that can be measured reliably depends on the system noise. The requirement of a dynamic range of 3000 assumes a noise of 350 e- (achievable in simulation with a 3 us shaping time) and no saturation for signals of 530000 e- (85 fC).
Effective noise due to ADC	INL, DNL < 1 LSB Noise < .5 LSB		The most important ADC specification is the effective noise that the ADC adds to the noise intrinsic to the front-end. Linearity is important for calorimetry, but this does not drive the specification because ionization statistics limits the achievable calorimetric precision. Non linearity that is not perfectly characterized is equivalent to a noise term; the linearity requirement is derived from the requirement that the effective noise alway be dominated by the random noise of the front end amplifier.	A 12-bit ADC that covers 0-1.6V implies a bin width of 1.6V/4096 = 390 uV. The RMS noise due to the bin width is 390uV/Sqrt(12) = 113 uV. This determines the absolute minimum noise contribution of a 12-bit ADC. With the FE gain set to 4.7 mV/fC, 113 uV corresponds to 150 e-. When convoluted with 500 e- of FE noise, this yields 522 e- total. The effective noise contribution of the ADC depends on the gain setting of the front-end. The effect of higher ADC noise can be minimized by using higher FE gain, at the cost of lower dynamic range.
Power	<50 mW/channel		From cryogenics requirement (DUNE-doc-112-v17) estimate of 23.7 kW for detector electronics in a 10 kT detector... 23.7 kW/384000 = 61.7 mW/channel.	ProtoDUNE is ~25 mW/channel for SP TPC cold electronics. Local hot spots may cause the liquid argon to boil. The dielectric strength of argon gas is much lower than liquid argon, and could therefore lead to breakdown if present in regions of high electric field. The current cold electronics modules are designed to provide a controlled path for bubbles to exit the liquid volume, so it is our understanding that this issue has been mitigated by this design. It should be noted that all ProtoDUNE cold electronics are located at the top of the APAs, whereas boiling is a potential issue only for DUNE electronics located below the lower APAs.
Reliability	<0.7% channel failure per APA plane in 30 years operation		Milind Diwan's requirements document starts with the requirement that the fiducial volume of the far detector should not be reduced by more than 2%. Using the approximation that signals from all three APA planes are required to form a hit, he says that the fiducial volume is reduced by a factor of p^3, where p = single plane efficiency. 99.3%^3 = 97.9%	***This needs to be a DUNE-wide requirement.***

Key Interfaces

- All Consortia
  - Enforcement of the grounding scheme (no electrical connections between APAs or between photon detectors & APA, reference voltage connection for all electronics made at the feed through flanges & connected to the cryostat [detector ground]).
- APA
  - Electrical & mechanical interface with FEMBs (to CR boards)
  - Provide bias voltages for APA wires (also to electron diverters & field cage termination electrodes [HV Consortium]); we have responsibility for everything from the bias supplies to the SHV board on the APA.
  - Routing of cables from bottom APA (inside frames or up the sides of the cryostat).
- DAQ
  - No trigger function in WIBs
  - Data transmitted on optical fibers to DAQ elements located in the Central Utility Cavern.
  - Design of the fiber plan can be delayed (current baseline assumes 1.28 Gpbs links; may use 5 or 10 Gpbs as in ProtoDUNE).
- Photon Detector
  - CE provides spool pieces (mounted on cryostat feed-throughs) and cable trays.

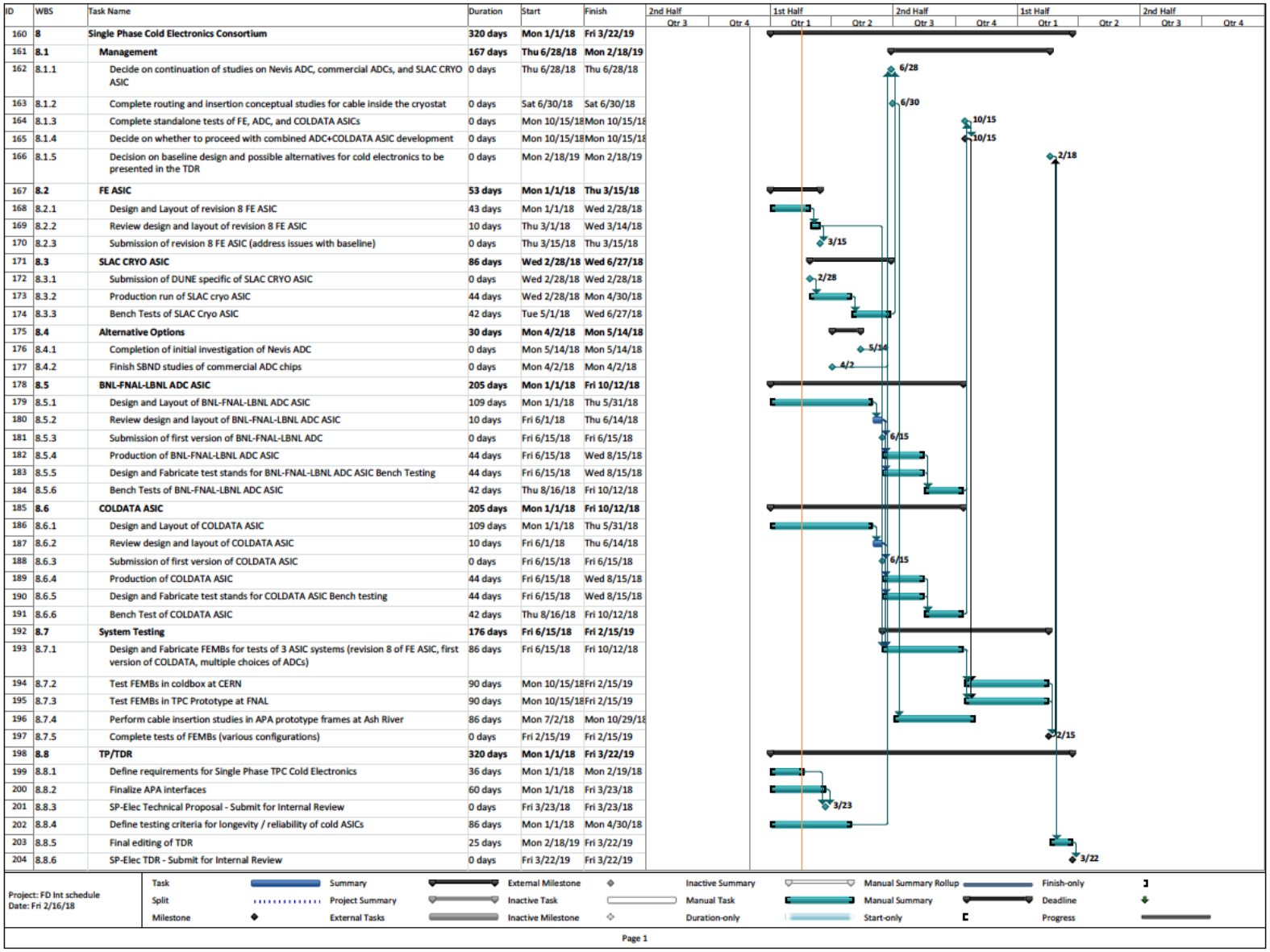
Strategy

- Top Priority is finishing ASIC development:
  - Minor modifications planned to FE ASIC (BNL)
  - Developing a pipelined ADC (LBNL-FNAL-BNL collaboration)
    - Submission in June.
  - Developing COLDATA (FNAL)
    - Submission in June.
  - Supporting adaptation to DUNE of the SLAC “Cryo” ASIC specified originally for nEXO (SLAC).
    - Submission in February.
  - Testing an ADC developed at Columbia U. for ATLAS
  - Monitoring SBND cold tests of a commercial ADC
- The timeline for these developments as well as a description of the types of tests that will be done is contained in a strategy document (DUNE-doc-6658).
- The process we will follow to choose which of these developments to continue is documented (DUNE-doc-7156).

Timeline for Technical Decisions

- Q4 2017: Establish validity of plan to use CERN cold box in electronics decision process (done).
- Q3 2018: Evaluate bench tests of Cryo and ATLAS ADC (decide whether to include in system tests)
- Q3 2018: Commission small TPC with ProtoDUNE electronics (establish validity of use for system tests)
- Q4 2018: Evaluate bench tests of Cold ADC & COLDATA (decide whether to include in system tests)
- Q4 2018 – Q2 2019: Evaluate system tests of new electronics (decide what to include in TDR)

Schedule



ID	WBS	Task Name	Duration	Start	Finish
160	**8**	**Single Phase Cold Electronics Consortium**	**320 days**	**Mon 1/1/18**	**Fri 3/22/19**
161	**8.1**	**Management**	**167 days**	**Thu 6/28/18**	**Mon 2/18/19**
162	8.1.1	Decide on continuation of studies on Nevis ADC, commercial ADCs, and SLAC CRYO ASIC	0 days	Thu 6/28/18	Thu 6/28/18
163	8.1.2	Complete routing and insertion conceptual studies for cable inside the cryostat	0 days	Sat 6/30/18	Sat 6/30/18
164	8.1.3	Complete standalone tests of FE, ADC, and COLDATA ASICs	0 days	Mon 10/15/18	Mon 10/15/18
165	8.1.4	Decide on whether to proceed with combined ADC+COLDATA ASIC development	0 days	Mon 10/15/18	Mon 10/15/18
166	8.1.5	Decision on baseline design and possible alternatives for cold electronics to be presented in the TDR	0 days	Mon 2/18/19	Mon 2/18/19
167	**8.2**	**FE ASIC**	**53 days**	**Mon 1/1/18**	**Thu 3/15/18**
168	8.2.1	Design and Layout of revision 8 FE ASIC	43 days	Mon 1/1/18	Wed 2/28/18
169	8.2.2	Review design and layout of revision 8 FE ASIC	10 days	Thu 3/1/18	Wed 3/14/18
170	8.2.3	Submission of revision 8 FE ASIC (address issues with baseline)	0 days	Thu 3/15/18	Thu 3/15/18
171	**8.3**	**SLAC CRYO ASIC**	**86 days**	**Wed 2/28/18**	**Wed 6/27/18**
172	8.3.1	Submission of DUNE specific of SLAC CRYO ASIC	0 days	Wed 2/28/18	Wed 2/28/18
173	8.3.2	Production run of SLAC cryo ASIC	44 days	Wed 2/28/18	Mon 4/30/18
174	8.3.3	Bench Tests of SLAC Cryo ASIC	42 days	Tue 5/1/18	Wed 6/27/18
175	**8.4**	**Alternative Options**	**30 days**	**Mon 4/2/18**	**Mon 5/14/18**
176	8.4.1	Completion of initial investigation of Nevis ADC	0 days	Mon 5/14/18	Mon 5/14/18
177	8.4.2	Finish SBND studies of commercial ADC chips	0 days	Mon 4/2/18	Mon 4/2/18
178	**8.5**	**BNL-FNAL-LBNL ADC ASIC**	**205 days**	**Mon 1/1/18**	**Fri 10/12/18**
179	8.5.1	Design and Layout of BNL-FNAL-LBNL ADC ASIC	109 days	Mon 1/1/18	Thu 5/31/18
180	8.5.2	Review design and layout of BNL-FNAL-LBNL ADC ASIC	10 days	Fri 6/1/18	Thu 6/14/18
181	8.5.3	Submission of first version of BNL-FNAL-LBNL ADC	0 days	Fri 6/15/18	Fri 6/15/18
182	8.5.4	Production of BNL-FNAL-LBNL ADC ASIC	44 days	Fri 6/15/18	Wed 8/15/18
183	8.5.5	Design and Fabricate test stands for BNL-FNAL-LBNL ADC ASIC Bench Testing	44 days	Fri 6/15/18	Wed 8/15/18
184	8.5.6	Bench Tests of BNL-FNAL-LBNL ADC ASIC	42 days	Thu 8/16/18	Fri 10/12/18
185	**8.6**	**COLDATA ASIC**	**205 days**	**Mon 1/1/18**	**Fri 10/12/18**
186	8.6.1	Design and Layout of COLDATA ASIC	109 days	Mon 1/1/18	Thu 5/31/18
187	8.6.2	Review design and layout of COLDATA ASIC	10 days	Fri 6/1/18	Thu 6/14/18
188	8.6.3	Submission of first version of COLDATA ASIC	0 days	Fri 6/15/18	Fri 6/15/18
189	8.6.4	Production of COLDATA ASIC	44 days	Fri 6/15/18	Wed 8/15/18
190	8.6.5	Design and Fabricate test stands for COLDATA ASIC Bench testing	44 days	Fri 6/15/18	Wed 8/15/18
191	8.6.6	Bench Test of COLDATA ASIC	42 days	Thu 8/16/18	Fri 10/12/18
192	**8.7**	**System Testing**	**176 days**	**Fri 6/15/18**	**Fri 2/15/19**
193	8.7.1	Design and Fabricate FEMBs for tests of 3 ASIC systems (revision 8 of FE ASIC, first version of COLDATA, multiple choices of ADCs)	86 days	Fri 6/15/18	Fri 10/12/18
194	8.7.2	Test FEMBs in coldbox at CERN	90 days	Mon 10/15/18	Fri 2/15/19
195	8.7.3	Test FEMBs in TPC Prototype at FNAL	90 days	Mon 10/15/18	Fri 2/15/19
196	8.7.4	Perform cable insertion studies in APA prototype frames at Ash River	86 days	Mon 7/2/18	Mon 10/29/18
197	8.7.5	Complete tests of FEMBs (various configurations)	0 days	Fri 2/15/19	Fri 2/15/19
198	**8.8**	**TP/TDR**	**320 days**	**Mon 1/1/18**	**Fri 3/22/19**
199	8.8.1	Define requirements for Single Phase TPC Cold Electronics	36 days	Mon 1/1/18	Mon 2/19/18
200	8.8.2	Finalize APA interfaces	60 days	Mon 1/1/18	Fri 3/23/18
201	8.8.3	SP-Elec Technical Proposal - Submit for Internal Review	0 days	Fri 3/23/18	Fri 3/23/18
202	8.8.4	Define testing criteria for longevity / reliability of cold ASICs	86 days	Mon 1/1/18	Mon 4/30/18
203	8.8.5	Final editing of TDR	25 days	Mon 2/18/19	Fri 3/22/19
204	8.8.6	SP-Elec TDR - Submit for Internal Review	0 days	Fri 3/23/19	Fri 3/22/19

Milestones

- Q4 2017: Cold box tests (at CERN) of ProtoDUNE-SP electronics (baseline) – Done.
- Q1 2018: Submission of SLAC Cryo ASIC
- Q2 2018: Technical Proposal draft complete, submission of Cold ADC & COLDATA
- Q3 2018: First operation of full ProtoDUNE-SP system
- Q4 2018: Tests of ProtoDUNE electronics with a small TPC (baseline)
- Q1 2019: Tests of new electronics in CERN cold box and with a small TPC
- Q2 2019: Technical Design Report draft complete.

Risks and Concerns

- DUNE-doc-6877 identifies 16 significant risks
- My top concerns:
  - Unacceptable noise: We believe low noise can be achieved with careful design and strict observance of grounding and shielding rules; ProtoDUNE results will be crucial to making this case.
  - Timely completion of ASIC development: It is essential that at least one of the ASIC options demonstrate good performance in this design cycle.

LBNC Recommendations

- 2017-148: “By the end of November 2017, present a detailed plan for DUNE ADC development as well as testing and evaluation. This should include intermediate technical milestones over the next 9 months for the ADC development.”
  - This was not done by the end of November 2017, but is now complete & contained in DUNE-doc-6658 (Strategy) and DUNE-doc-7156 (ASIC Decision Process).
- 2017-149: “At the next LBNC meeting, provide updates on the progress of all ADC options as well as the overall plan and timeline to work towards the TDR.”
  - This will be presented in tomorrow’s breakout session.