Update on Detector Imperfection Studies

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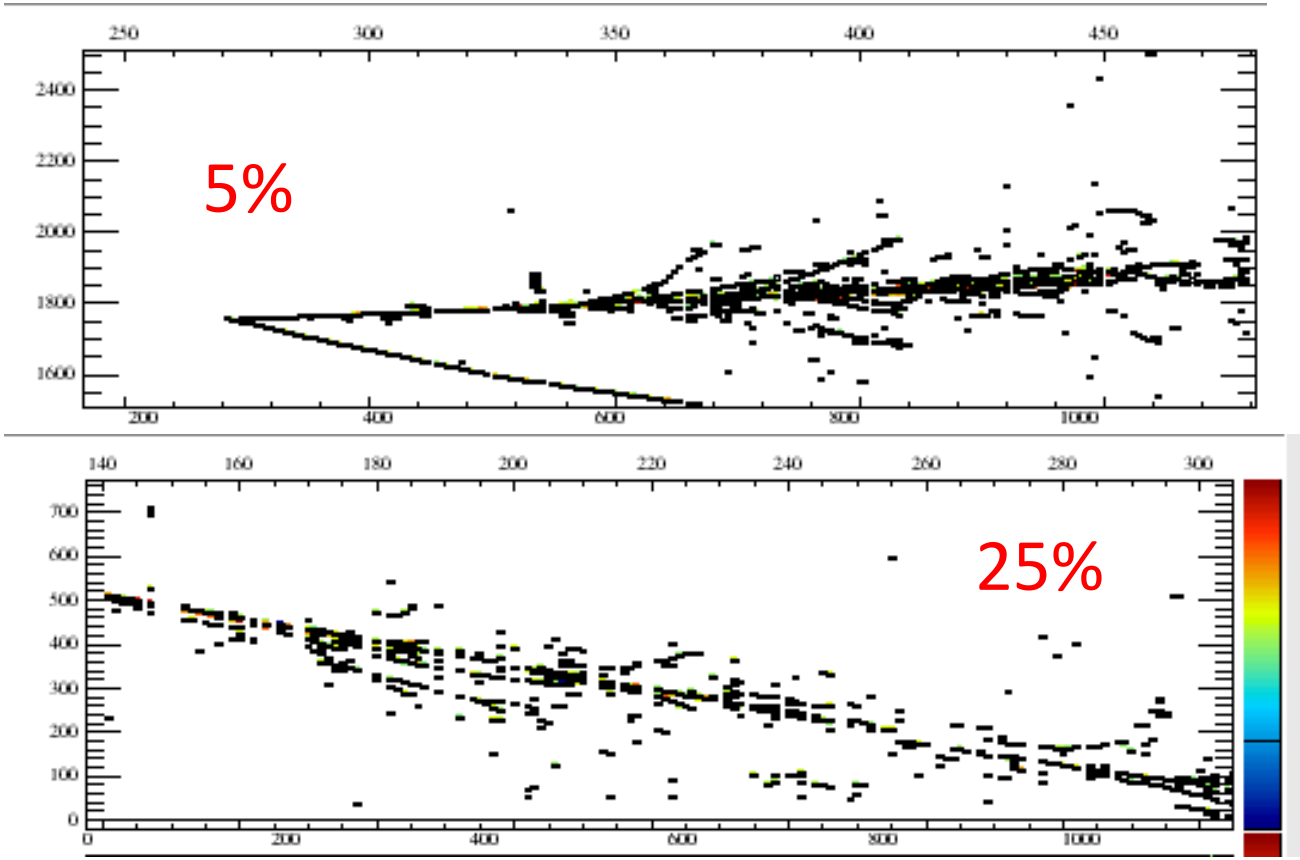
Long-Baseline Meeting

February 26, 2018

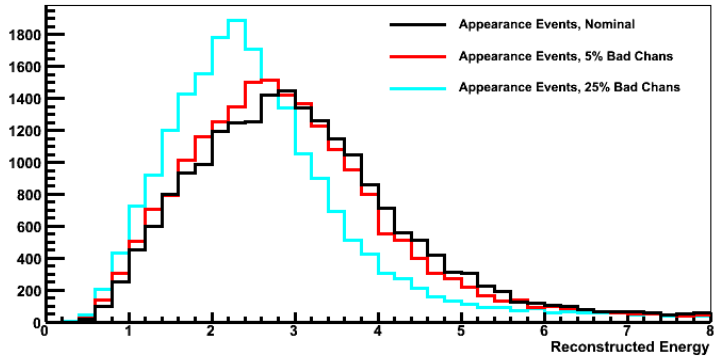
Random Bad Channel Simulation

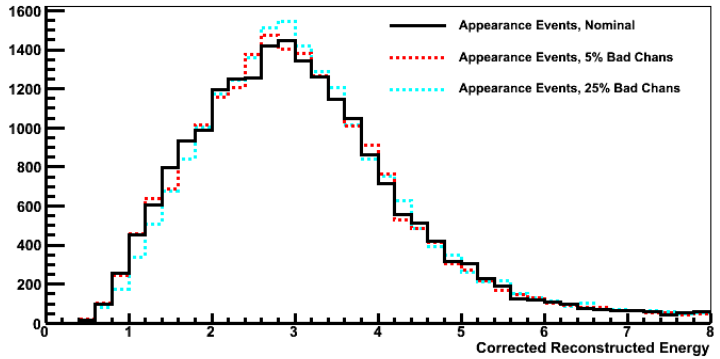
- MCC 10.1 for all variations
- Randomly remove 5% or 25% of channels (Backhouse)



Energy Reconstruction

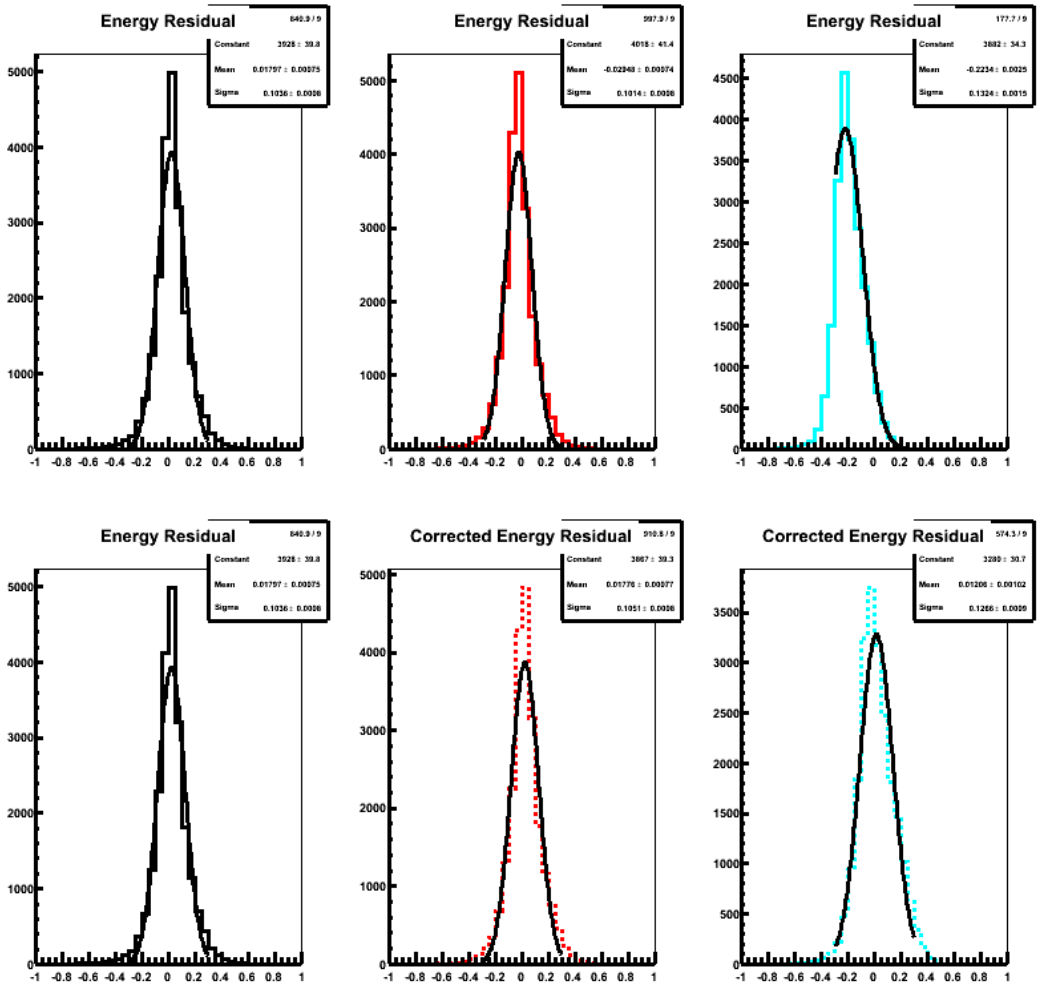
- Run only nominal energy reconstruction, which is calorimetric for EM showers
  - Expect to be missing ~5% or 25% of energy
  - Scaling reconstructed energy by 1.05 or 1.25 approximately corrects back to nominal reconstructed energy as expected
- Note: scaling performed at plot level only, does not impact PID variable





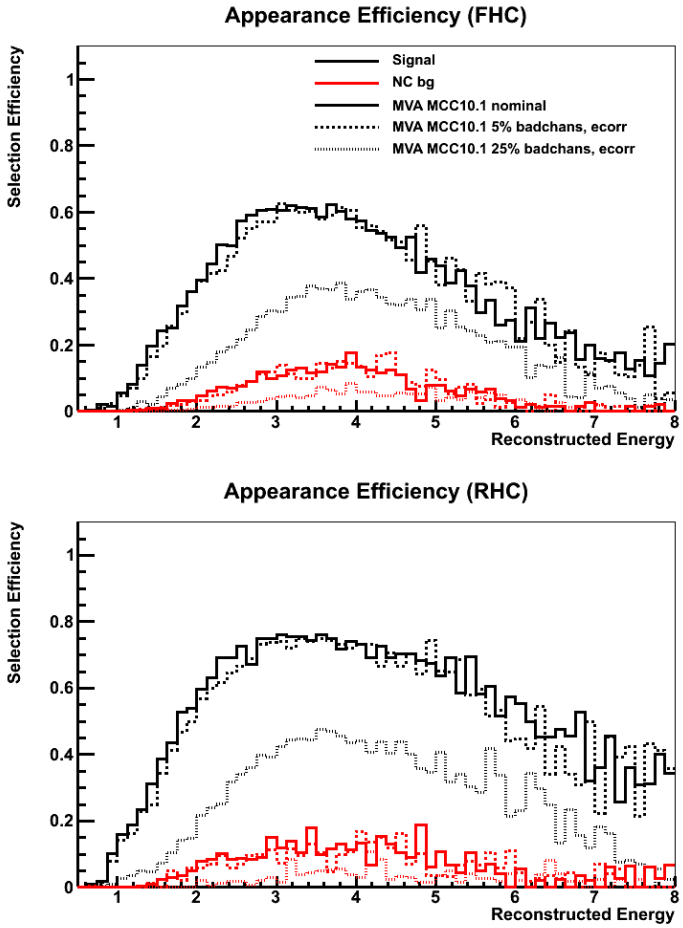
Energy Resolution

- Check fractional energy residuals for each case
- See bias as expected in uncorrected residuals
- Nominal resolution similar to that reported by N. Grant
- See some increase in resolution for 25% missing channels case



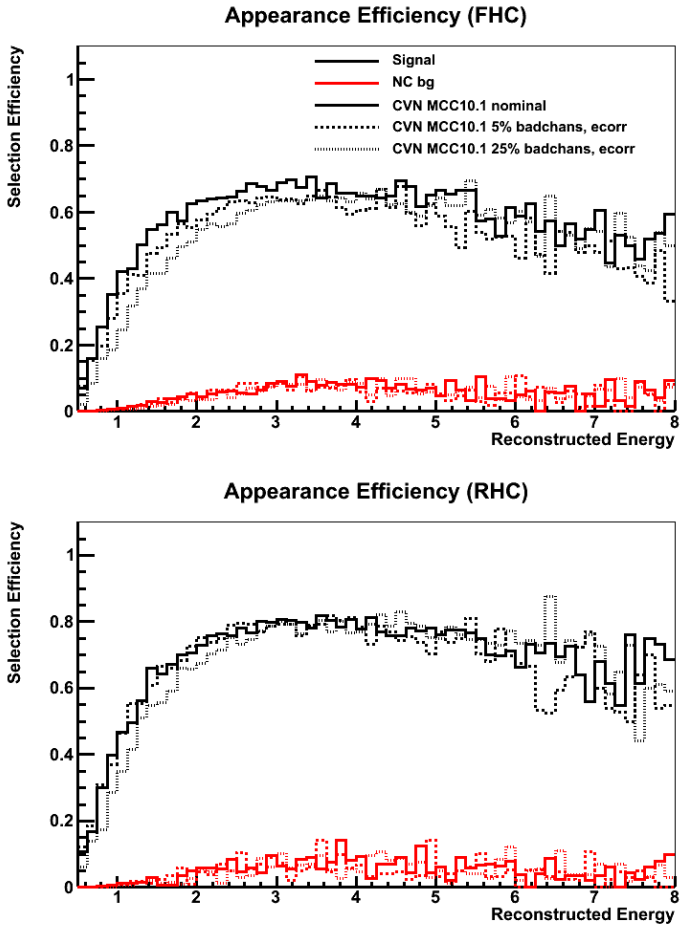
MVA Efficiency

- Efficiency for true ν_e appearance and NC bg events as a function of corrected reconstructed energy using nominal PID cut at 0.8
- MVA efficiency drops dramatically with 25% missing channels as expected
  - Is the reconstruction failing here? Need to look at variables going in to MVA selection
- NC efficiency also drops – maybe cut needs to be re-tuned?



CVN Efficiency

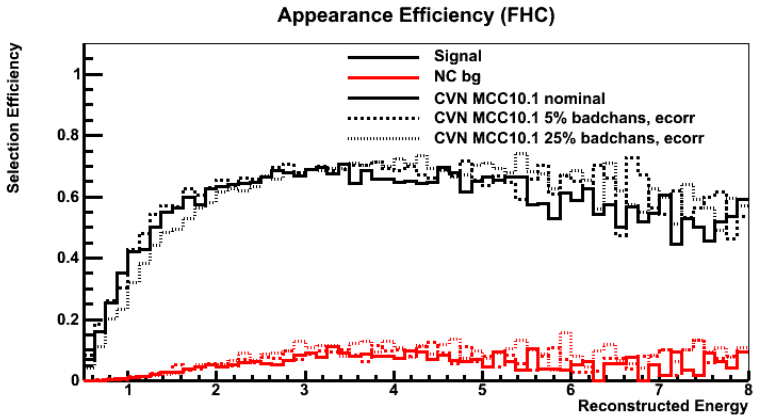
- Efficiency for true ν_e appearance and NC bg events as a function of corrected reconstructed energy using nominal PID cut at 0.7
- CVN efficiency does not degrade nearly as much - seems counter-intuitive. Do we believe this result?
- Again, do we need to re-tune cut?

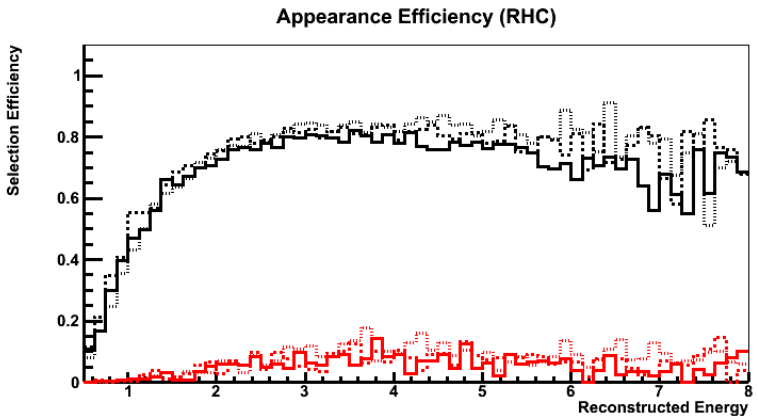


PID Cut Tuning

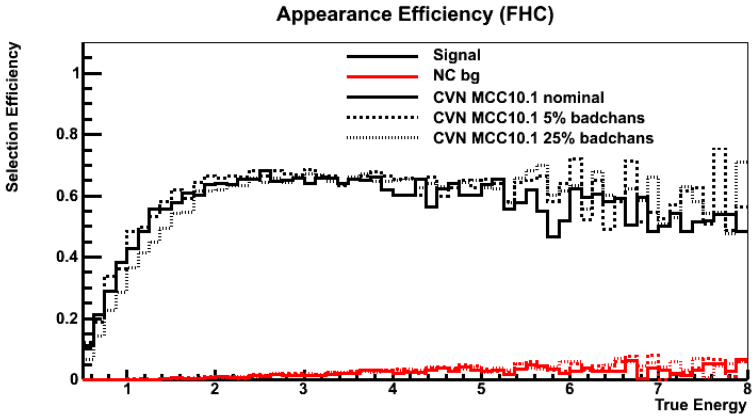
- Method:
  - Set numu PID cut at 0.5 (no tuning)
  - Require numu PID < 0.5 and nue PID > x for nue event to be selected (and inverse for numu events)
  - Scan through nue PID cut values in steps of 0.05, starting at 0.0
  - Evaluate CPV sensitivity at $\delta_{CP} = -\pi/2$
  - Define optimum cut value as the one before sensitivity starts to decrease (so might miss 2nd optimum value if sensitivity is not monotonic above and below optimum)
- Resulting optimized nue PID cut (CVN)
  - Nominal: 0.7
  - 5% bad channels: 0.65
  - 25% bad channels: 0.6
- With more bad channels, prefer cut with slightly higher acceptance such that signal efficiencies are more similar than with un-tuned cuts
  - Observe no major increase in background

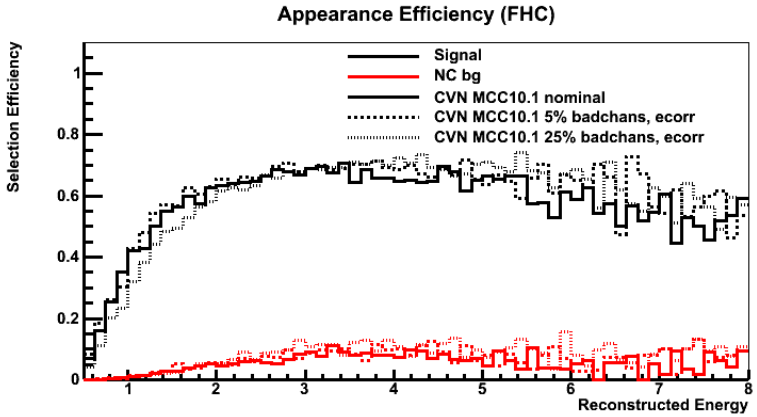
Efficiencies with PID cut at optimized value for each sample

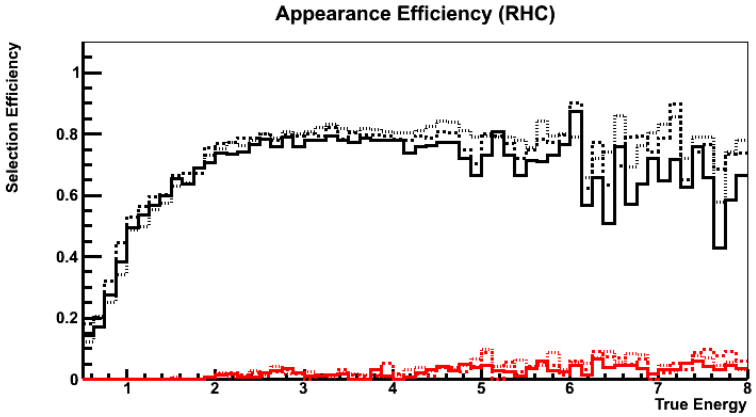


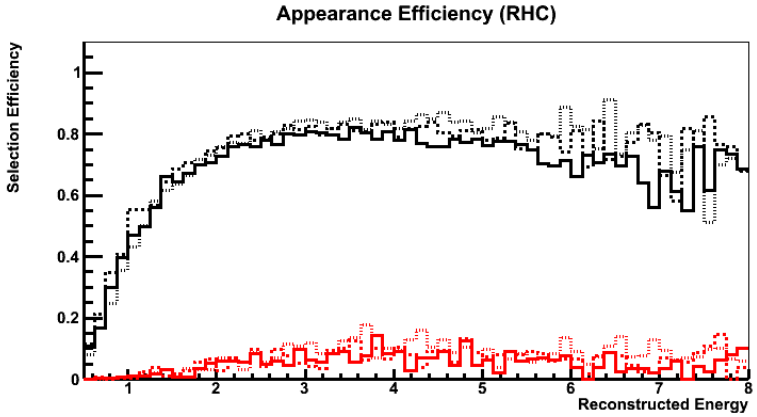


Efficiency vs True Energy









True energy

Compare corrected reco energy

Preliminary Conclusion

- CVN does appear to be much less impacted by 25% dead channels than we anticipated
- Maybe this makes sense
  - Bad channels randomly distributed
  - Basic differentiation between showers and tracks should not be impacted by this – a shower with a bunch of missing hits still looks very different by eye than a track with a bunch of missing hits
  - For background rejection: radiation length is 14 cm and dE/dx for e/g separation uses 2-3 cm of track while wire pitch is 5 mm
    - Only consecutive bad channels near the vertex would be expected to have dramatic impact – may be that even with 25% bad channels randomly distributed, this doesn't happen very often
- Next steps to validate results and extend study
  - Plot efficiency as function of other variables
  - More realistic treatment of bad channels (clustered by groups of wires, ASICs, FEMBs, etc) - see following pages for status

Cold Electronics Design

- 16 channels per ASIC
- 8 ASICs per board = 128 channels per board
- 20 boards per APA = 2560 channels per APA
- Each board serves a mix of U, V, W wires with non-trivial mapping… more on this next slide

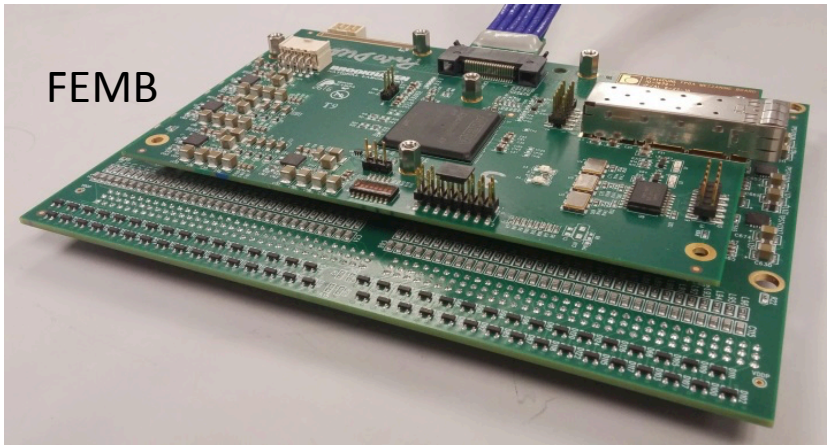


Table 2.6: Electronics components and quantities

Element	Quantity	Channels per element
TPC	1	15,360
APA	6	2,560
Front-End Mother Board (FEMB)	120, 20 per APA	128
FE ASIC chip	120 × 8, 8 per FEMB	16
ADC ASIC chip	120 × 8, 8 per FEMB	16
FEMB FPGA	120, 1 per FEMB	128
Cold cable bundles	120, 1 per FEMB	128
Signal flange	6, 1 per APA	128 × 20 (i.e., 2,560)
CE feedthrough	6, 1 per APA	128 × 20
Warm interface boards (WIB)	30, 5 per APA	(128 × 20) /5 (i.e., 512)
Warm interface electronics crates (WIEC)	6, 1 per APA	128 × 20
Power and timing cards (PTC)	6, 1 per APA	128 × 20
Passive backplane (PTB)	6, 1 per APA	128 × 20
LV power mainframe	2	7,680
LV supply modules	6, 1 per APA	128 × 20
Wire-bias mini-crate	2	7,680
Wire-bias supply modules	6, 1 per APA	128 × 20

Channel Mapping (protoDUNE)

- See DocDB 4064
- Description is for protoDUNE; can assume same for DUNE FD for now
- 40 U, 40 V and 48 W channels per board
- Mapping to LArSoft channel numbers not obvious and no service exists yet

ASIC:	1	2	3	4	5	6	7	8
ch00	u19	u09	w14	w02	u29	u39	w26	w38
ch01	u17	u07	w16	w04	u27	u37	w28	w40
ch02	u15	u05	w18	w06	u25	u35	w30	w42
ch03	u13	u03	w20	w08	u23	u33	w32	w44
ch04	u11	u01	w22	w10	u21	u31	w34	w46
ch05	v19	v09	w24	w12	v29	v39	w36	w48
ch06	v17	v07	v12	v02	v27	v37	v22	v32
ch07	v15	v05	v14	v04	v25	v35	v24	v34
ch08	v13	v03	v16	v06	v23	v33	v26	v36
ch09	v11	v01	v18	v08	v21	v31	v28	v38
ch10	w23	w11	v20	v10	w35	w47	v30	v40
ch11	w21	w09	u12	u02	w33	w45	u22	u32
ch12	w19	w07	u14	u04	w31	w43	u24	u34
ch13	w17	w05	u16	u06	w29	w41	u26	u36
ch14	w15	w03	u18	u08	w27	w39	u28	u38
ch15	w13	w01	u20	u10	w25	w37	u30	u40

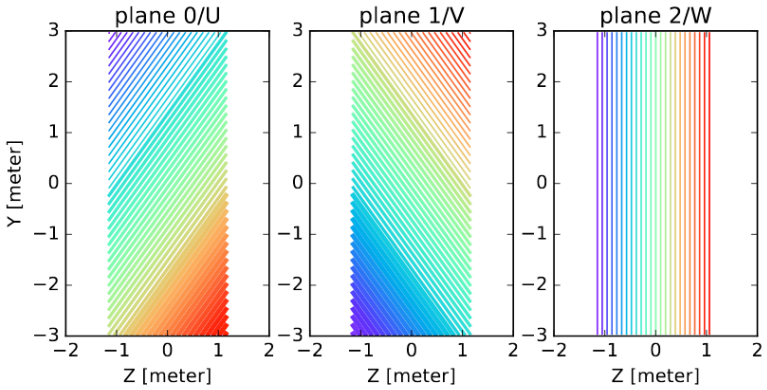


Figure 5: The wire (segments) for each wire plane on one face of one APA for protoDUNE. Increasing line width indicates increasing **segment number** $\in$ (0, 1 or 2). The color indicates increasing **wire index** from blue to red. Only one of every twenty wires are shown. The Y coordinate points opposite of gravity. The unlabeled X coordinate runs into the page and is counter to the drift direction. Z follows from the right-hand-rule.

Simulation Status

- Chris has implemented something like the mapping from the previous slide
- Now have option to make x% of channels bad grouped by "channel", "chips", "boards", "APAs"
  - Channel = random study we've already looked at
- See https://cdcvs.fnal.gov/redmine/projects/dunetpc/repository/revisions/develop/entry/dune/DetectorVariations/RandomChannelStatusService_service.cc
- Possibly not perfect representation of actual mapping, but should be useful for a first pass
- MC not yet generated?

Other Minor Updates

- Discussed wire-based imperfections (eg broken/shorted wires) with APA experts
  - No obvious scale for problem – could be single channels up through hundreds of wires – probably consider the full-APA removal (already in Chris' options) as covering worst case
- Working on configuration for reduced (250 V/cm) E-field after request from Bo and HV experts to study impact of lower field