## **TDR/TP Preparation**

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## Introduction

- DP-electronics Consortium is responsible for TDR Volume 4C
  - Editors: Jaime Dawson (APC), VG (IPNL)
- Technical Proposal (TP) is basically the short version of TDR
  - Rescaling TDR to TP
    - Volume (150 200 page) → Chapter (30 40 pages)
    - Chapters → Sections
- TP should have the same structure in terms of sections as TDR
- The TeX source of the entire TP (also TDR) is publically available on DUNE github (<a href="https://github.com/DUNE/Technical-Proposal">https://github.com/DUNE/Technical-Proposal</a>)



## **Dates**

From TDR planning document

May-19:

Jun-19:

Jul-19:

### 4. Timeline and Milestones

There are number of assumed dates that frame the programme of work:

LBNC review of TDR

CIC	are number	of assumed dates that frame the programme of work.
•	Oct-17:	Editors of TDR volumes appointed
•	Nov-17:	TP/TDR Kick-off meeting – outline of contents
•	Dec-17:	Complete tables of contents of TDR and TP (section heading level)
•	Apr-18:	Complete drafts of the TP volumes Next milestone
•	May-18:	Final version of the TP submitted to the LBNC
•	Jul-18:	LBNC review of the TP
•	Feb-19:	First drafts of all TDR volumes Draft of TDR
•	Mar-19:	TDR internal review
•	Apr-19:	Final version of TDR submitted to the LBNC

Finalize response to questions from LBNC

Cost appendix submitted to RRB Cost Scrutiny Group

DUNE

# Planning for Technical Proposal

Dates from T. Bolton and S. Zeller the overall editors of the TP volumes appointed by the spokespersons

- January 12: Finalize table of contents (section heading level)
- February 23: First rough draft of TP due
- March 16: Second rough draft of TP due
  - Drafts will be sent to external reviewers for comment
- April 13: Final version of TP due
- May 11: TP submitted to LBNC

Start filling sections as much as possible from the existing material

- DUNE CDR
- <u>Document prepared</u> for DAQ workshop
- Interface document for DP-Electronics DAQ
- Material prepared for the LAr-Proto paper



## **TP Outline**

Total should be ~30 pages

1	TPO	C Electronics 2
	1.1	TPC Electronics System Overview
		1.1.1 Introduction
		1.1.2 Design Considerations
		1.1.3 Scope
	1.2	TPC Electronics System Design
		1.2.1 Cryogenic Analog FE Electronics
		1.2.2 Signal Feedthrough Chimneys
		1.2.3 Low-voltage Power Supplies for FE Electronics
		1.2.4 Network-based uTCA Architecture
		1.2.5 Digital AMC Electronics
		1.2.6 Timing Distribution
		1.2.7 Electronics for Light Readout
	1.3	Production and Assembly
		1.3.1 Cryogenic Analog FE Electronics
		1.3.2 Signal Feedthrough Chimneys
		1.3.3 Timing System and uTCA
		1.3.4 Charge Readout Electronics
		1.3.5 Light Readout Electronics
		1.3.6 Quality Assurance
	1.4	Interfaces
		1.4.1 Cryostat and Cryogenics
		1.4.2 Slow Control System
		1.4.3 DAQ System
		1.4.4 Photon Detection System
	1.5	Installation, Integration and Commissioning
		1.5.1 Transport and Handling
		1.5.2 Signal Feedthrough Chimneys
		1.5.3 uTCA crates
		1.5.4 Integration within DAQ
		1.5.5 Integration with Photon Detection System
		1.5.6 Calibration
	1.6	Quality Control
		1.6.1 Protection and Assembly (Local)
		1.6.2 Post-factory Installation (Remote)
	1.7	Safety
	1.8	Organization and Management
		Organization and Management
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		1.8.3 WBS and Responsibilities
		1.8.4 High-level Cost and Schedule



1	TPC		2
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		1.2.2 Signal Feedthrough Chimneys	5
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			5
		1.2.5 Digital AMC Electronics	5
			5
			5
	1.3	Production and Assembly	5
			5
			5
		1.3.3 Timing System and uTCA	5
			5
			5
			5
	1.4	Interfaces	5
		1.4.1 Cryostat and Cryogenics	<u>5</u>
			5
			5
	1.5	Installation, Integration and Commissioning	5
			5
			5
			5
		1.5.4 Integration within DAQ	5
		1.5.5 Integration with Photon Detection System	5
		1.5.6 Calibration	5
	1.6	Quality Control	5
			5
		1.6.2 Post-factory Installation (Remote)	5
	1.7		5
	1.8	Organization and Management	
			5
			5
			5
		1.8.4 High-level Cost and Schedule	5

Most of the material already exists in various documents

Sections that require most new writing:

- Production and Assembly
- Interfaces
  - There is a DAQ Interface document written already
- Installation, Integration and Commissioning

Most of the material also exists: WBS document

Basic numbers are well defined (caveat: number of ch for LRO)

→ baseline cost model



#### Components for a 10 kton dual-phase module

(list based on current 6x6x6 design, possible optimizations on channels density increase)

Total number of charge readout channels: 153600

- Cryogenic ASICs (16 ch): 9600
- Cryogenic FE cards (64 ch): 2400



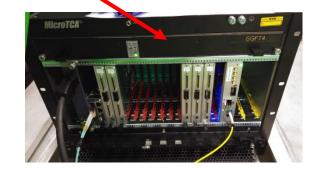
- AMC cards (64 ch): 2400
- uTCA White-Rabbit cards: 240
- uTCA crates (including MCH,PU,FU): 240
- 10 Gbe optical links to backend: 240
- VHDCI cables (32 ch) 4800



White-Rabbit switches (18 ports): 16









## Conclusions

- Produce the first draft of the TP document by the end of Feb
- Final version of TP is to be submitted to LBNC in May
- Structure adopted for TP should be extendable to TDR

