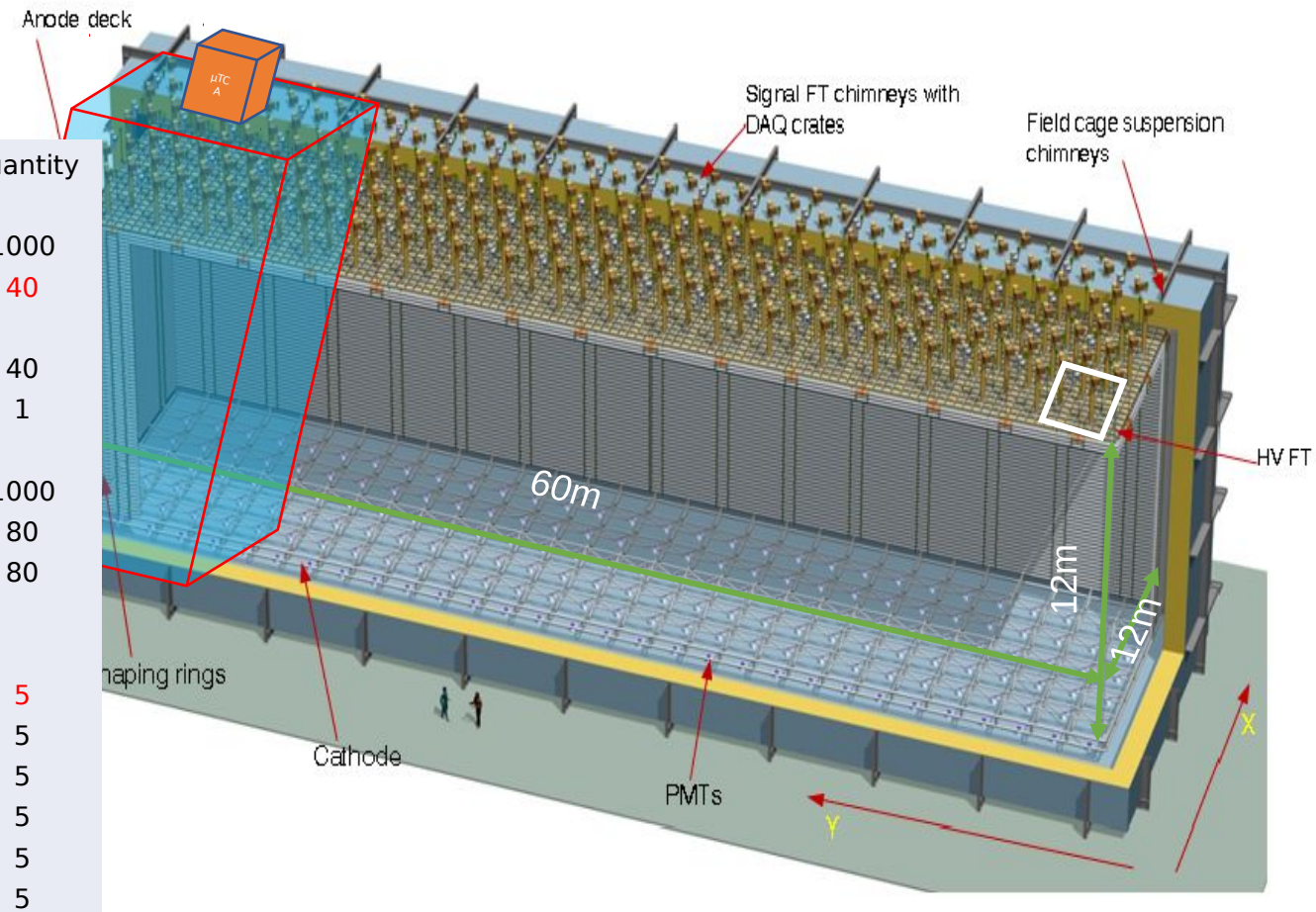
Dual-Phase: Light Read-Out

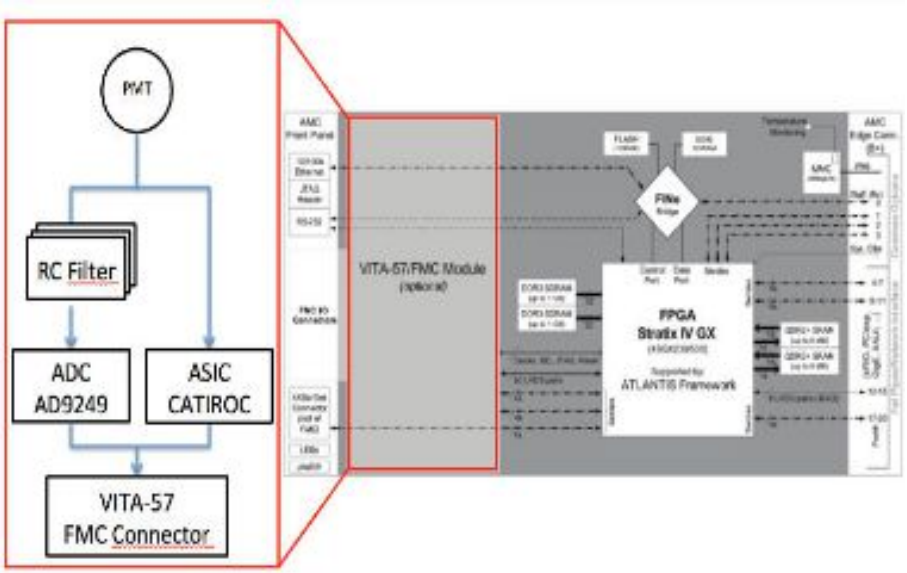
~720 PMTs (1 PMT/ m2)

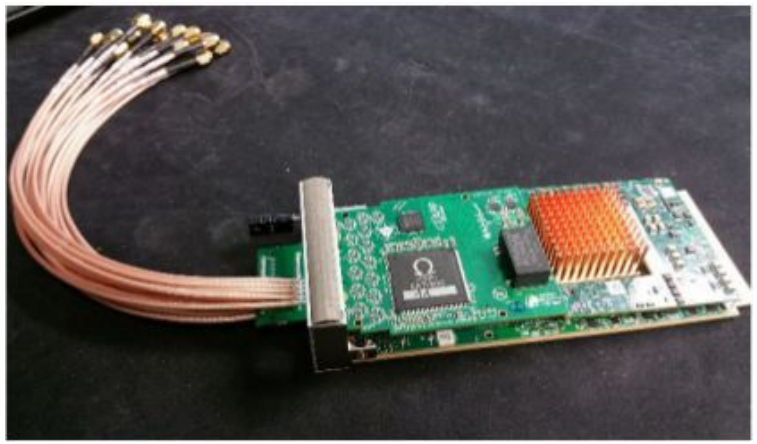
Item	Details	Quantity
PMTs		1000
FE-Cards	32 channels	40
	Components	
	printed cirquid	40
	PCB masques	1
	Mounting of components	
	Cabels SMA	1000
	Catyroc	80
	ADC	80
micro-TCA crate		5
	MCH	5
	Power Module	5
	XAUI (x4)	5
	Uplink SFP+	5
	Uplink SFP+850	5
White Rabbit		5
	SPEC Card	5
	FMC DIO	5
	SFP (x2)	5



CABLING
RG393 (0.4 dB/100 feet @ 400 MHz)
RG303 (8.6 dB/100 feet @ 400 MHz)
RG316 (20 dB/100 feet @ 400 MHz)

LRO Card in brief





Development for protoDUNE-DP consists of a daughter board (IPNL, LAPP, Omega, APC) and a commercial motherboard.

16 channels

Anti-aliasing low pass filter

ADC: AD9249 65 MHz, 14 bits provides waveform with a window of ± 4ms around beam trigger down-sampled to 400 ns

ASIC: CATIROC

Provides auto-triggered channel-wise Q, t and generates light trigger

More hardware details can be found in:
DUNE FD DAQ Workshop Oct 30-31
https://indico.fnal.gov/event/15366/session/4/contribution/30/material/slides/1.pdf

ADC & Catiroc

ADC

- Digitisation at 25ns (possibility to read out 25ns for special events/runs)
- Downsampled to 400ns (same as Charge ReadOut).
- 16 channel, 2Vp-p, 14 bit [DNL <0.6 LSB, INL <0.9 LSB]
- Possibility of online processing in FPGA

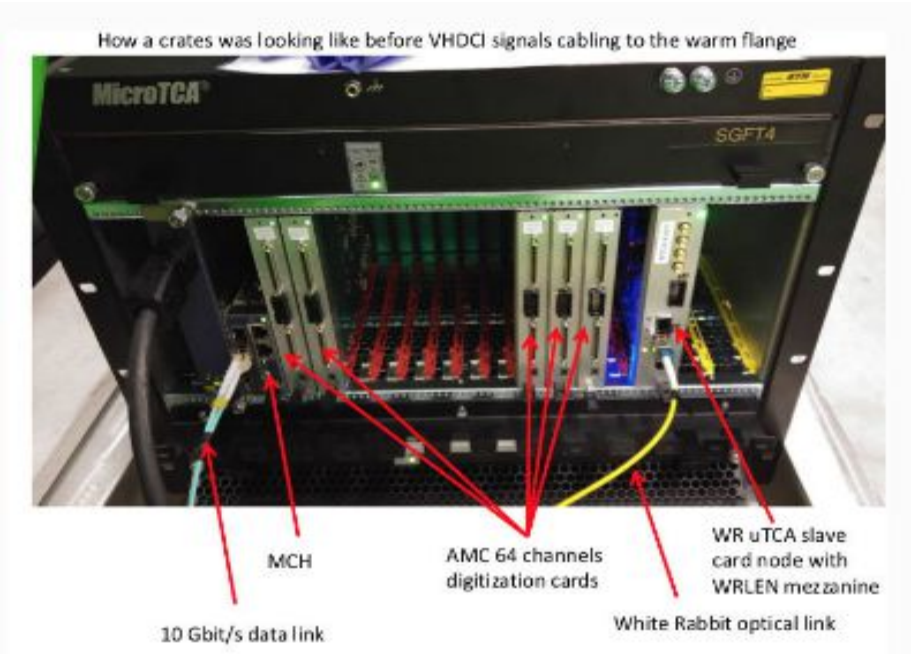
System is flexible
Cross-calibration ADC-CatiROC
ASIC gives early and precise channelwise Q,T
ADC waveform

CatiROC (Omega)

- 16 channel for negative pulses
  - High/Low noise amplifiers for small and large signals (charge precision ~30 fC)
- Variable 8-bit gain/amplifier/channel
  - Preamp followed by 2 variable slow shapers to measure up to 50 pC
- Time: coarse + fine timing
  - 10 bit Wilkingson ADC to convert charge and fine time at 160 MHz
  - Deadtime ~5 us
  - 2 x 16 effective channels (2 capacitors)
- Fast shaper/channel followed by a discriminator* for auto-triggering
  - Timestamp of 26 bits course time

* One common, leading edge 10 bit threshold

Global Scheme



LRO Card fully integrable into existing framework (Charge ReadOut)

uTCA standard

Synchronised channels per card

AMC motherboard takes clock through uTCA backplane

Crate Sync – dedicated White Rabbit, uTCA slave node acts a sync receiver distributing clocks to the back plane

Data readout through data link

Plan

NOW →	Firmware development of daughter board
April 2018	Testing with pulse generator/PMT signals
June-Oct 2018	Installation protoDUNE DP
June 2018-Oct 2019	Development of DUNE card

Prospectives

Merger of Daughter and IPNL developed Mother board

- AdvancedMC (AMC) doublewidth slots
- 32 channel (2 ADC, 2 ASICs)
- Lower spec FPGA

- 32 channels * 11 cards = 352 channels per uTCA crate
- Continuous read-out (as for Charge)
- Increase Dynamic Range of ADC (currently ± 1V, include DC offset)
- Pulse processing on FPGA

Interface PhotoDetection

- **Number of readout channels** (to be determined by simulations and/or measurements). Simulations must be complete and include attenuation, Rayleigh scattering, cathode transparency, PDE of coated PMTs.
- **Dynamic range** at the input to Front-End
- Deep understanding of **PMT characteristics**: saturation, recovery time, ringing, pre-, delayed and after pulsing, since this impacts the FE electronics (e.g. trigger scheme, dead time)
- **Ringing** should be suppressed at the level of the PMT base to avoid creating false multiple events, which will result in an increased dead-time and the generation of spurious LRO triggers.
- Definition of connectors to be used at the FE input panel.