Discussion of TP Draft

Current State of the Outline

5	1 TP	C Elect	ronics 1		
6	1.1	TPC E	Electronics System Overview		
7		1.1.1	Introduction		
8		1.1.2	Design Considerations		
9		1.1.3	Scope		
10	1.2	TPC E	Electronics System Design		
11		1.2.1	Cryogenic Analog FE Electronics		
12		1.2.2	SFT Chimneys		
13		1.2.3	Digital AMC Electronics for Charge Readout		
14		1.2.4	Electronics for Light Readout		
15			Waveform branch		
16			CatiROC branch		
17		1.2.5	Network-based uTCA Architecture		
18		1.2.6	Timing Distribution		
19	1.3	Produc	ction and Quality Assurance		
20		1.3.1	Cryogenic Analog FE Electronics		
21		1.3.2	SFT Chimneys		
22		1.3.3	Timing System and uTCA		
23		1.3.4	Charge Readout Electronics		
24		1.3.5	Light Readout Electronics		
25	1.4	Interfa	ces		
26		1.4.1	CRP and Photon Detection System		
27		1.4.2	DAQ System		
28		1.4.3	Cryostat and Cryogenics		
29		1.4.4	Slow Control System		
30	1.5	Installa	ation, Integration and Commissioning		
31		1.5.1	Transport and Handling		
32		1.5.2	SFT Chimneys		
33		1.5.3	Digital uTCA crates		
34		1.5.4	Integration within DAQ		
1		1.5.5	Integration with Photon Detection System		
2		1.5.6	Comissioning		
3	1.6	Risks and Vulnerabilities			
4	1.7		ization and Management		
5		1.7.1	Dual-Phase TPC Electronics Consortium Organization		
6		1.7.2	Planning Assumptions		
7		1.7.3	WBS and Responsibilities		

~60% devoted to introduction and description of the system design This is in-line with the guidelines given by the TP head editors (shown in the next few slides)

Some of the sub-sections shown in the original outline have disappeared:

- Too short and merged with other subsections
- Removed because they were redundant

Added section on risks and vulnerabilities as requested by the TP head editors

The overall length is OK (~30 pages)

Introductions are important

- We cannot be complacent!
- Take the attitude that LBNC will be a tough and skeptical review committee.
- What is the very purpose of sub-system and its parts? Be clear.
 Example:
 - Photon detection system.
 - Slow monitoring.
 - Calibration.
- Why have certain design decisions been made and retained, even if circumstances have changed. Example:
 - Wrapped APA.
 - Cold electronics.



The TP is not an updated CDR

- Heading towards the baseline design, the TDR
- Options should be narrowing.
- Designs should be flowing from requirements.
- Design performance should be demonstrable from simulation.

In this sense, we tried to limit the discussion to the baseline design only:

- The possibility of increasing the channel density of AMCs is however briefly mentioned and motivated by cost reductions
- Increasing the strip length is not discussed (anyway need to interface with the CRP consortium for that), since it goes in the direction of "less conservative" (less readout channels) design. Moreover there are still things to be understood
- Of course, one had to make some assumptions on the number of the light readout channels. Same area coverage is assumed (=720 channels) as in the ProtoDUNE-DP

Don't duck vulnerabilities

- Call them out. Examples:
 - Cannot achieve nominal HV?
 - Single point failures in HV?
 - Noise impacts on DAQ.
 - Dead electronics channel impacts.
 - Inaccessibility: "unmanned spaceship" analogy.
 - 20-40 years of operation.
- Discuss trade-offs, mitigation. Examples:
 - Electric field vs. purity.
 - Dead channel model, and tolerance of performance.

Additional guidance received

- Do not refer to docdb documents
 - This was motivated as the TP should be like a publication style document: self-contained and uploadable on arxiv
 - It is not clear how this is to be avoided though and we kept the references to all relevant docdb documents at least for now
- Costs and schedule will be developed in separate documents
 - We just say a few words and give some key milestones
- Do not reproduce the WBS tables
 - We state that these will come as separate documents

Relevant deadlines

- January 12: Finalize table of contents (section heading level)
- February 23: First rough draft of TP due
- March 16: Second rough draft of TP due
 - Drafts will be sent to external reviewers for comment
- April 13: Final version of TP due
- May 11: TP submitted to LBNC

The draft has been committed to the DUNE git

March 16 is the next relevant deadline. By this point everyone in the consortium should be happy with the draft and we will have incorporated any additional comments from the head editors After this the draft will be under review by "external" referees

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8		1.7.4	High-level Cost and Schedule			

The sections on *Production* and *Installation* ... perhaps not as too detailed.
But there is certainly still room to expand (i.e., the number of pages is not too high) if there are specific items to be added

In summary ...

- Please start reading the draft and send us your comments in advance of the March 16 deadline
- Please use the uploaded draft document to refer to page – line number for specific comments
 - The version on the git may have changed in the meantime
- Otherwise send us a pdf file with inserted comments
- The document uploaded on indico is only the chapter concerning the DP electronics
 - Both TP volumes could be found on git. It is important to also check the other chapters especially the ones with significant interface overlap (e.g., CRP, DAQ, PD DP)