Development of Cold Front-End ASIC for DUNE SP LArTPC

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Outline

- Development of P3 Cold Front-End ASIC
  - Front-End (FE) ASIC overview
  - Performance of P2 FE ASIC in ProtoDUNE-SP
  - Development of a new baseline generation for collection mode
  - Default gain setting
  - Layout details

- Fabrication and Evaluation of P3 FE ASIC

- Summary

- WIB → DAQ Fiber Test
Front End ASIC
Continuing development toward a robust design adaptable to future design rule and process technology changes

Layout & functionality:

- 16 channels (details next slide)
- band-gap referenced biasing circuits
- temperature sensor (~ 3mV/°C)
- integrated 6-bit pulse generator
- 144 configuration registers, SPI interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- Designed for room (300K) and cryogenic (77K) temperature
- Technology CMOS 0.18 µm, 1.8 V, 6M, MIM, SBRES

*original layout
Dual stage charge amplification, high order filter
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC (charge 55, 100, 180, 300 fC)
- Adjustable filter time constant – peaking time 0.5, 1, 2, 3 µs
- Selectable collection / non-collection mode (baseline 250, 900 mV)
- Selectable charge amplifier coupling (AC-DC)
- Programmable bias current: 100 pA, 500 pA (default); 1 nA, 5 nA (*)

(*) a high value of bias current is not intended to use in order not to increase the parallel noise

15,360 channels of P2 FE ASIC is being used to instrument ProtoDUNE-SP
Highlight of Cold Electronics Performance in ProtoDUNE-SP

- With drift 180kV and nominal bias voltages
  - 99.74% (15,320 of 15,360) of TPC channels are active regardless of noise performance
    - Only 4 inactive FE channels, others can be attributed to TPC etc.
  - 92.83% (14,259 of 15,360) of TPC channels are good with excellent noise performance (ENC < 800e-)
    - A probable cause of the higher noise is from other TPC instrumentation, to be studied.

- Noise performance with drift and bias on
  - ENC of collection (X) plane (5,473 of 5,760 channels): 565 ± 60 e-
  - ENC of induction (V) plane (4,347 of 4,800 channels): 662 ± 56 e-
  - ENC of induction (U) plane (4,439 of 4,800 channels): 651 ± 54 e-

- Uniform gain measured by on-board calibration pulser
  - Inverted gain of collection (X) plane: 135 ± 6 e-/ADC, INL ~ 0.59%
  - Inverted gain of induction (V) plane: 133 ± 5 e-/ADC, INL ~ 0.81%
  - Inverted gain of induction (U) plane: 129 ± 6 e-/ADC, INL ~ 0.78%
Test#35 (09/23/2018) CE Performance Evaluation (Drift = 180kV, Nominal Wire Bias)

Histogram of ENC of U plane (4781 Chns)
- 4439chns: 651 ± 54 e⁻
- 342chns: > 800 e⁻

Histogram of ENC of V plane (4781 Chns)
- 4347chns: 662 ± 56 e⁻
- 434chns: > 800 e⁻

Histogram of ENC of X plane (5716 Chns)
- 5473chns: 565 ± 60 e⁻
- 243chns: > 800 e⁻

Histogram of Gain of U plane (4781 Chns)
- 4781chns, 129 ± 6 (e⁻ / bit)

Histogram of Gain of V plane (4781 Chns)
- 4781chns, 133 ± 5 (e⁻ / bit)

Histogram of Gain of X plane (5716 Chns)
- 5716chns, 135 ± 6 (e⁻ / bit)

Histogram of INL of U plane (4781 Chns)
- 4781chns, 0.78 ± 0.30 %

Histogram of INL of V plane (4781 Chns)
- 4781chns, 0.81 ± 0.26 %

Histogram of INL of X plane (5716 Chns)
- 5716chns, 0.59 ± 0.31 %
Collection mode – DC analysis – new FE analysis (1)

Non-collection (induction) mode

Collection mode

In collection mode, due to packaging, FE channels have non-uniform baseline

*In induction mode baseline DC voltage is uniform*

Baseline voltage across channels in the chip

Modify DC circuits for collection mode, maintaining the same (DC) operating points of the original FE, by making it similar to the induction mode
Collection mode – DC analysis – new FE analysis (2)

Changes made in the FE (filter)
- New DC bias points – V1 and V2 – in order keep proper DC levels in the analog chain
- Current source removed
Stability of Amp1, Amp2 & Amp3 verified for corners FF, SS, SF, FS, variation of Power Supply (~10%) and Temperature → Phase Margin (PM) > 30 degrees*

* PM mostly greater than 45, it approaches ~ 30 when T<186 and peaking time 3μs

2018/09/25
H. Chen - DUNE Collaboration Meeting
Gain setting – SG0 SG1

Current configuration
SG(0,1): \(00=4.7\text{mV/fC}, 10=7.8\text{mV/fC}, 01=14\text{mV/fC}, 11=25\text{mV/fC}\)

New setting
SG(0,1): \(00=14\text{mV/fC}, 10=25\text{mV/fC}, 01=7.8\text{mV/fC}, 11=4.7\text{mV/fC}\)
Layout of P3 FE ASIC

- Layout of P3 FE ASIC, with modifications highlighted in yellow boxes
- P3 FE ASIC will address
  - Non-uniform baseline by using similar baseline scheme for both induction mode and collection mode
  - In addition, default gain setting of FE ASIC will be 14mV/fC, instead of 4.7mV/fC
- More details can be found in the July CE workshop
  - [https://indico.fnal.gov/event/17076/session/1/contribution/4/material/slides/0.pptx](https://indico.fnal.gov/event/17076/session/1/contribution/4/material/slides/0.pptx)
Fabrication and Evaluation of FE ASIC

- P3 FE ASIC was submitted in late March
  - PO dispatched on 03/21
  - Total 240 dies are produced

- Packaging of chips took much long than expected
  - Bonding diagram was released on 06/22
  - Marking form was confirmed on 07/30
  - Chips were delivered on 08/27

- P3 FE ASIC maintains same foot print and pinout as P2 FE ASIC
  - Quad socket FE ASIC test board for ProtoDUNE-SP is being used for evaluation
  - It is compatible with FEMBs for both ProtoDUNE-SP and SBND
Preliminary test results of P3 FE ASIC in LN2 show

- Baseline distortion in collection mode is fixed
- Default gain setting of 14mV/fC is verified

- Evaluation of P3 FE ASIC
Baseline has been characterized in different configurations (4 gains x 4 peaking times)

For all 188 chips tested in LN2, no baseline failure has been observed
Gain has been characterized in different configurations with calibration

- Monitoring output has been verified for all channels
Summary

- Cold FE ASIC is continuing development toward a robust design adaptable to future design rule and process technology changes.

- P3 FE ASIC has been fabricated and evaluated in the lab:
  - Baseline distortion caused by package has been addressed.
  - Default gain configuration is set as 14mV/fC.

- All 188 P3 FE ASICs have been tested with quad FE ASIC test board in LN2:
  - 176 chips passed test, with yield of 93.6%.
  - 9 chips failed warm+cold test (die or wire bonding issue) and 3 chips have input pin failure in cold (socket issue).

- P3 FE ASIC will be evaluated on FEMB in various integration test stand for performance studies:
  - 40% APA at BNL, small TPC at Fermilab and APA7 at CERN.

- Test results of P3 FE ASIC will guide the development plan of P4 FE ASIC:
  - Current plan is to implement SE-DIFF converter in FE ASIC.
Outline of Fiber Test

- Introduction
- Test Setup of 300m Fiber
- Test Results
- Summary
Introduction

- DUNE far detector has DAQ system housed in the CUC
- The interface between DUNE SP LArTPC electronics and DAQ system is fiber optical links between WIB and DAQ system
- The fiber length could be up to 300 meters with few adapters/couplers
- Motivation of fiber test is to verify if 300m fibers work for 9.6 Gb/s from WIB to FELIX, and to measure the margin of optical power
- Preliminary test results have been presented in the July CE workshop
  - [https://indico.fnal.gov/event/17076/session/5/contribution/24/material/slides/0.pptx](https://indico.fnal.gov/event/17076/session/5/contribution/24/material/slides/0.pptx)
Test Setup of 300m Fiber

- ProtoDUNE-SP WIB and FELIX card are used for fiber test
  - WIB FPGA: Altera Arria V GT 5AGTFD3H3F35I3
  - QSFP+: AFBR-79EIPZ
  - FELIX FPGA: Kintex Ultrascale XCKU115-2
  - MiniPOD: Avago AFBR-824Vxyz

- Both OM3 and OM4 fibers are being tested
  - 300m OM3 MTP-12 trunk cable: $672.5
  - 300m OM4 MTP-12 trunk cable: $822.5
  - ~22% cost difference

- Attenuator is used in the test setup to measure optical power margin
  - Two patch boxes are used in the test setup, to emulate adapter/coupler in final experiment configuration

- Test data stream
  - 8b10b input is 32-bit PRBS31 with SOP, EOP and several IDLEs.
**FLX-712 MiniPOD Power Scan**

<table>
<thead>
<tr>
<th>channel#</th>
<th>MINIPOD_RX1</th>
<th>MINIPOD_RX2</th>
<th>MINIPOD_RX3</th>
<th>MINIPOD_RX4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (uW)</td>
<td>626.78</td>
<td>514.60</td>
<td>605.36</td>
<td>637.14</td>
</tr>
<tr>
<td>1 (uW)</td>
<td>525.50</td>
<td>586.80</td>
<td>585.30</td>
<td>629.79</td>
</tr>
<tr>
<td>2 (uW)</td>
<td>682.17</td>
<td>608.70</td>
<td>665.02</td>
<td>686.98</td>
</tr>
<tr>
<td>3 (uW)</td>
<td>656.98</td>
<td>694.25</td>
<td>689.74</td>
<td>709.07</td>
</tr>
<tr>
<td>4 (uW)</td>
<td>565.50</td>
<td>491.46</td>
<td>515.80</td>
<td>579.20</td>
</tr>
<tr>
<td>5 (uW)</td>
<td>670.44</td>
<td>658.50</td>
<td>628.60</td>
<td>626.40</td>
</tr>
<tr>
<td>6 (uW)</td>
<td>671.80</td>
<td>627.77</td>
<td>716.48</td>
<td>616.96</td>
</tr>
<tr>
<td>7 (uW)</td>
<td>430.04</td>
<td>697.88</td>
<td>696.10</td>
<td>701.95</td>
</tr>
<tr>
<td>8 (uW)</td>
<td>570.18</td>
<td>589.36</td>
<td>572.97</td>
<td>618.52</td>
</tr>
<tr>
<td>9 (uW)</td>
<td>636.80</td>
<td>625.00</td>
<td>621.60</td>
<td>611.78</td>
</tr>
<tr>
<td>10(uW)</td>
<td>716.21</td>
<td>725.02</td>
<td>688.00</td>
<td>642.21</td>
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<tr>
<td>11(uW)</td>
<td>746.20</td>
<td>762.50</td>
<td>700.94</td>
<td>726.70</td>
</tr>
</tbody>
</table>

- Power measurement was done on 4 MiniPOD receivers, total 48 channels on FLX-712 card
- The weakest RX channel is used for fiber test → a conservative approach
The attenuator introduces extra (0.4dB~0.7dB) attenuation even if the value is set to 0.
Automatic Data Taking

- BER test is carried out by scripts automatically
  - VIO for error counter in FPGA firmware is controlled by TCL script
  - Attenuator can be configured remotely with Python script
  - Interface between TCL and Python scripts is implemented

- Once the test setup is ready, the only thing need to do manually is to switch fibers
Fiber Test between WIB2 and FELIX

- BER < $10^{-14}$, assuming these points have 1 error, though no error was detected in the test
  - Weakest FELIX RX link was used in the test
  - The attenuator introduces extra (0.4dB~0.7dB) attenuation

- Margin of OM3 fiber > 7.15dB, margin of OM4 fiber > 8.4dB
Summary of Fiber Test

- Test setup of 300m fiber has been established to verify ~10Gb/s link from WIB to FELIX
  - Margin of optical power is being characterized with both OM3 and OM4 fibers

- The margin for BER < 10^{-14} is more than 7.15dB for OM3 fiber, and more than 8.4dB for OM4 fiber
  - 1.25dB more margin is aligned with ~20% higher cost on OM4 fiber
  - More test with different WIB links ongoing as a cross check

- Conclusion: WIB to FELIX link can run stably with 300 meter OM3/OM4 fiber at 9.6Gb/s with good margin
  - This supports the recent TC decision on the default plan of 10Gb/s link between WIB and DAQ system