Demonstration of micro-power pixel readout for LArTPCs

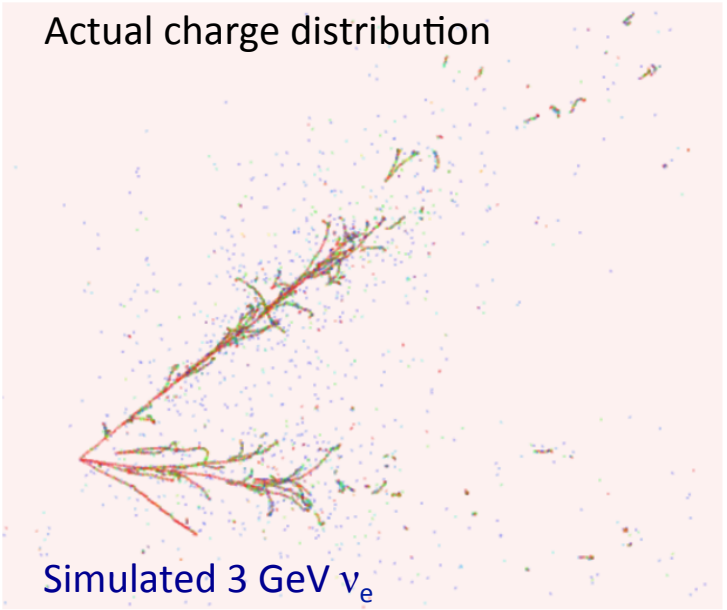
Dan Dwyer (LBNL)

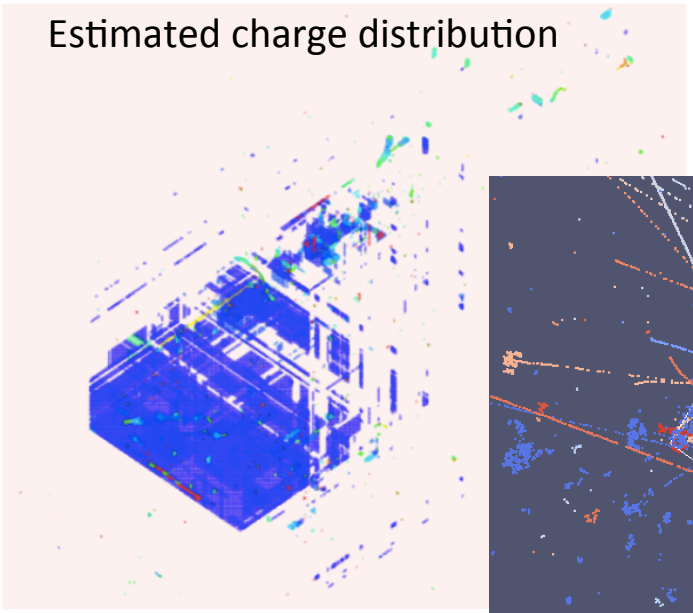
Pixels for DUNE Meeting – FNAL

Mar. 5, 2018

3D LArTPC: Motivation

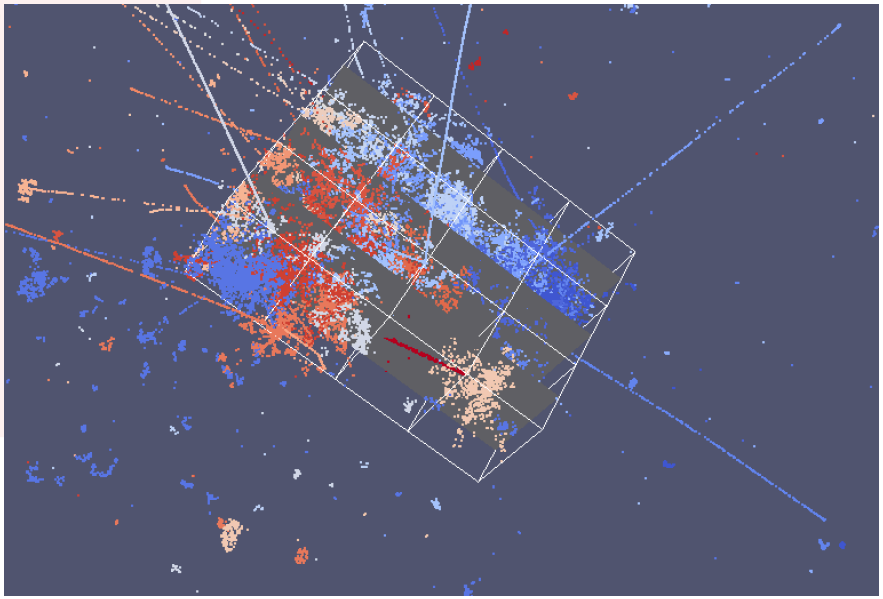
Ambiguities in projective wire readout:





DUNE Near LArTPC:

High neutrino rate exacerbates ambiguities.



Example neutrino signals from one LBNF spill

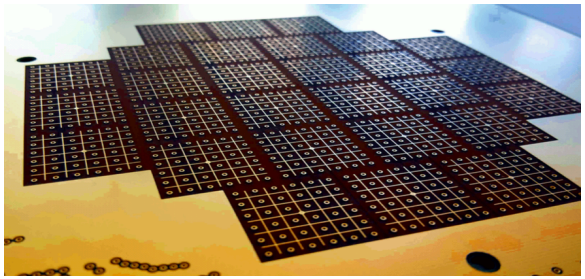
Pixel Readout Development

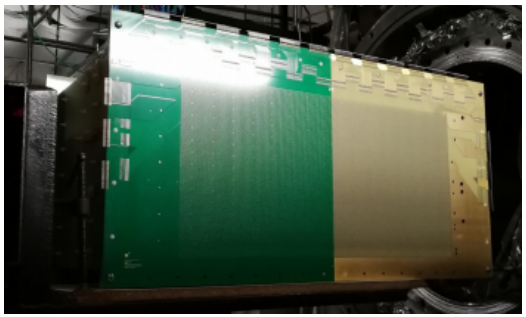
Demonstration of pixel sensor feasibility (Bern/ArgonCube)

Progress with in-beam tests (PixLAr)

→ Low-power pixel electronics (LBNL)

ArgonCube





PIXLAR

A LArLAT production

LArPix Overview

Developing front-end ASIC for scalable LArTPC pixel readout

- True 3D readout: front-end channel for each 'pixel' (i.e. pad-based readout)
- Scalable: power use must be very low to avoid excess heat generation in LAr

Much progress over last few months:

- Produced first-generation LArPix-v1 ASIC
- Room temp tests: Chips performance good. Exceeded design targets.
- Cryogenic tests (LN_2 bath): No issues with cryogenic operation.
- Integrated with 10-cm-drift Demonstrator LArTPC.

Next Steps:

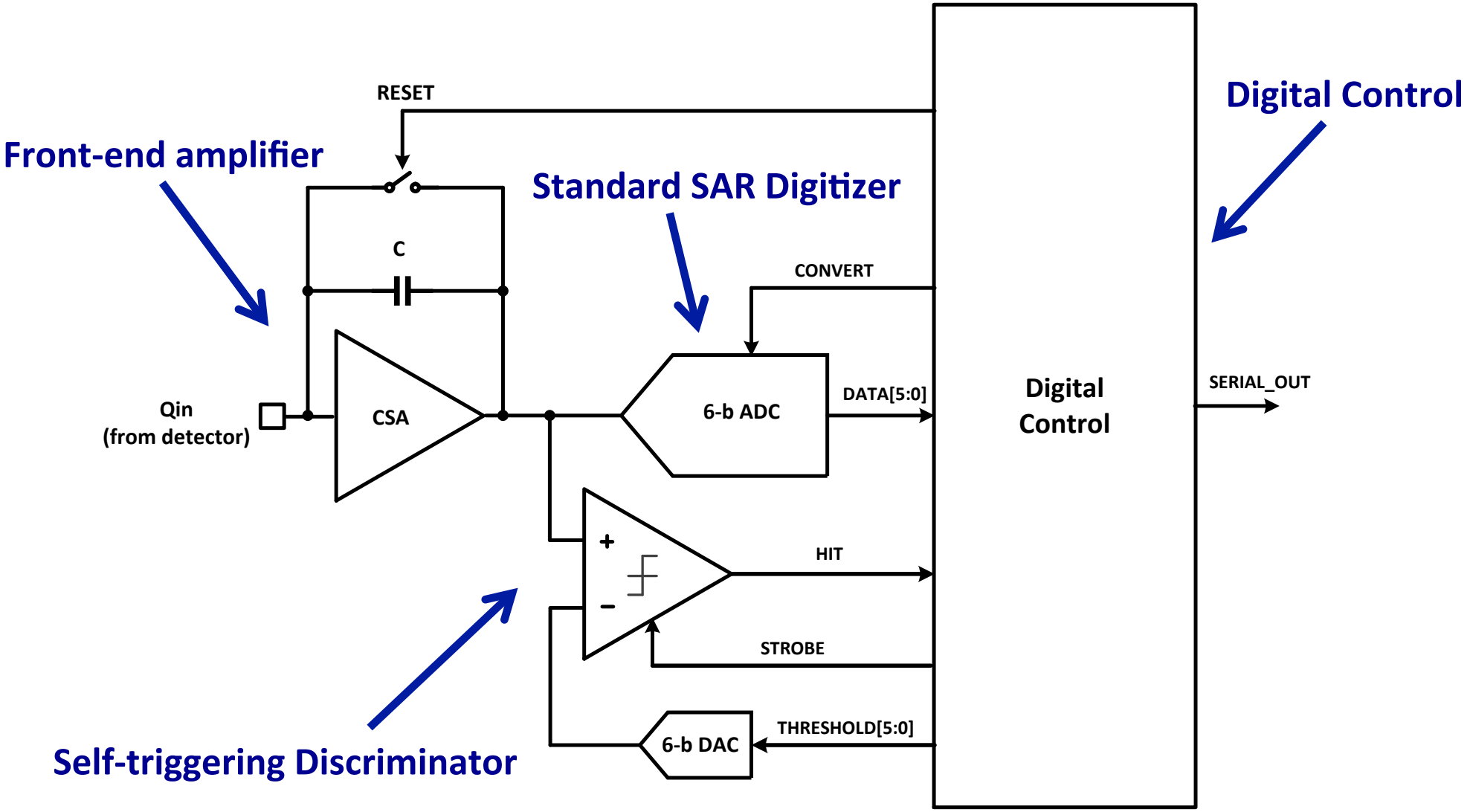
- Scaled-up O(1000) pixel sensor production almost complete.
  → Will install and test in 60-cm pixel demonstrator TPC at Bern

Team:

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stezelberger, M. Kramer, S. Kohn, P. Madigan

LArPix-v1: Design Concept

Amplifier with Self-triggered Digitization and Readout

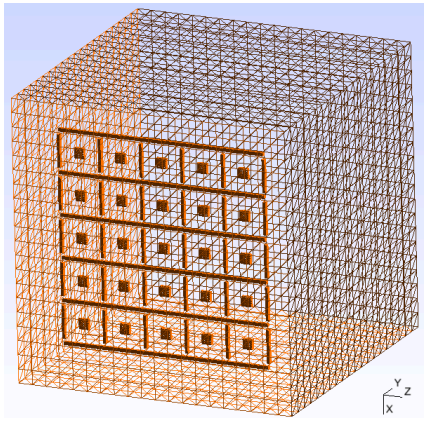


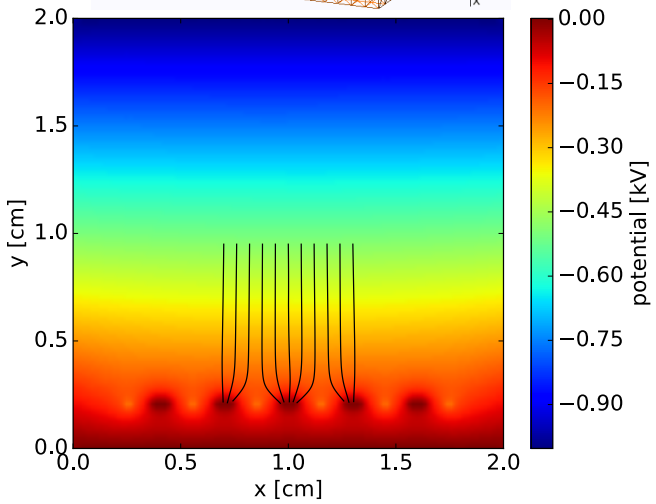
Achieve low power: avoid digitization and readout of mostly quiescent data.

Design Tools

Developed a set of tools to assess TPC readout design

Sensor model in 3D

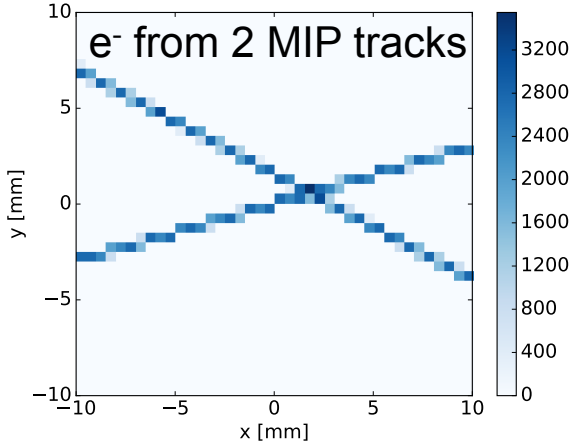


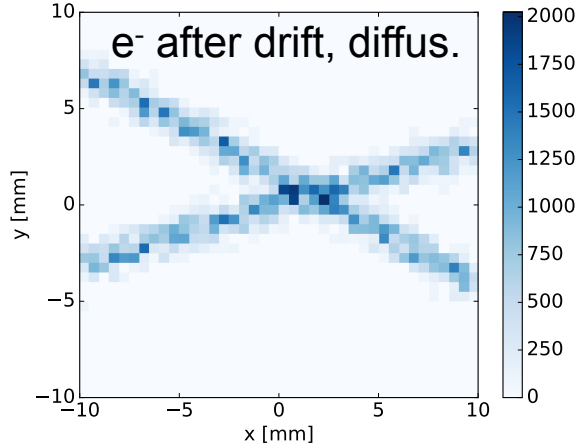


3D drift field, pix response

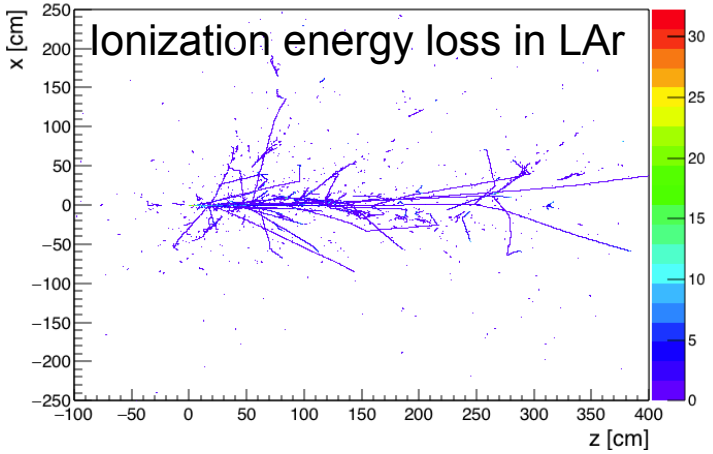
→ *Thanks to B. Viren for intro to BEM tools*

Ionization, recomb., drift loss, diffusion

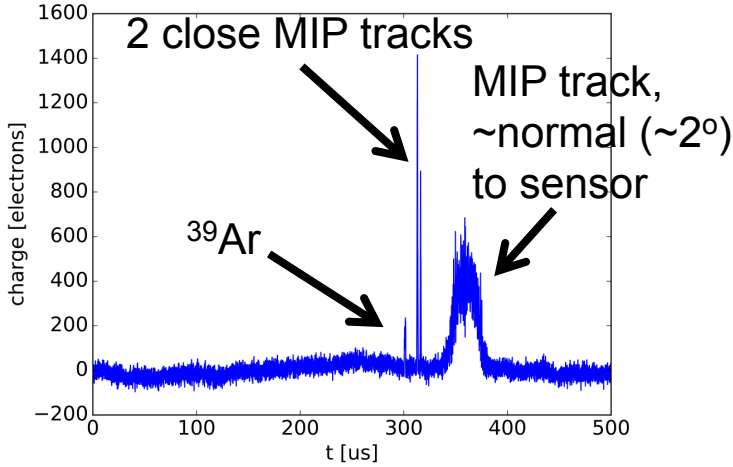




Fast primitive Geant4 sim.



Realistic signals (with noise)

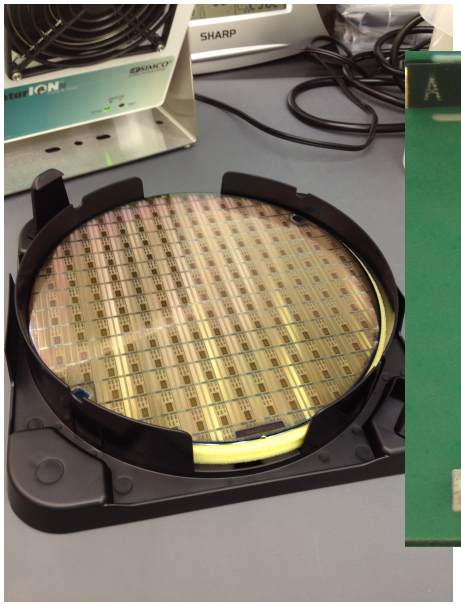


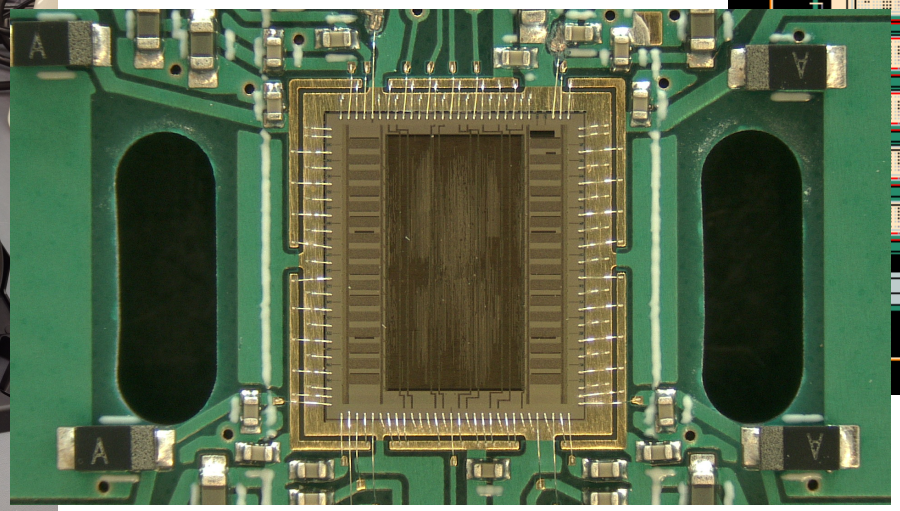
Signals have been input to IC modeling program (Spice, Cadence) to assess IC design, performance.

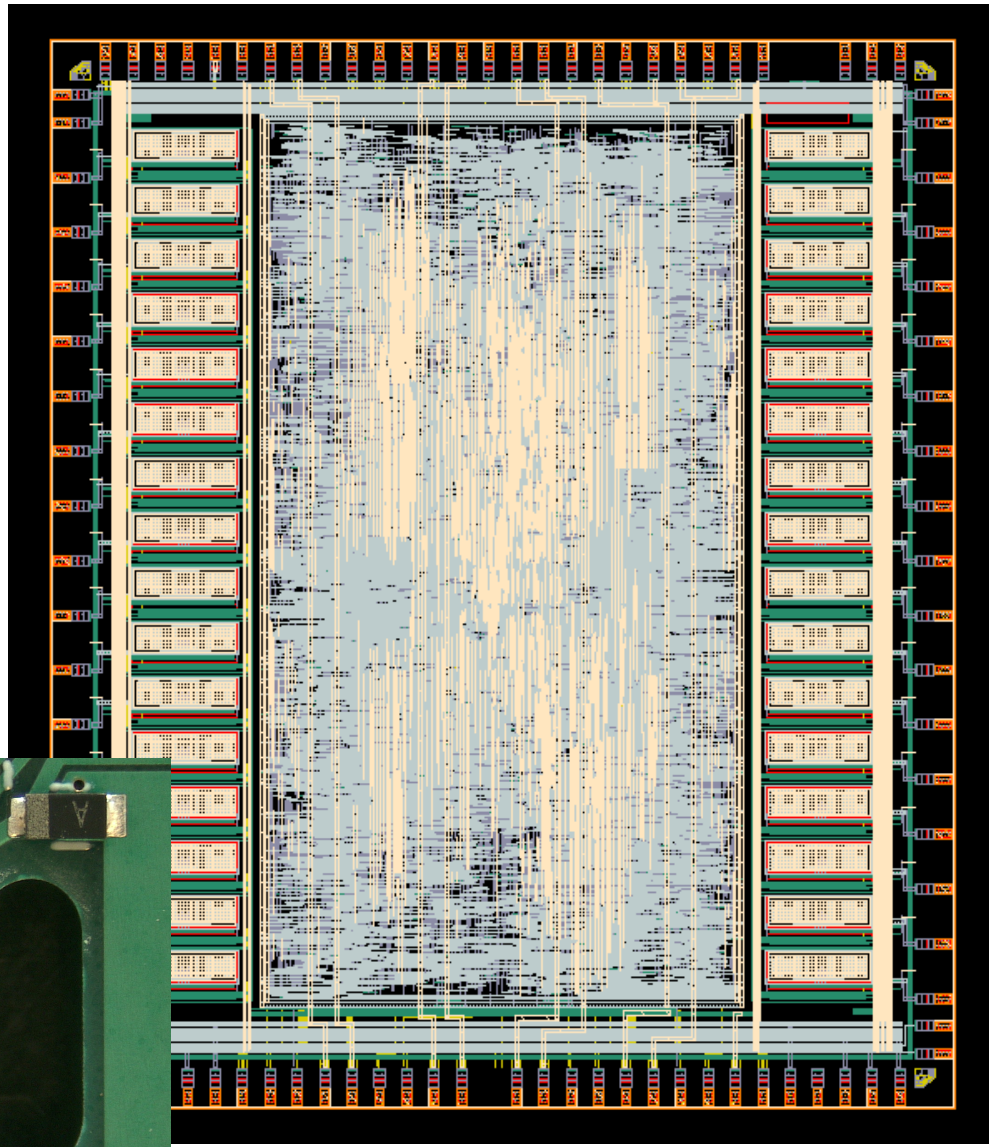
LArPix Prototype Progress

LArPix-v1 ASIC:

- Dec. 2016: Design began
- May 2017: Design completed
- June 2017: Submitted for fabrication
- Sep. 2017: Test board designed
- Oct. 2017: Chips, test boards @ LBNL
- Nov. 2017: Basic tests completed
- Dec. 2017: Cryo-tests completed
- Jan. 2018: First chips bonded to sensor
- Feb. 2018: First operation of 3D LArTPC







Process: TSMC 180nm

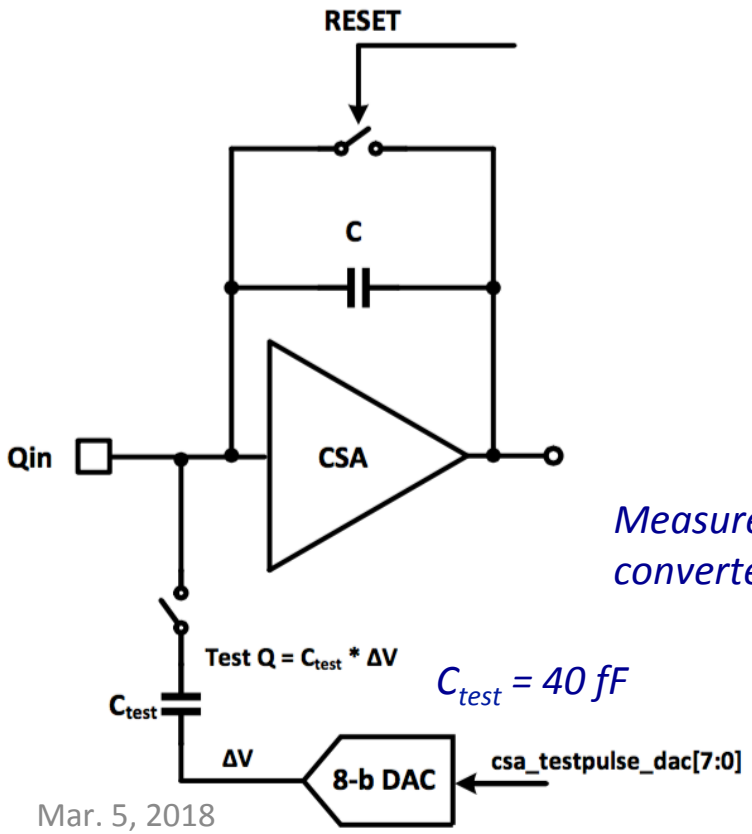
LArPix-v1: Amplifier

Target 1: Demonstrate low-noise low-power cryogenic amplifier (CSA)

Design goal: Amplify electron signal at gain of 1 mV per 250 e-

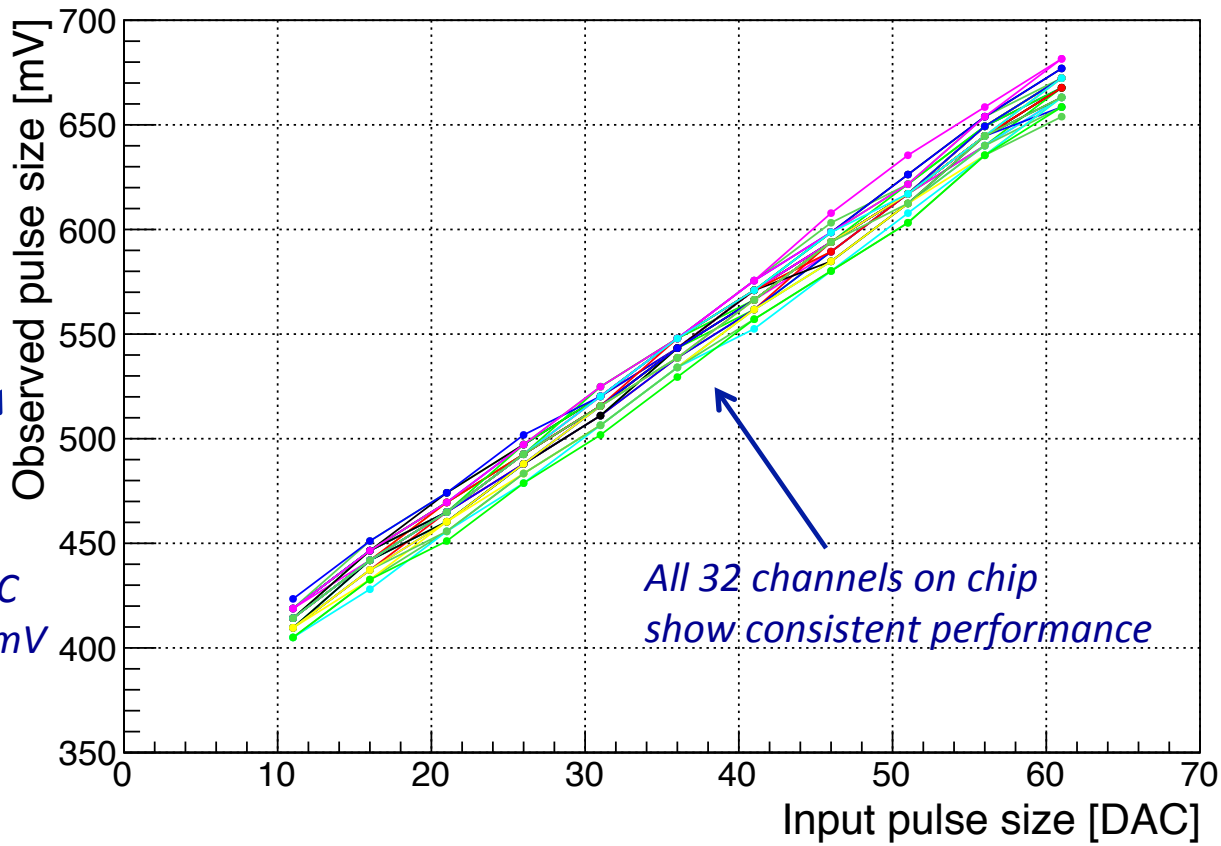
Initial Results: Amplifiers functions as expected

- Use internal test pulser on each channel
- No sensor attached
- Measured signals using ADC in self-trigger mode
- **Gain: Consistent with ~1 mV per 250 e-**



C_{test} = 40 fF

Measured ADC converted to mV



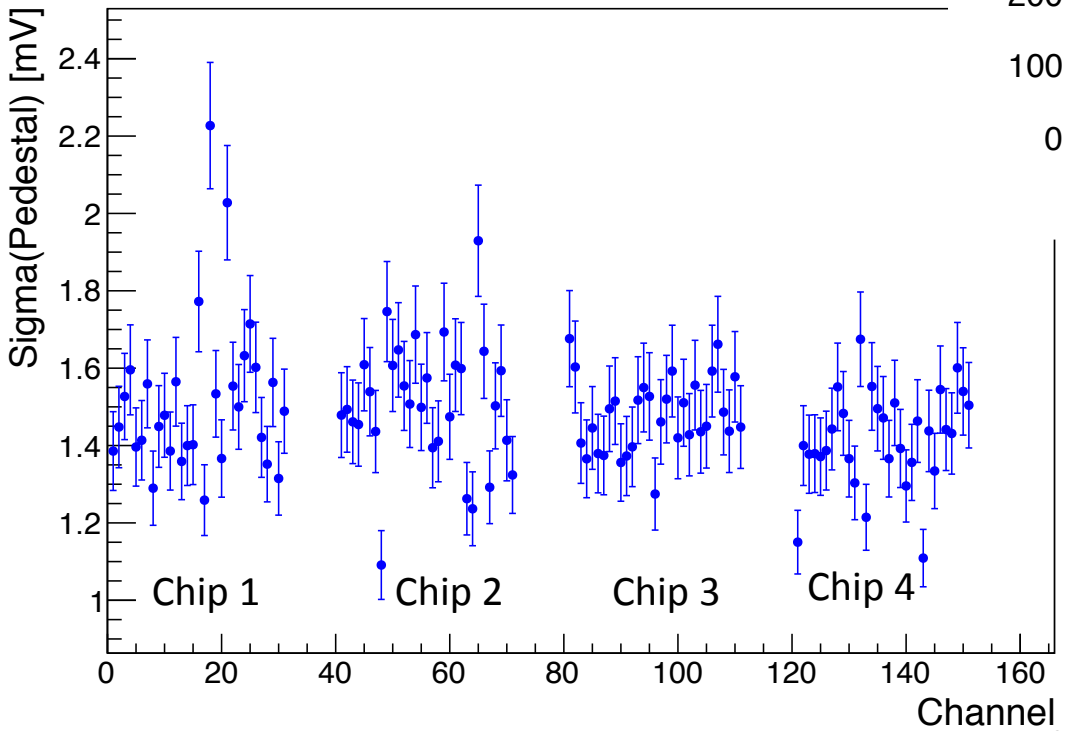
All 32 channels on chip show consistent performance

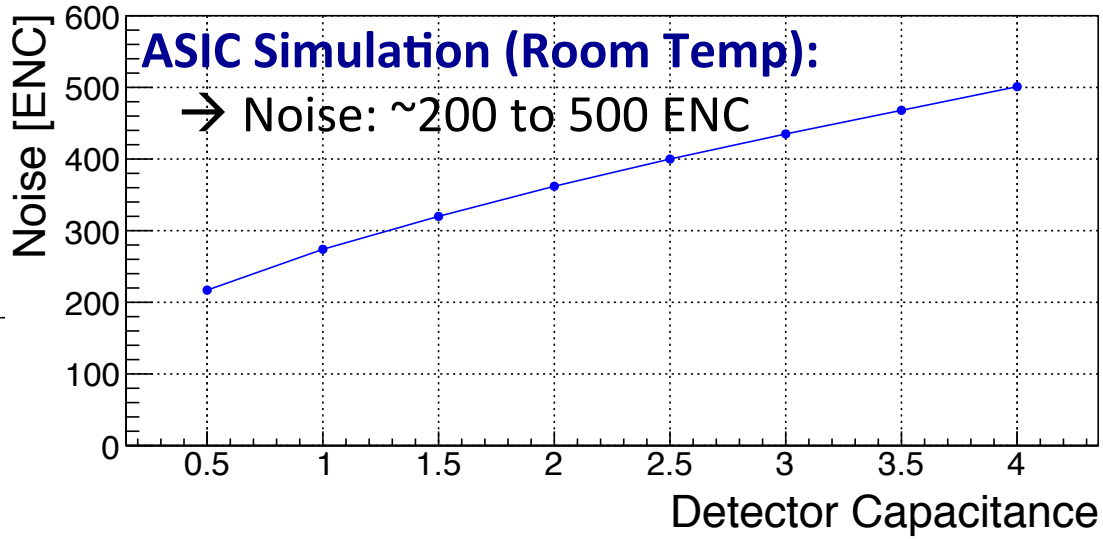
LArPix-v1: Noise

Target 1: Demonstrate low-noise low-power cryogenic amplifier (CSA)

Design goal: >10:1 signal-to-noise ratio for MIP signal
→ Noise < ~1600 electron-noise-equivalent (ENC)

Initial Results:
- First 4-chip board (128 channels)
- No sensor attached.
- Measured signals via forced ADC digitization.
- **Noise (1σ): ~1.5 mV → 375 e-**





Notes:
CSA gain: 1 mV ≈ 250 e-
1 ADC bin ≈ 2 mV, so binning (quantization 'noise') also contributes to this measurement.

LArPix-v1: Power

Target 1: Demonstrate low-noise low-power cryogenic amplifier (CSA)

Design goal: Power use (heat generation) less than heat flux through cryostat walls

→ Total pixel electronics power consumption ~< 10 W/m^2

Pixel Pitch	Pixels/m^2	Power/m^2	(assuming 100 µW/channel)
3 mm	111.1k	11.1 W	
4 mm	62.5k	6.3 W	
5 mm	40.0k	4.0 W	

Analog Power:

- ASIC Simulation: 24 µW/channel
- Bench Measurement: 24 µW/channel

Unexpected surprise: Digital power also very low!

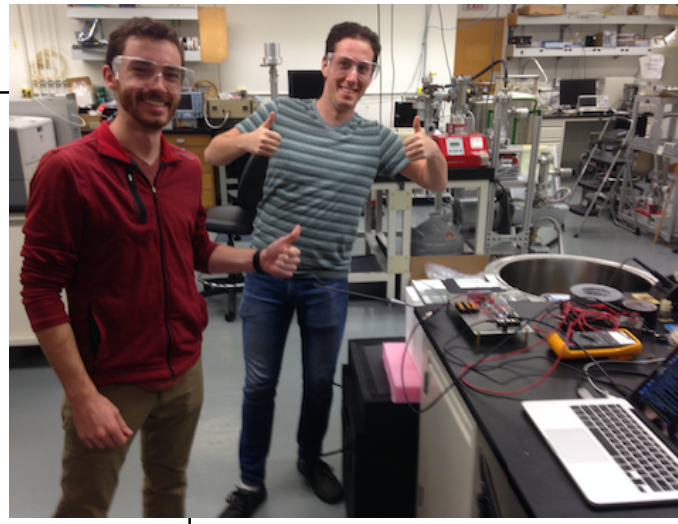
Mode:	Core Voltage	I/O Voltage	Power (Dig.) [µW/ch]	Power (Ana.+Dig.) [µW/ch]
Default	1.8 V	3.3 V	233	257
Low-power	1.1 V	2.0 V	37	61

→ Still some room for tuning I/O voltage to bring power down further.

LArPix-v1: Cryo-performance

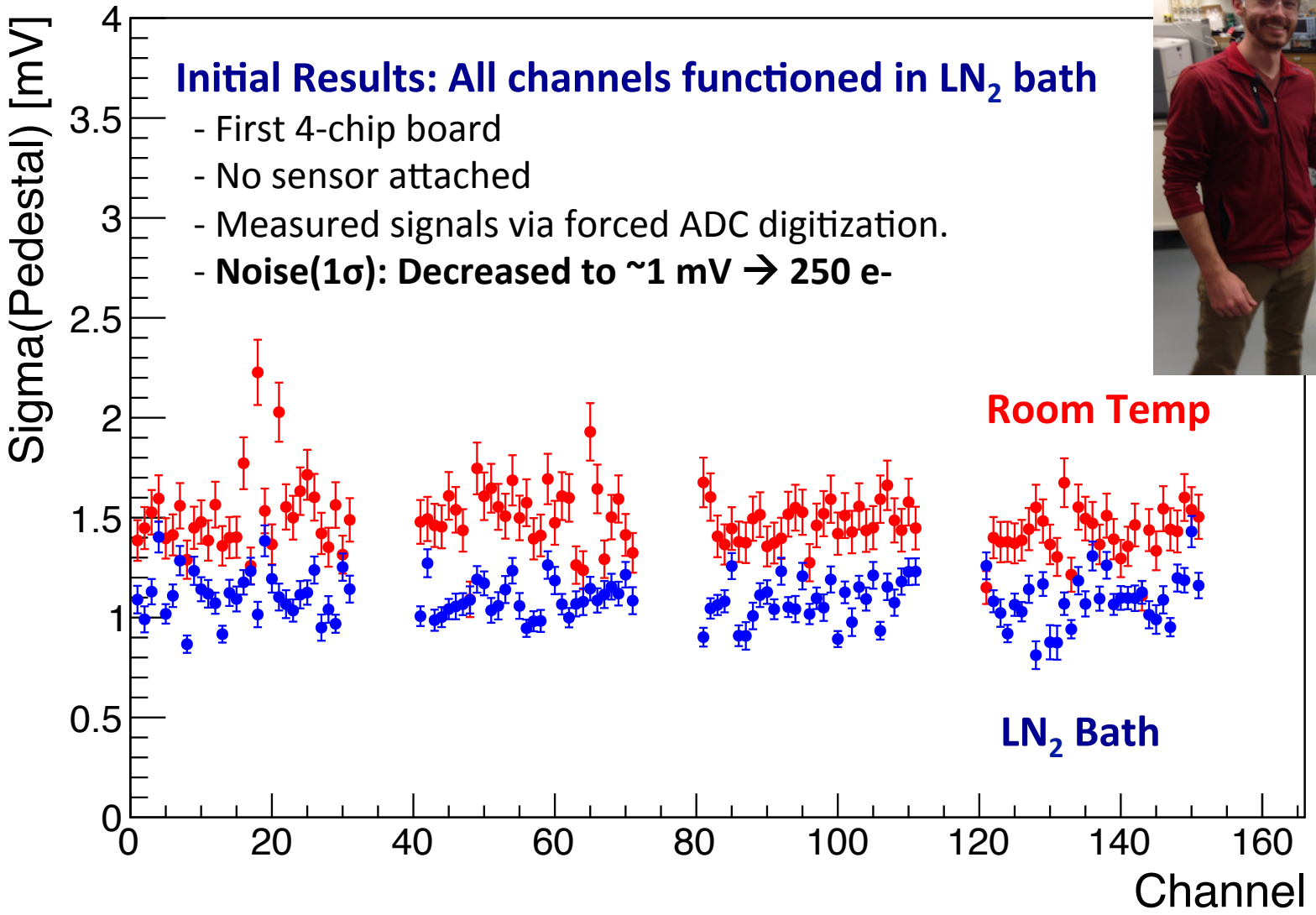
Target 1: Demonstrate low-noise low-power cryogenic amplifier (CSA)

Design goal: Operate at liquid argon temperature



Initial Results: All channels functioned in LN_2 bath

- First 4-chip board
- No sensor attached
- Measured signals via forced ADC digitization.
- **Noise(1σ): Decreased to ~1 mV → 250 e-**

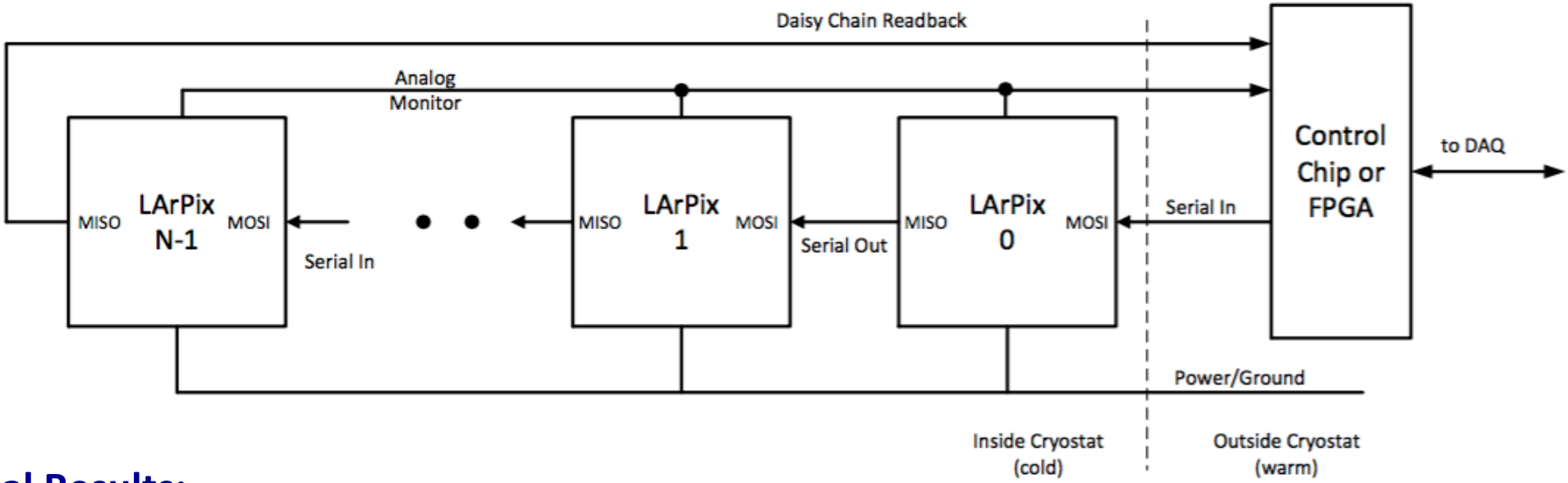


LArPix-v1: Digital Multiplexing

Target 2: Demonstrate scalable low-power digital multiplexing

Design goal: Reduce cryostat data I/O penetrations to manageable level.
→ I/O penetrations ~< 100 per m^2 of sensor

Approach:
Daisy-chain I/O through internal FIFO buffer on each chip.

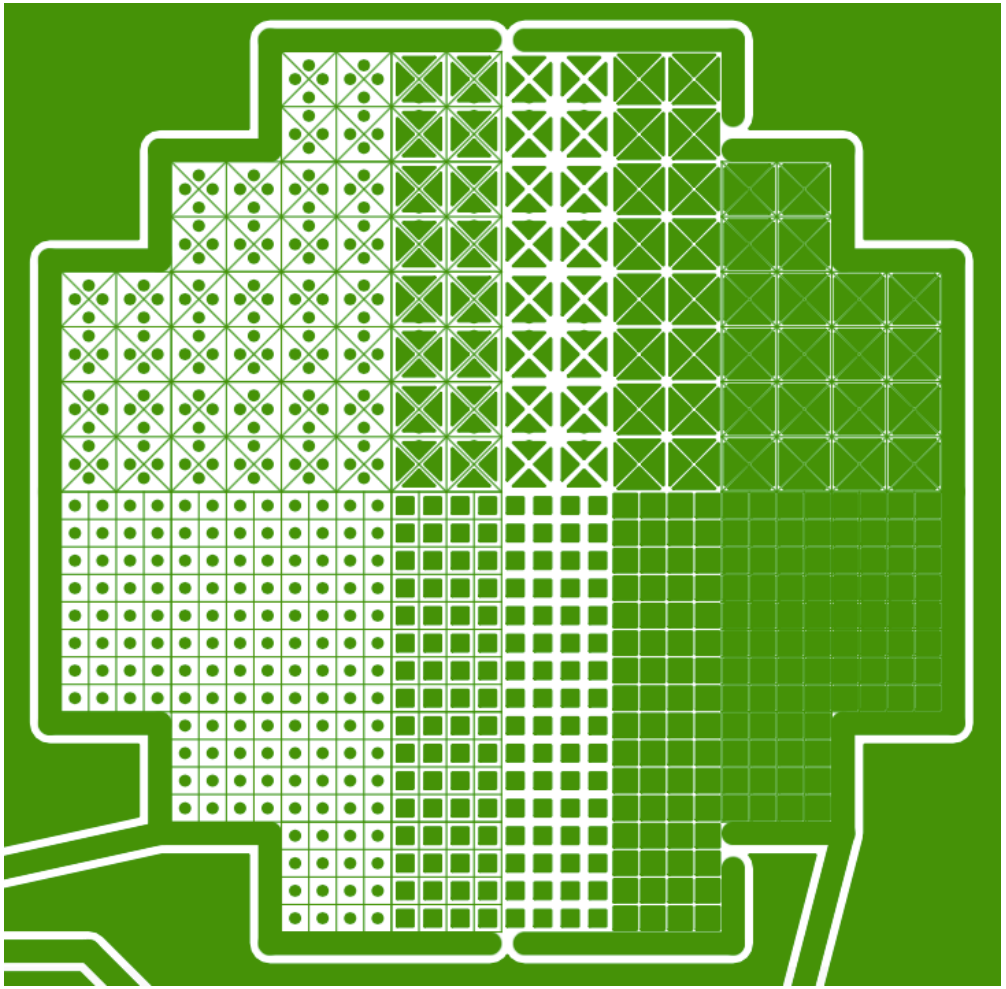


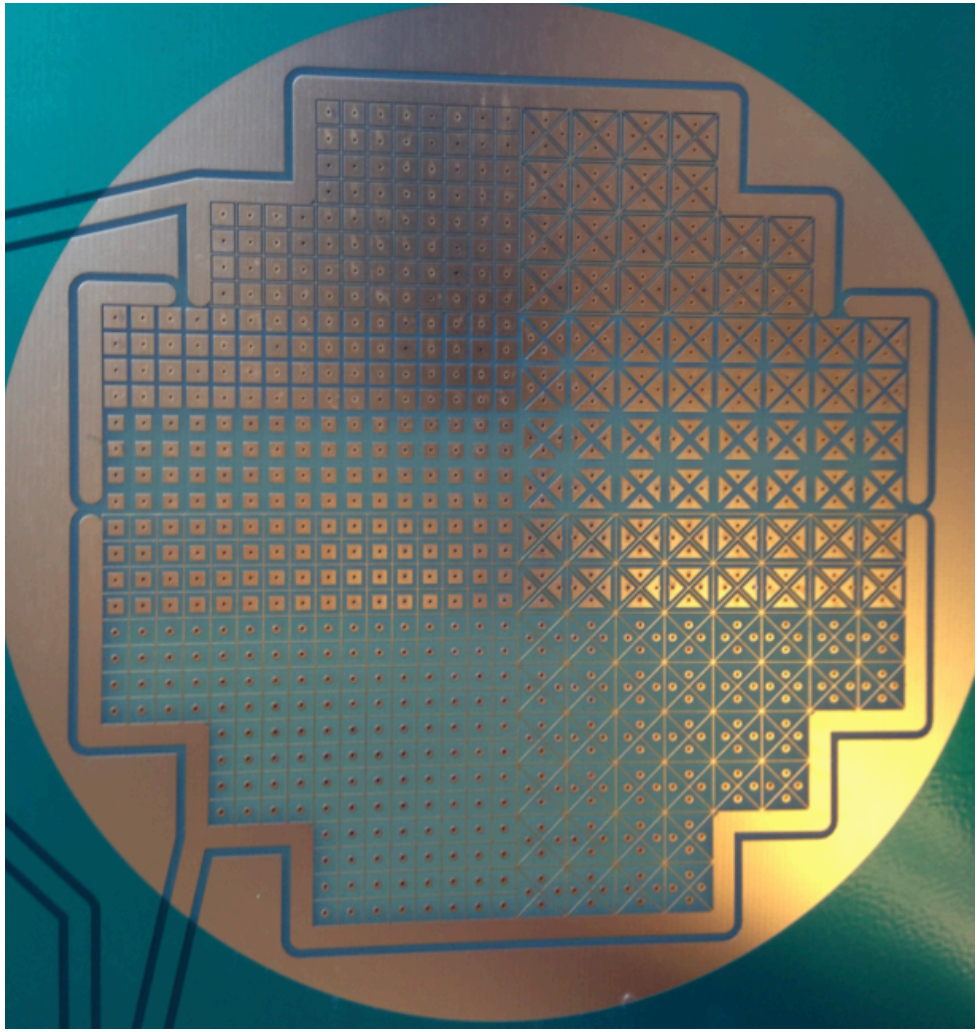
Initial Results:
- No problems multiplexing 128 channels on single pair of digital I/O lines
- Internal FIFO buffers: no issues with buffer overflow; plenty of FIFO headroom
- LArPix-v1: Can scale to 8160 pixels on single I/O chain (~30 lines / m^2 of sensor @ 3mm pitch)

LArPix-v1: Sensor Prototype

Prototyping a variety of pixel sensor geometries

Sensor board designed to fit Bern Pixel Demonstrator TPC
Includes 10 different pixel geometries/configurations
Tested in combination with 128-channel LArPix board.

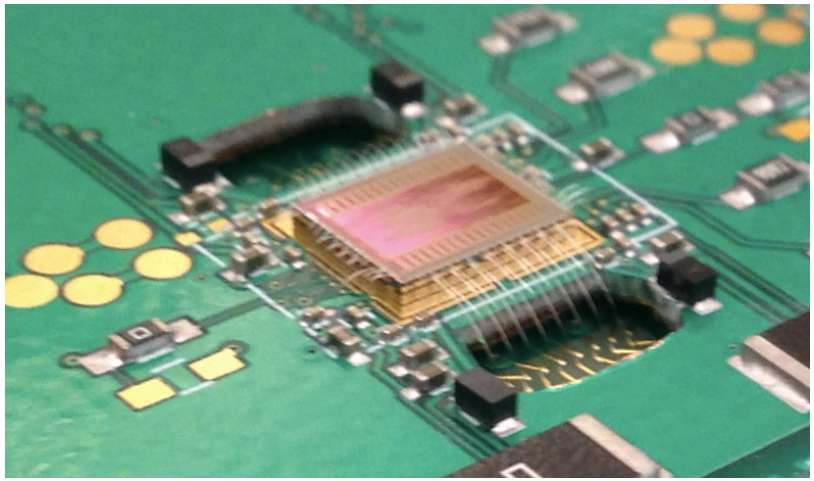




LArPix-v1: TPC Integration

Initial LArTPC operation:

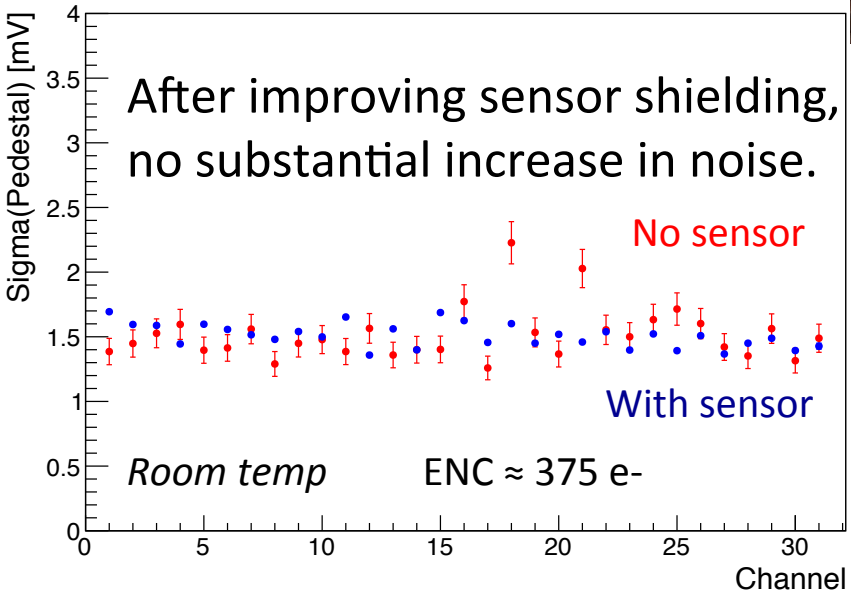
First chips bonded to sensor board



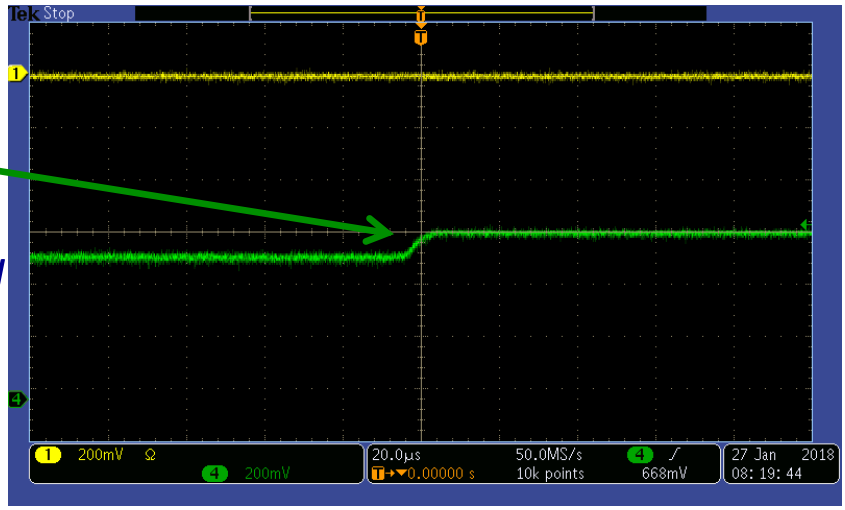
First LArPix 128-pixel sensor integrated with 10-cm Demonstrator LArTPC

First cool-down, LAr fill:
Jan. 26, 2018

Initial results:
- All chips operational.
- TPC system noise OK.
- Tested μ-telescope
- Tested bias and cathode HV.
- Tested CSAs with internal pulser and bias grid coupling.

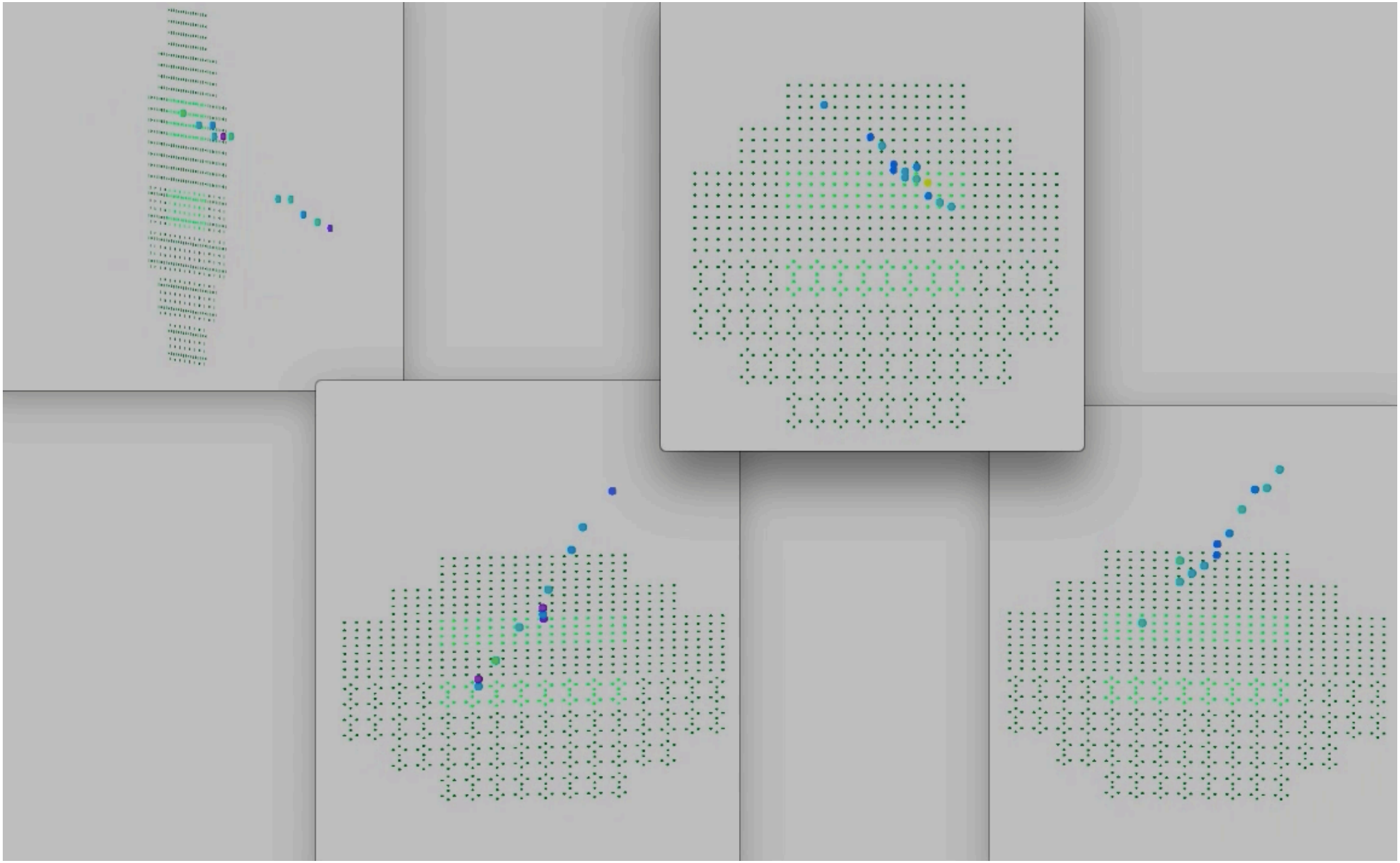


Example pulse consistent with ~25k e- signal (using integrated analog monitor)



LArPix-v1: First Tracks

Feb. 13, 2018: Detected first cosmic ray tracks



LArPix-v1: O(1000) Pixel Sensor

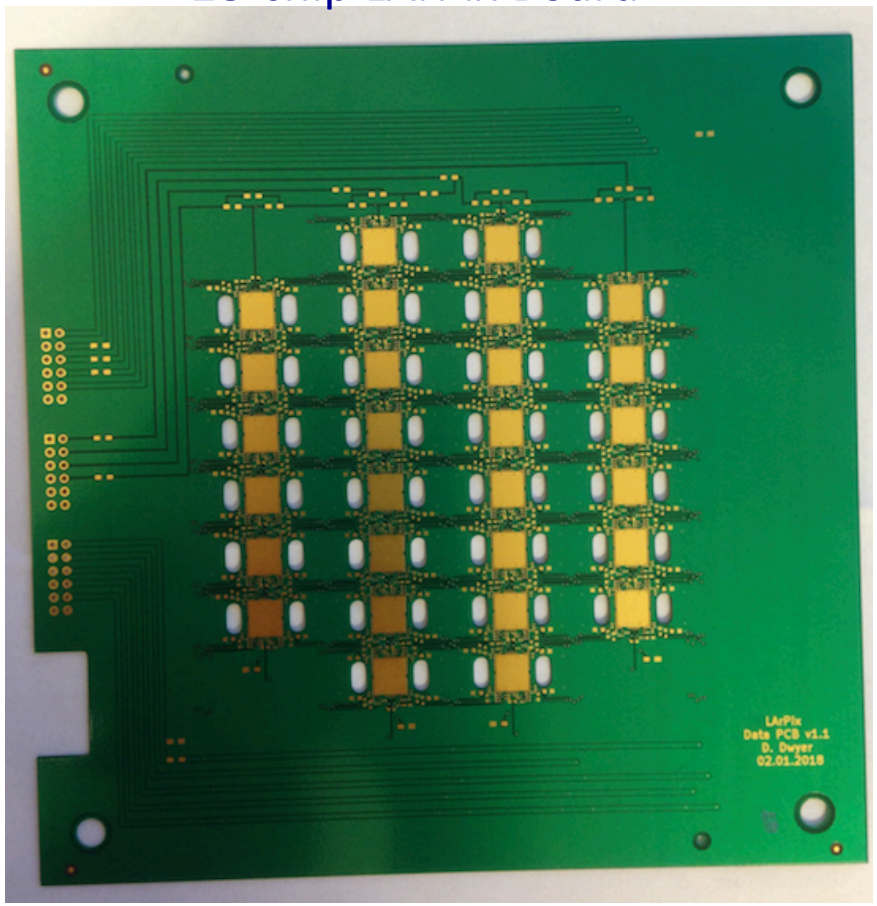
Assembling fully-instrumented 832-pixel sensor:

Loading first chips onto 28-chip LArPix PCBs this week.

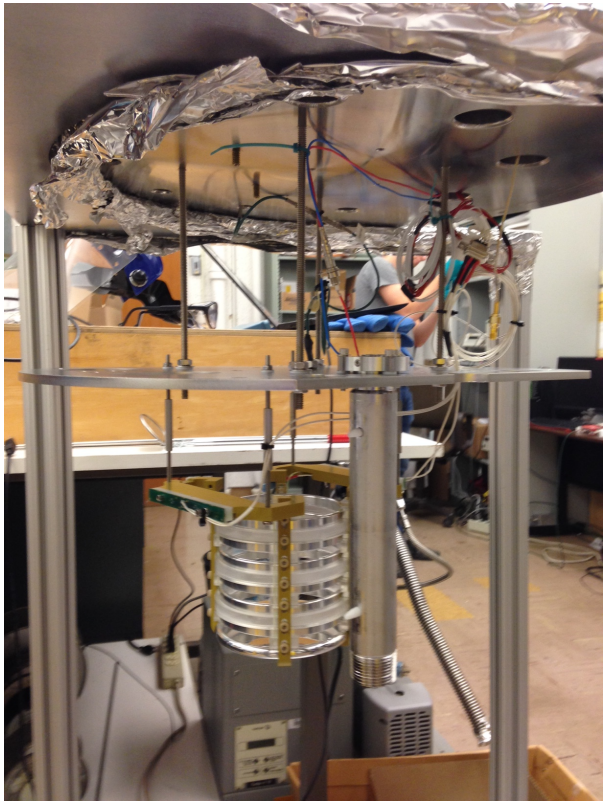
One board: testing in 60-cm-drift Pixel Demonstrator TPC (Univ. of Bern)

One board: testing in 10-cm-drift Pixel Demonstrator TPC (LBNL)

28-chip LArPix Board

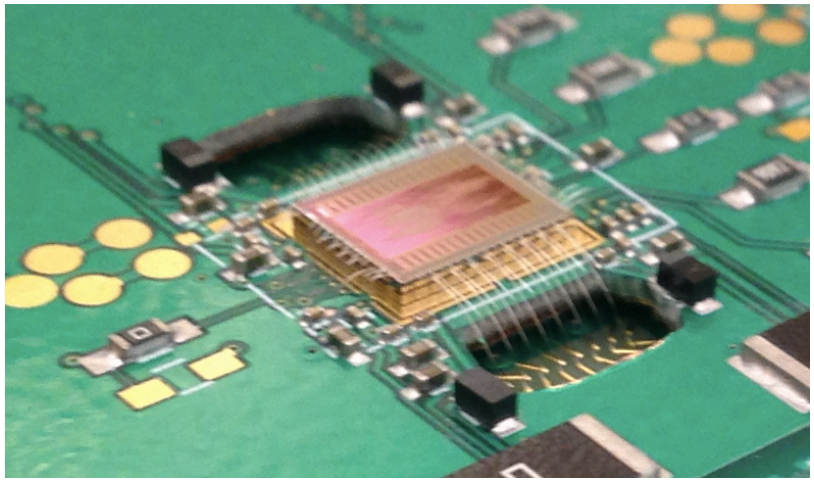


10-cm Pixel Demonstrator



60-cm Pixel Demonstrator

Looking Forward



Given success of LArPix-v1, now aiming for next goals:

1) LArPix-v2

- Pursue fully-featured IC design to meet LArTPC physics needs

2) LArIAT

- Design, produce sensor board for LArIAT PixLAr tests
- Install in LArIAT TPC
- Characterize performance with well-known particle beam.

3) ArgonCube 2x2

- Design, produce sensor plane for ArgonCube 2x2 module

→ Glad to work with any others interested in 3D readout.