

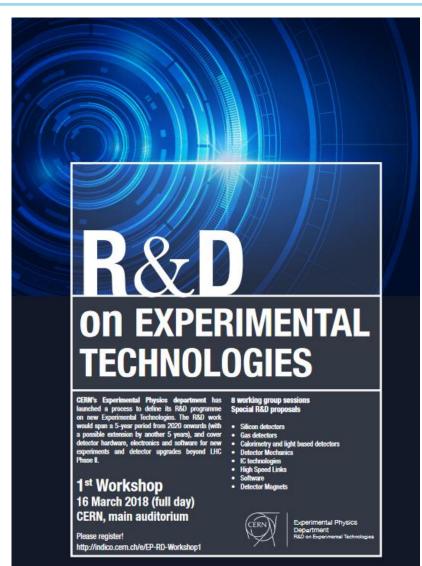
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CERN Workshop on R&D For Experimental Technologies

An Overview

Alan G. Prosser Detector R&D Advisory Group 12 April 2018

1st Workshop on R&D for Experimental Technologies General



Full Day Workshop on Experimental Technologies Sponsored by CERN Experimental Physics Department

Many efforts of interest to our group discussed

Organized by Working Groups:

Silicon Detectors Gaseous Detectors Calorimetry and Light Based Detectors Detector Mechanics High Speed Links IC Technologies Software

Detector Magnets

Material Summarized Here Can Be Found At: https://indico.cern.ch/event/696066/

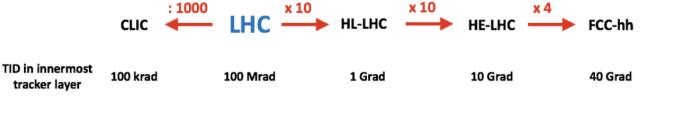


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1st Workshop on R&D for Experimental Technologies General

Scope of the discussions: HL-LHC and Beyond Radiation Environments Radiation tolerance requirement is strongly machine dependent

Here reference TID levels are in the innermost tracker layer (note that in some cases the forward calorimeters might be exposed to larger doses, such as in FCC-hh).For a lepton FCC machine, no simulation of the detectors' environment is still available.



Time to test 1 chip in our 1 minute 10 hours 4 days 40 days > 5 months X-ray machine

	RHIC STAR	LHC - ALICE	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp	
NIEL [n _{eq} /cm²]	10 ¹²	10 ¹³	<10 ¹²	10 ¹⁵	10 ¹⁶	10 ¹⁵⁻ 10 ¹⁷	
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad	
Hit rate [MHz/cm ²]	0.4	10	<0.3	100-200	2000	200-20000	<u>Re</u>

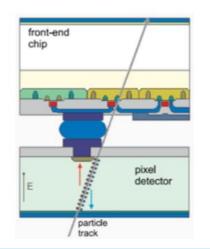


1st Workshop on R&D for Experimental Technologies Working Group 1: Silicon Detectors

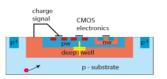
WG1 Topics: CMOS Sensors

Ref 1

Hybrid Pixels Hybrid Pixel Detectors

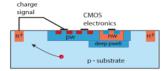


Large electrodes



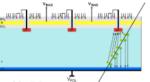
- Electronics in collection well
- No or little low field regions
- Short drift path for high radiation hardness
- Large(r) sensor capacitance
 (dpw/dnw) ->higher noise and slower @ given pwr
- Potential cross talk between digital and analog section

Small electrodes



- Electronics outside collection well
- Small capacitance for high SNR and fast signals
 Separate analog and digital
 - electronics Large drift path -> need process modification to usual CMOS processes for radiation hardness

"Burried" electrodes (SOI)



Double SOI structure

- Electronics and sensor in separate layer
- Can use thick or thin high resistivity material and HV (>200V)
- Special design/processing to overcome radiation induced charge up of oxides

• Front-end chip

- Depending on application we need specialized FE-ASIC (covered in ASIC WG), hence we have a clear interface with FE chip development for silicon sensors has much
- Sensor developments
 - For very high radiation and track density (e.g. 3D sensors, active edge planar)
 - Sensors for 4D tracking, i.e. spatial and time information (e.g. pixel sensors with trench electrodes)

Interconnection Issues (\$)

Wafer-wafer or wafer-die

Cu-cu direct DBI TSV

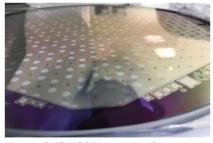


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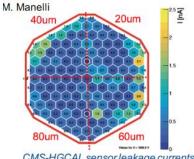
1st Workshop on R&D for Experimental Technologies **Working Group 1: Silicon Detectors**

WG1 Topics: Large Pitch and Timing Detectors

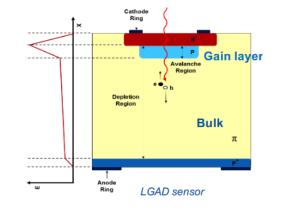
- Many challenges at system level: readout ASICs, clock distribution, module design, interconnects, cooling, automated production
- Silicon-specific R&D needs (WG 1):
 - Sensor technology: planar, passive CMOS, LGAD
 - · Sensor characterization and simulation
 - Understanding/mitigation of radiation effects



CMS-HGCAL sensor wafer



CMS-HGCAL sensor leakage currents



$$\sigma_t^2 = \sigma_{Jitter}^2 + \sigma_{TimeWalk}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

Several vendors: CNM, FBK, HPK Reached ~20 ps for few mm² size sensors → considered for HL-ATLAS/CMS/LHCb timing layers

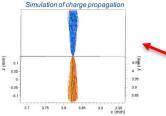


Ref 1

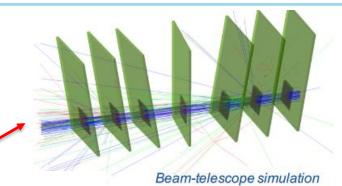
1st Workshop on R&D for Experimental Technologies Working Group 1: Silicon Detectors

WG1 Topics:

Device Modelling and Simulation



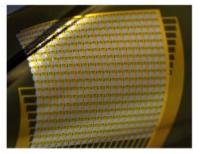
Wide range of simulation scope fromCharge level to Plane level



Interconnection and Module Construction



Materials and design for stability and thermal management (CTE, material budget)



Techniques and materials for fabrication and assembly (printing, adhesives)

http://engineering.nyu.edu/pressrelease/2011/11/14/

LED Professional, 13 Sep 2011, <u>https://goo.gl/aVkLzo</u>

Lab Infrastructure and Specialized Instrumentation

Essential Facilities Include:

Prototyping facilities Clean rooms Irradiation facilities

	2017		
Registered experiments	46 (<u>3 postponed</u>)		
Users / user teams	32		
User institutes	19		
Irradiated objects	802		
Measured Al-foils dosimeters	>600		
Max requested fluence	1×10 ¹⁷ p/cm ²		



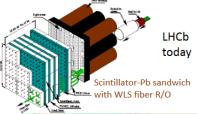


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1st Workshop on R&D for Experimental Technologies Working Group 3: Calorimetry

Possible Calorimetry Technologies for Future Detectors (a sample):

LHCb Beyond HL-LHC



Homogeneous crystal calorimeter with longitudinal segmentation Sampling Calorimeter (e.g. Shaslik or SpaCal type)

CLIC/ILC – CALICE

Large area Si Arrays Segmented Gas Amplification Structures SiPMs on scintillator tiles or strips

PFA Calorimeter

FCC-hh

Ref 2

HG EM Calorimeter based in Noble Liquid in Barrel Region Hadronic Calorimeter: Scintillator/Steel (barrel) Noble Liquid for Endcaps and Forward Calorimeter





1st Workshop on R&D for Experimental Technologies Working Group 3: Calorimetry

Large variety of active materials considered for calorimetry for future accelerator experiments. R&D needs depend on technology:

- Scintillator/crystal based
 - Radiation hardness of crystals, fibres, SiPMs (Photon detection \rightarrow see next talk)
 - Timing performance: understanding and improving the full detection chain
- Si based
 - Cost-effective solutions
 - Radiation hardness
 - Timing resolution (down to 10-20ps hit timing)
- Noble liquid based
 - High granularity challenge ightarrow read-out electrodes, feedthroughs
 - Noble liquid properties under high ionization rates
 - · Cryostats with minimal material
 - Timing performance (down to 20ps for showers)
- Gaseous detectors based
 - Homogeneity, mechanical structures, reliability

Presented projects clearly not exhaustive! Please contact us, if you find important ideas missing! The next step is to further evaluate the challenges in each field and converge on proposals of R&D projects

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<u>Ref 2</u>

1st Workshop on R&D for Experimental Technologies Working Group 6: High Speed Links

Development of Links is highly dependent on:

- Machine being considered
 - Radiation environment
 - HL LHC: > 100 Mrad
 - CLIC: < 1 Mrad
 - FCC: > 1Grad
 - Timing requirements (beam structure)
- Type of detector (e.g. Pixel-Detectors, Trackers or Calorimeters)
 - Data rates / aggregation
 - Distances

Ref 3

Power consumption

If a projection can be made in the horizon of 2020 to 2025 the HEP systems should be targeting 20 - 40 Gb/s systems:

Well within the capability of today's FPGAs

Important for Links and ASICs to maintain compatibility with FPGA technology





Radiation resistance is not changing with new generations of opto electronic components (in our observations)

- Commercial high speed driver ASICs are usually SiGe-BiCMOS based (not CMOS)
- Data rates in HEP have historically been limited by the serializer (Rad-hard GOL or GBTx)

Time-division multiplexing hits a limit around 25-50Gbps (VCSELs)

- Higher bit-rates achieved through
 - Wavelength multiplexing
 - Multi-level signaling (PAM-4 and others)

More on future technologies to take the next step in another talk...

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<u>Ref 3</u>

1st Workshop on R&D for Experimental Technologies Working Group: ASICs and IC Technologies

ASICS and IC Technology Issues Appear Across the Board

List of topics were drawn up:

- Pixel detector readout (hybrid) monolithic is in Si WP
- Strip detector readout
- Calorimeter readout
- Muon Detector readout
- Control and monitoring Slow control ADC, DACs etc
- Trigger generation
- Fast timing
- Power supply distribution
 - DCDC
 - Linear regulators
- Serial powering

<u>Ref 4</u>

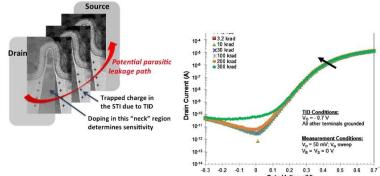


1st Workshop on R&D for Experimental Technologies Working Group: ASICs and IC Technologies

Start to test 28nm and FinFET devices to understand the physics

Put in the place the necessary infrastructure to allow us access to these processes

- NDA's
- Technology files and support
- Foundry access
- Training



ASIC interconnect technology (TSV, bump bonding) should be included in the work package as it depends on or is inseparable from the ASIC Technology chosen

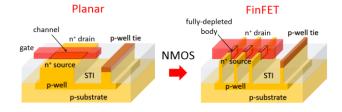
Below 28nm FinFETs become the workhorse

- Increased gain, faster switching, lower leakage current
- Increased layout restrictions (already at planar 28nm)
- Radiation tolerance largely unknown (although initial indications not promising)

<u>Ref 4</u>

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1st Workshop on R&D for Experimental Technologies References

Thank you for your attention.

For more details, consult the excellent presentations at:

https://indico.cern.ch/event/696066/

- 1. <u>https://indico.cern.ch/event/696066/sessions/268661/attachments/1618325/2573737/wg1_slides_all.pdf</u>
- 2. <u>https://indico.cern.ch/event/696066/contributions/2926622/attachments/1618427/2573489/EPWG3-WS1-Calorimetry-20180316.pdf</u>
- 3. <u>https://indico.cern.ch/event/696066/contributions/2926624/attachments/1618459/2573474/wg6presentatio</u> <u>n.pdf</u>
- 4. <u>https://indico.cern.ch/event/696066/contributions/2931535/attachments/1618581/2573769/MCampbel_ICTe</u> <u>chnologies16March2018.pdf</u>

