Update of Cold Electronics Development at BNL

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BROOKHAVEN NATIONAL LABORATORY
JANUARY 29TH, 2019
Outline

- Introduction
  - FE Readout Electronics Production for ICEBERG/APA7

- Cold Electronics Development
  - Study of FE ASIC Ledge Effect and Development Plan
  - ADC ASIC Test Board
  - FEMB Development Plan and 40% APA Integration Test

- Signal Feed-through and Cold Cable
  - Investigation of Cold Data Cable Cross Section
  - Cold Data Cable Development
  - HEPA Filter for WIEC

- Warm Interface Electronics
  - WIB Development

- Summary
ProtoDUNE-SP had a successful beam data taking from September to November 2018.

**Highlight of cold electronics performance in ProtoDUNE-SP**

- With drift 180kV and nominal bias voltages
  - 99.74% (15,320 of 15,360) of TPC channels are active regardless of noise performance
    - Only 4 inactive FE channels, others can be attributed to TPC etc.
  - 92.83% (14,259 of 15,360) of TPC channels are good with excellent noise performance (ENC < 800e-)
    - A probable cause of the higher noise is from other TPC instrumentation, to be studied.

- Noise performance with drift and bias on
  - ENC of collection (X) plane (5,473 of 5,760 channels): 565 ± 60 e^{-}
  - ENC of induction (V) plane (4,347 of 4,800 channels): 662 ± 56 e^{-}
  - ENC of induction (U) plane (4,439 of 4,800 channels): 651 ± 54 e^{-}
ProtoDUNE-SP front-end electronics serve as basis for further development of DUNE far detector

- Integration tests will be used to validate various new developments
- ICEBERG at Fermilab, APA7 at CERN and 40% APA at BNL

FE readout electronics production for ICEBERG/APA7

- **10 ProtoDUNE-SP FEMBs** have been produced, tested, installed and checked out on ICEBERG TPC at Fermilab
  - Including signal feed-through assembly and warm interface electronics
  - See Dave’s talk in plenary session Monday afternoon
- **20 ProtoDUNE-SP FEMBs** (plus spares) have been produced and tested, will be shipped to CERN this week
- **10 SBND FEMBs** with COTS ADCs (plus spares) have been produced, will be tested and shipped to Fermilab in February
Study of FE ASIC Ledge Effect (1)

- Ledge effect of FE ASIC was observed in ProtoDUNE-SP data taking
  - A mitigation with 900mV baseline has been proposed and implemented on 10/11/2018
  - See Shanshan’s slides in SP TPC Electronics Consortium meeting on 10/15/2018
    - [https://indico.fnal.gov/event/18686/](https://indico.fnal.gov/event/18686/)
- Further evaluation tests were carried out to study the ledge effect
  - Tests on V4* (MicroBooNE), P1, P2 (ProtoDUNE-SP) and P3 FE ASICs
- Ledge effect shows up from P1 FE ASIC
  - Significant change of design rules from V4* (2013) to P1 (2016)
  - Add more bias current options (1nA and 5nA)
  - GOhm input resistor is necessary to bring up P1 FE channel
Study of FE ASIC Ledge Effect (2)

- Ledge effect comes from circuit related to FE pre-amplifier
  - Change of gain, peaking time, AC/DC, buffer On/Off doesn’t help
  - Changing FE bias current setting changes ledge threshold slightly
  - Ledge threshold at 200mV FE baseline is as low as ~60fC.
  - Ledge threshold is significantly increased with 900mV FE baseline

- Ledge threshold can be further improved or eliminated with input resistor
  - Lower the resistance, the ledge threshold of both 200mV/900mV increases
    - FE ASIC can’t work properly with < 270 MOhm resistors at input
  - With 2 GOhm resistor at FE input (900mV FE baseline)
    - 97.6% (250 of 256) channels without ledge up to 1pC
    - 2.4% (6 of 256) channels with ledge effect, with threshold > 250fC
  - With 1 GOhm resistor at FE input
    - 8 FE ASICs (128 channels) were tested with quad-socket FE test stand
    - No ledge effect was observed at 900mV FE baseline
  - With 470 MOhm resistor at FE input
    - Ledge threshold > 200fC at 200mV FE baseline
    - No ledge effect was observed at 900mV FE baseline
Study of FE ASIC Ledge Effect (3)

- **Histogram of ledge threshold at 200mV FE baseline**

- **Histogram of ledge threshold at 900mV FE baseline**

2019/01/29  
H. Chen - DUNE Collaboration Meeting
Study of FE ASIC Ledge Effect (4)

- Ledge threshold can be further improved or eliminated with input resistor
  - With 470 MOhm resistor at FE input
    - Ledge threshold > 200fC at 200mV FE baseline
    - No ledge effect was observed at 900mV FE baseline
  - Side effect: baseline shift which will reduce dynamic range slightly
    - 7.8mV/fC, 2us: FE baseline shift less than 50mV
    - 14mV/fC, 2us: FE baseline shift ~100mV

- Development plan
  - P4 FE ASIC development will examine past designs, particularly the V4*, to address the ledge effect
    - Will implement SE-DIFF converter, perform extensive simulation with better models
    - New ASIC engineer will join the BNL and start to work on FE ASIC design in Spring
  - More P2 and P3 FE ASICs have been shipped to MSU, where additional evaluation tests will be performed
DUNE cold ADCs have been fabricated, a cold ADC test board is being developed for evaluation.

ADC ASIC Test Board

- Detector input
- External input
- Input from LArASIC or external, selectable

SAMTEC TSW

Power socket

LDO TPS74201

LDO TPS74201

LDO TPS74201

LDO TPS74201

LDO TPS74201

Analyzer III

ADC test input

Single ADC/Socket test board

Charge injection

GbE

FPGA

$FP module

FPGA Mezzanine

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Single Cold ADC Test Board

- Use **ProtoDUNE-SP FPGA mezzanine** as digital readout and slow control
  - Similar to ProtoDUNE-SP single ADC screening test board
  - FPGA readout through GbE or WIB
  - Layout will support population of packaged chip and wire bonding of bare die
  - LQFP128 socket has been identified for future development

- Schematics design has been completed
  - Layout design is ongoing after ADC ASIC package information became available on 01/03/2019
  - Layout design is expected to be finalized by the end of this week
  - Firmware design is ongoing based on the firmware of ProtoDUNE-SP single ADC screening test board
FEMB Development Plan and 40% APA Integration Test

- FEMB design will use P3 FE ASIC and cold ADC ASIC
  - FPGA mezzanine will be used before COLDATA ASIC becomes available
  - FPGA mezzanine will have two FPGAs to accommodate interface with cold ADCs, also facilitate the interface definition for COLDATA mezzanine
  - Schematics design will be finalized after the initial test of cold ADC in the lab

- 40% APA at BNL has been used for integration test
  - An unexpected damage occurred in mid December, broke some wires on 40% APA
  - An attempt was made to salvage the 40% APA in past three week, including repair of mesh layer and cut of loose wires
  - > 85% wires are usable, cold test was performed to confirm the ENC performance
Cold Data Cable Installation on ICEBERG

- Ken was at Fermilab for the ICEBERG cold electronics installation on 11/12/2018
  - It was noticed the cable strain relief is very tight for ICEBERG cold data cable
  - It was not an issue for ProtoDUNE cold data cable installation at CERN

- Measurements on 11/13/2018
  - Cable strain relief opening: 18.42mm x 3.81mm
  - ProtoDUNE cold data cable: 18.29mm x 4.19mm
  - ICEBERG cold data cable: 19.81mm x 4.45mm
  - Big difference in width > 1.5mm

- Ken was at Fermilab for the ICEBERG cold electronics debug on 01/14/2019
  - One FEMB was working intermittently before Xmas holiday
  - Further debug test confirmed the issue is not from FEMB or WIB, should be between feed-through and cold cable in early January
  - It was found the cold cable cable was pinched between the aluminum parts of the cable strain relief
  - The cable was installed without Teflon wrap due to the tight fit in the cable strain relief in November

- Why do we see big difference between ICEBERG cold data cable and ProtoDUNE cold data cable?
- 7 meters cold data cable was ordered from BNL in 2016
- 2.5 meters cold data cable was ordered from Fermilab in 2018
Communication with Samtec

- Difference between CCS-192589 and CCS-199713

- ProtoDUNE design CCS-192589 used a standard 26awg 7 stranded conductor and a thinner Cu Foil shield tape

- ICEBERG design CCS-199713 uses a larger 26awg 19 stranded conductor and a thicker Cu Foil shield tape to improve SI for acceptable conditions
Why was CCS-199713 used?

- In late 2017 and early 2018, the **cable routing option** was discussed extensively
  - It was considered to route cable along the cryostat wall before the baseline option to route cable within APA frame was adopted
  - Routing cable along the cryostat wall will need 35 meters long cold cable

- We have been working with Samtec to identify possible solutions for 35 meters of cold cable in 2017
  - Two options, solid core and 19 strand cable, were developed by Samtec, tested and verified at BNL
  - Due to the production difficulty to handle solid core, Samtec prefers to use 19 strand twin-ax cable
  - Samtec updated the drawing without notifying us on 10/18/2017
  - Fermilab order in 2018 was to add length options based on the drawing updated in 2017

- 11 cold data cables have been ordered in February 2018 for cable routing test at PSL/Ash River
  - These cables were built with CCS-199713 with large cross section
  - **The test at PSL/Ash River was valid**

- Path forward
  - With current baseline option to route cable through APA frame, we have the option to use CCS-192589 with smaller cross section, which saves ~10% of space
Cold Data Cable Development (1)

- Connector failure has been observed with cold data cable in ProtoDUNE-SP
- Various options have been discussed (in July CE workshop and September collaboration meeting) to improve the connection between connector and cold data cable

Add two wings to the male connector PCB

Surface mount standoff

A notch cutout in PCB

Surface mount nut
Cold Data Cable Development (2)

- Samtec developed the cold data cable drawing per new requirements
- A testing fixture to verify connector connection reliability is being built
- Order of new cold data cable arrived, connection reliability test will be performed in coming weeks

X, Y and Z directions adjustable simulating assembly misalignments.
It was found from ProtoDUNE-SP operation that dust was accumulated on warm interface electronics boards.

Plan to implement **air filter** to minimize the dust accumulation and potential risk to warm interface electronics boards:
- The dimensions of the fan plenum on CE crate is 7.468” x 5.3”
- If we make a straight tunnel for supporting the air filter, we can size the air filter to 7 3/8” x 5 1/4”

Samples of air filter have been procured, with different thickness options:
- The air flow and thermal management will be tested once the WIEC was shipped back from Fermilab
Warm Interface Electronics (1)

- ProtoDUNE-SP WIB has been revised slightly for evaluation of CRYO ASIC
  - FEMB clock distribution: two clocks distributed to each FEMB bypassing FPGA
  - FEMB power: a linear regulator added to feed power down to FEMB
  - FEMB communication: two IO signals added to FEMB data cable
  - Keep the compatibility with other options (Cold ADC, COTS ADC etc.)

- Interface to FEMB has been defined
  - Being reviewed by Hawaii and SLAC groups
  - Purchase order has been processed, will be released once we get confirmation
DUNE far detector will need 750 WIBs, FPGA is the main cost driver

Market survey has been carried out in past months
- Current Intel FPGA cost on ProtoDUNE-SP WIB is $1,360.6 each
- Xilinx Zynq+ offers a cost effective alternative, $799.77 each, with additional features, e.g. ARM, TCP/IP etc.

<table>
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<th>WIB</th>
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A WIB design based on Zynq+ FPGA is being fleshed out
WIB Design Considerations (2)

- Design is largely based on the ProtoDUNE-SP WIB
- Improved WIB to FEMB power distribution to allow better control and monitoring
  - Up to six supplies delivered to each FEMB
  - All supplies are monitored for current and voltage
  - All supplies can be controlled remotely
    - Enabled or disabled
    - Voltage adjustments are control by a 12bit DAC, the resolution and range are determined by WIB component population

- Power control and monitoring
  - Power sequencing, monitor and control for on board WIB power
  - Multiple configuration options for FEMB power (ProtoDUNE, SBND and DUNE Cold Data ASIC)
  - Multiple temperature sensors across WIB

Preliminary schematics design is complete, more inputs and requirements are welcome

- Broader collaboration on development of warm interface electronics is being actively pursued, e.g. Pitt, besides BU, UC Davis working on ProtoDUNE-SP
Summary

- ProtoDUNE-SP FEMBs and SBND FEMBs are being produced for integration test with ICEBERG/APA7

- Extensive study of ledge effect has been carried out, new FE ASIC design will address it

- ADC ASIC test board design is being finalized, will provide inputs to the FEMB design

- Cold data cable is using 16-strand configuration currently, new design with improvement on strain relief will be tested soon

- WIB has been updated for CRYO ASIC test, new development plans to use Xilinx Zynq+ FPGA