BNL FD DAQ TDR TASKS and Additional R&D

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Outline

Two Additional R&D Tasks

BNL Task Subscriptions

Dual-Phase CRO/LRO to FELIX

DP charge (CRO) and light (LRO) readout features:

- DP crates will send data via UDP/IP
- 240 CRO crates ∼2Gbps, 5 LRO crates ∼5 Gbps
  - total: 245 × 10 Gbps fibers to DAQ
- CRO is full-stream data, nominal 10× lossless data compressed

R&D task: develop and demonstrate FELIX as DP data receiver.

- Aggregate 10+ CRO per FELIX to reduce number of FECs.
- FELIX + direct links can assure "reliable UDP" unlike network switch.
- High degree of symmetry with SP for parts downstream of FELIX.
  - Especially in the FELIX + Commodity Computing design

Note, this task addresses Giles item #8 with alternative solution. It pushes the trigger primitive pipeline downstream but see next slide.

Dual-Phase Trigger Primitive Production on CPU

DP's μTCA crates do not produce trigger primitives.

R&D tasks:

- Develop DP trigger primitive algorithms.
  - $\rightarrow$ Algs $\sim$identical to SP, just different config parameters.
- Implement prototype algorithms on CPU.
- Evaluate their CPU requirements.
- Extend to consider GPU/FPGA/etc if needed.

Notes:

- Connects with Giovana's trigger farm item.
- This task is needed with Giles' "bump on the wire" design or with a direct CRO/LRO-FELIX link (previous slide). Also connects to Giles' #6 and #7.

BNL Software Tasks

- **Wire-Cell Toolkit signal and noise simulation:** continue developing DUNE support, including hardware addressing and data format, Geant4 input, LArSoft Integration.
- **Trigger primitives on CPU:** continue with design, prototype and evaluation of multi-threaded algorithms, SIMD optimization, ring buffer integration.
- **Hierarchical trigger system:** participate in design, prototyping and evaluating system architecture and algorithms.
- **Data Selector:** participate in design prototyping and evaluating of interface between event builder and ring buffer.

BNL Simulation and Studies Tasks

- Use **WCT noise+signal sim** to provide the **fodder** for developing and evaluating trigger primitive algs, driving vertical slice test (described later). Samples to include:
  - "Real" 3 seconds of data (ie, just noise + ^{39}Ar).
  - Artificially enhanced number of high-energy events.
- Develop **models for excess noise**
  - WCT supports **noise spectra as function of wire length**.
  - Provides model of **MicroBooNE** post-software-filter residual noise.
  - Needs support for **coherent noise models**.
  - Expect best models based on **ProtoDUNE** measurements.

  $\rightarrow$ Goal: understand noise repercussions for DAQ designs.

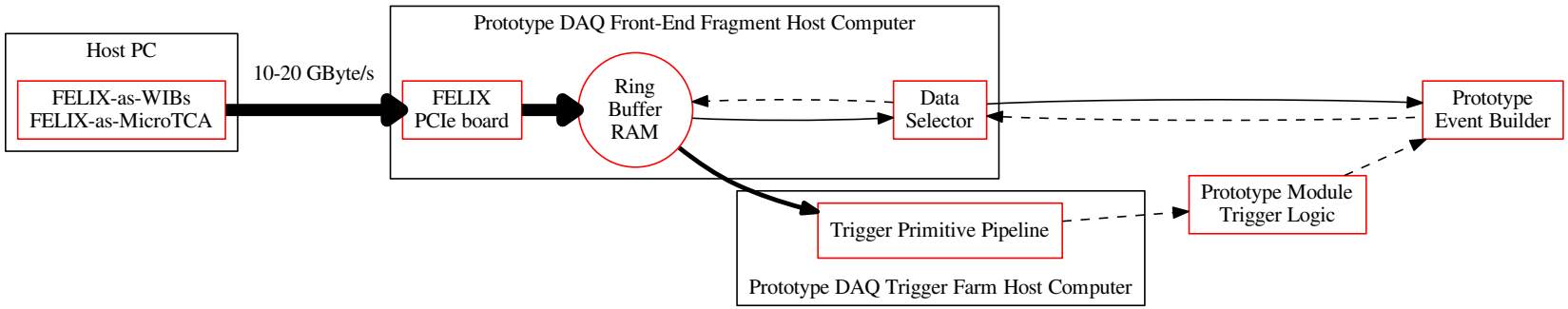
BNL FELIX Firmware Tasks

Develop firmware features for:

- **Receiving data from SP and DP**
  - "from SP" means from RCEs and direct from WIBs
- **DMA transfer to host RAM** into ring buffer structure suitable for sharing with host CPU threads.
- **Explore using FELIX FPGA for trigger** how much trigger primitive production pipeline can be offloaded to FELIX FPGA?

Note, we expect this work to continue to occur within the existing collaboration with CERN, Nikhef and others.

Vertical Slice Test Tasks



One possible VST configuration.

Bring together the FELIX-centric parts:

- Firmware: **FELIX-as-WIB** and **FELIX-as-μTCA** for faking data source, real prototype for data receiving and xfer to RAM.
- Use the **realistic signal+noise simulation** from WCT as "real" data.
- Use prototype **trigger primitive pipeline on CPU** code on "trigger farm".
- Install/test **prototype Event Builder** (ie, from DAQ backend WG)
- Assemble **prototype hardware**: host PCs, FELIX and network and connections.

Details on exactly where/who/how/what still needs working out.
Want to fit in with other plans on vertical slice tests.