# UK DUNE DAQ R+D Tasks

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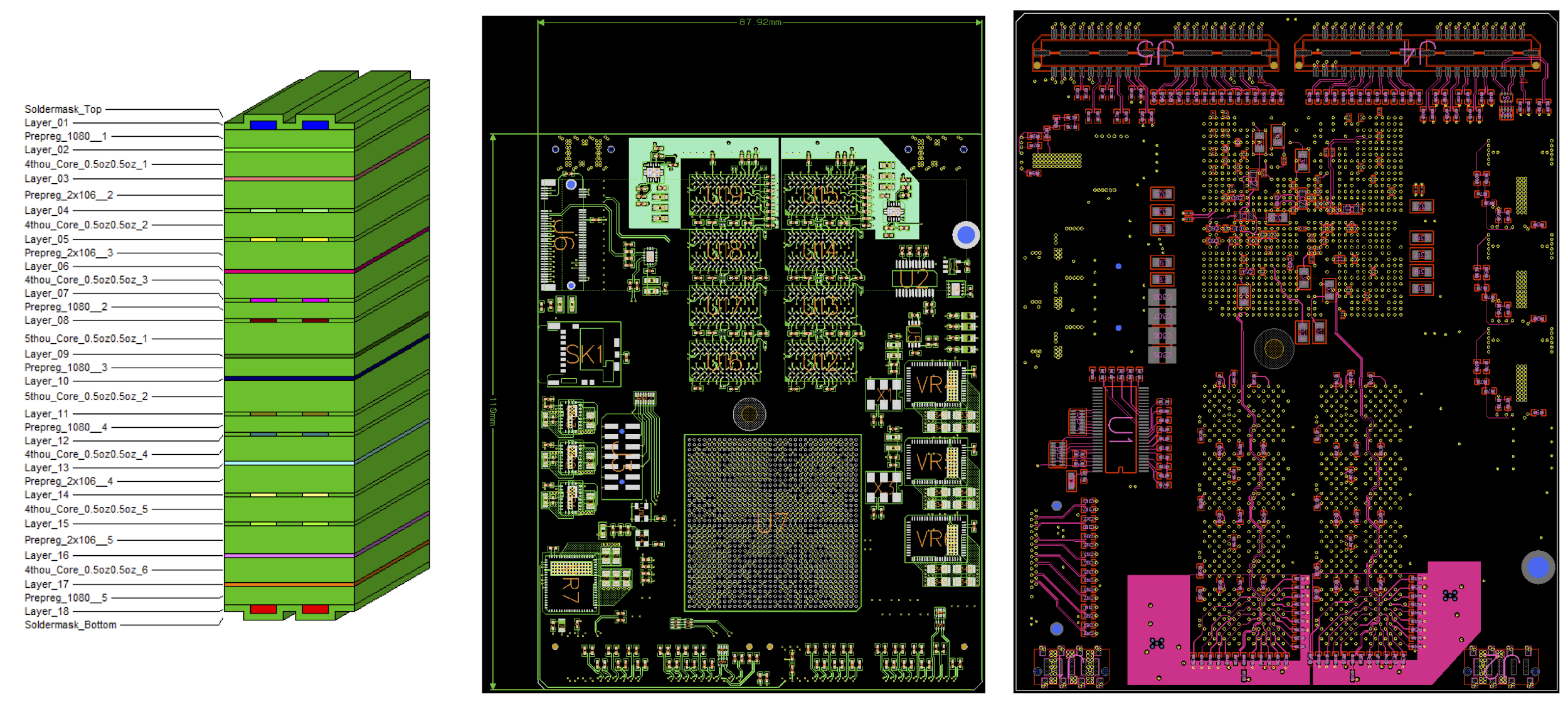
## Tasks:

1. **Produce DUNE Specific Data Transfer Module (DTM)**
2. **Vertical Slice Test Hardware(DPM Carrier)**
3. **Trigger Primitive Extraction and Data Compression**
4. **Data Flow**
5. **Photon Detector Trigger**

## A: **Produce DUNE Specific Data Transfer Module (DTM)**

We will complete the ongoing DTM development, delivering tested modules for the creation of test stands at CERN and institutes working on front-end pipeline algorithms. The DPM being developed is based around a large Xilinx Kintex UltraScale FPGA, has a large quantity of DRAM and can be fitted with an M.2 SSD. This task lasts six months. It will involve hardware development, but also firmware development for RAM and NVM buffer management.

* + Institutes: Oxford (+SLAC)
    - Leadership: Abi, Barr
    - Effort: Babak Abi (60%), Roy Wastie (50%), Peter Hastings (50%)
  + Deliverables:
    - 2 week deliverable: Schedule and task-list for testing.
    - 6 month deliverable: DPM boards
  + Sub-tasks
    - Complete DPM PCB development
    - Deliver tested modules
    - Develop firmware for RAM and NVM management
  + Comments
    - Involve other group(s) in firmware and testing?
    - Hardware currently on track (est. delivery Sept)
  + Reference: https://indico.fnal.gov/event/16877/contribution/1/material/slides/0.pdf



## B: **Vertical Slice Test Hardware(DTM Carrier)**

We will develop a low-cost carrier board for the upgraded DTM, capable of use as (a) a test platform for ProtoDUNE self-triggered readout, (b) testing and integration of cold electronics, (c) development platform for front-end pipeline algo work. This task will construct and maintain the hardware for a vertical slice of the path between the WIB and Felix (preferably using the new DTM+carrier, but using other hardware if not). This task will involve hardware, infrastructure firmware and control software development.

* + Institutes: Birmingham, Bristol, Oxford, UCL, RAL
    - Input from SLAC
    - Leadership: Watson(Staley?), Cussans
    - Effort: UCL Engineer(50%), Kostas Manolopoulos (firmware engineer), Babak Abi, Cussans(20%) then new Bristol PostDoc
  + Deliverables:
    - 2 week deliverable: Investigate feasibility of team working and schedule. Specify hardware and tasks for vertical slice test.
    - 3 month deliverable: Schematics and design review, initial PCB layout.
    - 6 month deliverable: DPM Carrier, infrastructure firmware.
    - 12 month deliverable: Demonstration of protoDUNE readout with DPM carrier(vertical slice-test of front-end hardware).
  + Sub-tasks:
    - Infrastructure firmware, software
    - Separate daughter-board for optics to WIB (?)
  + Comments:
    - Schedule is **extremely** tight
  + Reference: https://indico.fnal.gov/event/16877/contribution/0/material/slides/0.pdf

## C: **Trigger Primitive Extraction and Data Compression**

## We will set down detailed definitions of trigger primitives for SP and DP TPCs, along with the filtering / pre-processing steps needed to obtain them, based on simulation studies. We will implement the Trigger Primitive Extraction(TPE) pipeline in firmware (FPGA) and code (CPU / GPU) and compare the cost / performance of each approach under different noise assumptions, in preparation for the TDR design. We will demonstrate TPE in ProtoDUNE.

* + Institutes: Sussex, Bristol, Oxford, Edinburgh,RAL,UCL
    - (UK) Leadership: Peeters
    - Effort: A.Booth(Sussex),+others(Sussex), Miquel Nibot(50%,Edinburgh), Bristol PostDoc(when recruited), UCL PostDoc, Kostas Manolopoulos(RAL), Phil Rodrigues(Oxford,20%), C. Shepherd-T
  + Deliverables:
    - 3 month deliverable: Initial studies (FPGA,GPU,CPU)
    - 6 month deliverable: Trigger primitive definition, and rates from simulation studies. Compression algorithms in FPGA.
    - 12 month deliverable: Compare implementations in FPGA, GPU and CPU
    - 18 month deliverable: Implementation in vertical slice-test (either FPGA or GPU/CPU, as selected at 12 months)
  + Comments:
    - Overall leadership Klein (Penn)
    - Compression in collaboration with SLAC
  + Reference: Docdb 7920, https://indico.fnal.gov/event/15987/contribution/4/material/slides/0.pdf

## D: **Data Flow**

We will work with international partners to define a detailed dataflow architecture for the layer between the readout hardware and the DAQ back-end, based on a combination of transfer protocols, custom IO hardware (FELIX), and low-level control software for data-flow management. The performance of the system will be demonstrated in practice by constructing and running tests on a “slice” of the system between the readout hardware and the DAQ back-end.

* + Institutes: Oxford, RAL
    - (UK) Leadership: Barr
    - Effort: P.Rodrigues(50%,started), G.Barr(20%,started), Sankey, Shepherd-T, Harder, Dopke, Manolopoulos, Wilson
  + Deliverables:
    - Immediate Tasks: Initial network tests, plan “escalator” work, build team with Felix.
    - 6 month deliverable: Design of FE dataflow architecture, first performance tests.
    - 12 month deliverable: Vertical slice data-flow demonstrator operating for protoDUNE readout.
  + Sub-tasks:
    - Architecture
    - Low-level data-flow software
    - Test of I/O protocols and system performance
  + Reference: Docdb 7920, https://indico.fnal.gov/event/15987/contribution/4/material/slides/0.pdf

## E: **Photon Detector Trigger**

We will validate and use the Photon Detector(PD) simulation tools to assess the triggering capabilities of the PD, either stand-alone or in combination with TPC information. We will demonstrate the resource requirements for TPE based on the tools developed in task C and the software platform provided in task D.

* + - Institutes: Warwick, Edinburgh, UCL
    - Leadership: Haigh
    - Effort: J.Haigh(50%,ramp from protoDUNE), F.Muheim(20%)+Student, UCL PostDoc effort
  + Deliverables:
    - 6 month deliverable: Primitive definition, trigger capability from simulation
    - 12 month deliverable: Demonstration of PD trigger extraction in hardware
  + Comments:
    - Depends on output of firmware and software from front-end data flow and trigger primitive groups
  + Reference: https://docs.google.com/document/d/1v8FSayeTCfD7boDuhj--z7Hl4IApXACqmJIZYFqlzyU/edit