Introductory talk
UK plan for EOIs etc.

Draft

G.Barr 13.Apr.2018

Introduction

- Consortium-wide, we are formulating action-plans.
- We want activities for three main time-frames:
  - Up to Oct 2018 [start writing next STFC grant]
  - Up to 'Mar' 2019 [End of TDR writing]
  - Up to Sep 2019 [Don't lose momentum after TDR, complete UK pre-prod project]
- Very urgent for UK to get started
  - UK project – there are gaps in the DAQ plans and lists of work being done
  - We don't have much time; e.g. we must interleave with ProtoDUNE, teaching etc.
- Additional....
  - UK full project proposal deadline 18 Sept 2018.
  - This intensifies the urgency
  - Over weekend, will try to identify some 1-month and 2-month tasks from the discussion today to move ahead faster

Introduction

- Structure into tasks.
  - Loosely aligned with R&D project list at https://docs.google.com/spreadsheets/d/1k-T8ultywyvo9oPI-mHtLKzKsyrXnTigXeIunzXe4tY/edit?usp=sharing

  A) DPM (Hardware, firmware, software)
  B) DPM Carrier (Hardware, firmware, software, system tests)
  C) Front-end dataflow (software, systems tests)
  D) Trigger Primitive Extraction (software, firmware, system tests)
  E) Photon Detector System (software, firmware, system tests)
- Will now quickly go through C) – E) , then more time on A), B)

A) Hardware: DPM

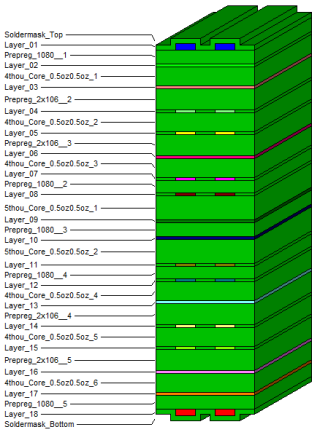
Scope

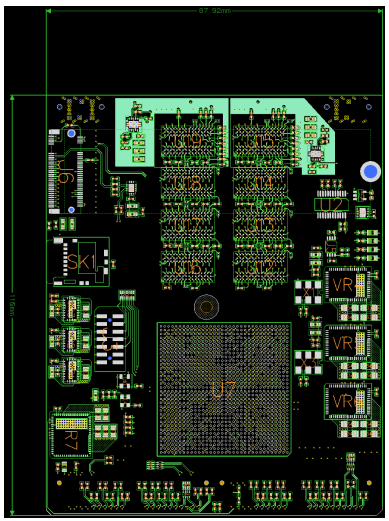
- Demonstrate capability of 10Gb/s board layout
- Experience with manufacture and testing.
- Upgrade Gen3 DPM to Ultrascale+
- Produce assembled and tested PCBs
- Firmware development for buffer management (DRAM and NVRAM)

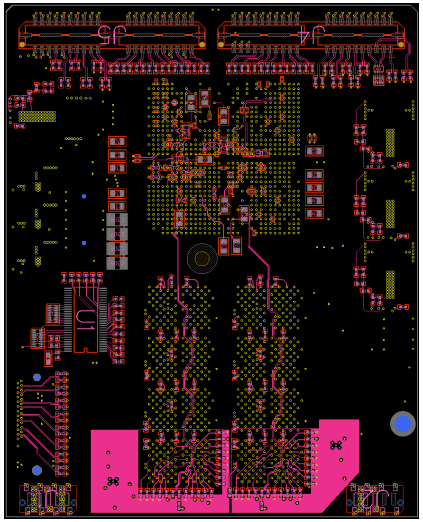
International References

O(1/month) phone meetings with SLAC

https://indico.fnal.gov/event/16877/contribution/1/material/slides/0.pdf







B) Hardware: DPM Carrier

Scope

- Develop carrier board for upgraded DPM

This is useful for

- Test platform for cold electronics
- Development platform for front-end algorithm development
- (thin) Vertical slice tests at protoDUNE
- Infrastructure firmware, control software

International

Extensive discussions with SLAC

References

https://indico.fnal.gov/event/16877/contribution/0/material/slides/0.pdf

Note: closely coupled to A):
In particular: testing firmware, experience using processors on Zynq U+,
specific firmware IP studies, design QA/QC for UK proposal,
experience with signal integrity checking, experience with manufacture
We can optimize which of these two packages some of these things are in

A) Could be fast-track (STFC proposal) B) is starting now, so likely ready later.

C) Trigger Primitive Extraction

Scope

- Define Trigger primitives for SP and DP
- Filtering and pre-processing steps (based on simulation)
- Implement trigger primitive extraction in (a) FPGA, (b) GPU, (c) CPU
- Compare cost/performance of each
- Study variations with noise
- Proof-of-concept: Demonstrate in protoDUNE

International

Sussex have made many presentations in Monday meetings

D) Front-end Data Flow

Scope

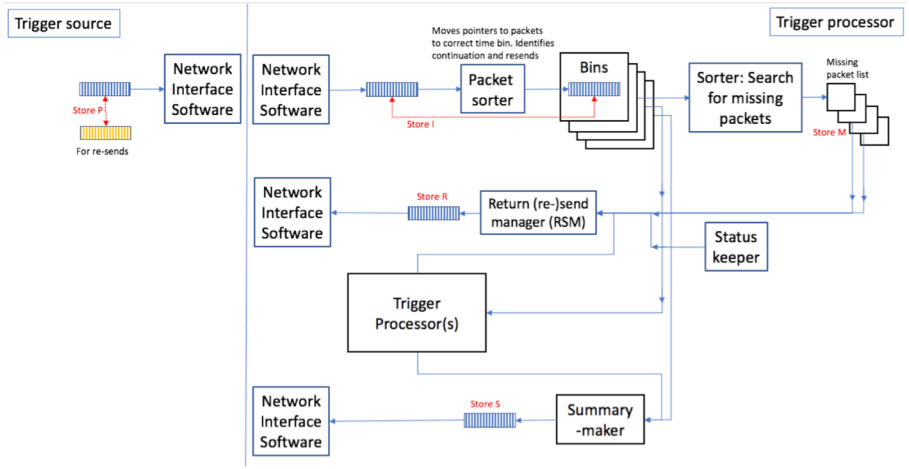
- Data flow architecture for FE
  - Transfer protocols
  - Use of custom I/O hardware (FPGA boards)
  - Low level data-flow software
  - Proof-of-concept
  - Here is where we max-out the throughput of the PCs

International

Recent discussions with Kurt, less recent discussions with Giovanna

References

Docdb 7920, https://indico.fnal.gov/event/15987/contribution/4/material/slides/0.pdf



E) Photon Detector

Scope

- Make photon detector versions of the key TPC DAQ concepts:
- Trigger decisions
- Storage & latency
- Hit primitives, robustness to noise
- Treatment of SNB-full-events

International

Recent discussions GB with Alex Himmel and JH with Alex Himmel

References

https://docs.google.com/document/d/1v8FSayeTCfD7boDuhj--z7Hl4IApXACqmJIZYFqlzyU/edit?usp=sharing

Backup Slides

Mapping from Alphabetic to Numeric Tasks

- Recent E-mails had numbered tasks (1..7)
  - … with Firmware as a separate task
    - Firmware probably best included with the task it services.
  - Split hardware into DPM and DPM carrier
    - One a mature tasks, the other new.
- 1) Firmware → Dispersed to other tasks.
- 3) Hardware → split to A,B
- 4) Trigger algorithm development → C
- 5) Data-link software →D
- 6) Vertical slice tests → Dispersed to other tasks.
- 7) Photon detector development → E