High speed X-ray detection for timing correlation spectroscopy type experiments

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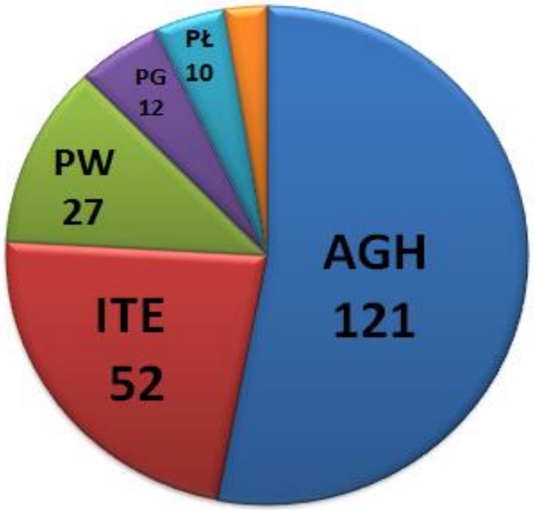
[3]Particle Physics Division, Fermi National Accelerator Laboratory, Batvia, USA
[4]Time Resolved Research, Argonne National Laboratory, Lemont, USA

AGH University of Science and Technology

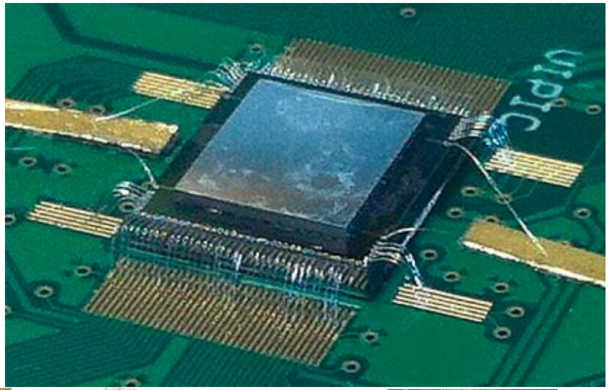
- One of the oldest and biggest Polish technical universities
- 16 faculties, 65 fields of study, more than 200 specializations
- Over 33 000 students
- Over 200 000 graduates
- 2 200 researchers including more than 650 associate and full professors
- Own attended campus area
- ~50% of budget from projects

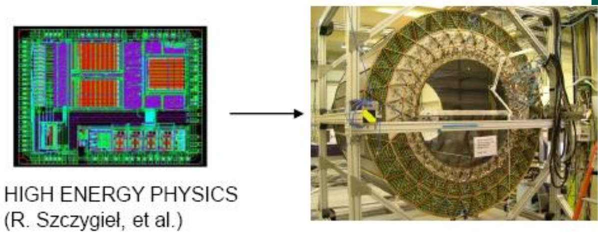
AGH University - ASIC Design

Universities and research institutes in Poland involved in Application Specific Integrated Circuit design

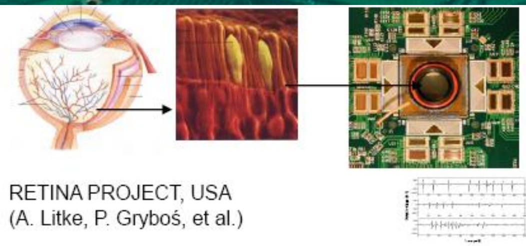


EUROPRACTICE statistics - chip design

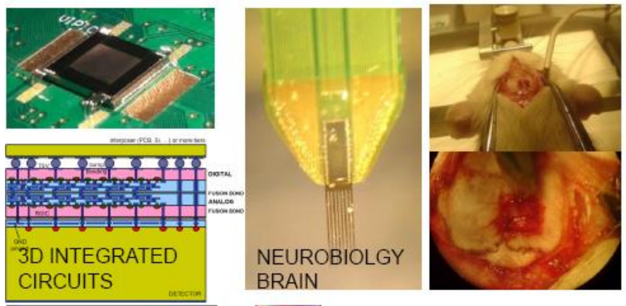


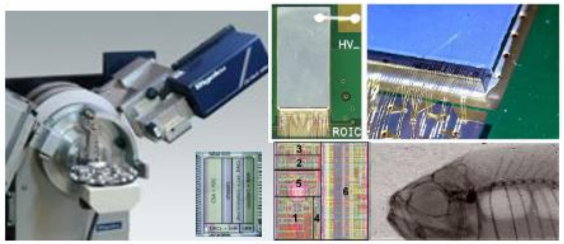


HIGH ENERGY PHYSICS
(R. Szczygieł, et al.)

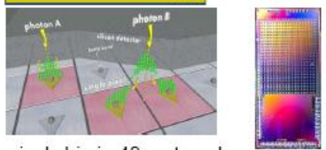


RETINA PROJECT, USA
(A. Litke, P. Gryboś, et al.)





ASICs for Rigaku Corporation, Japan



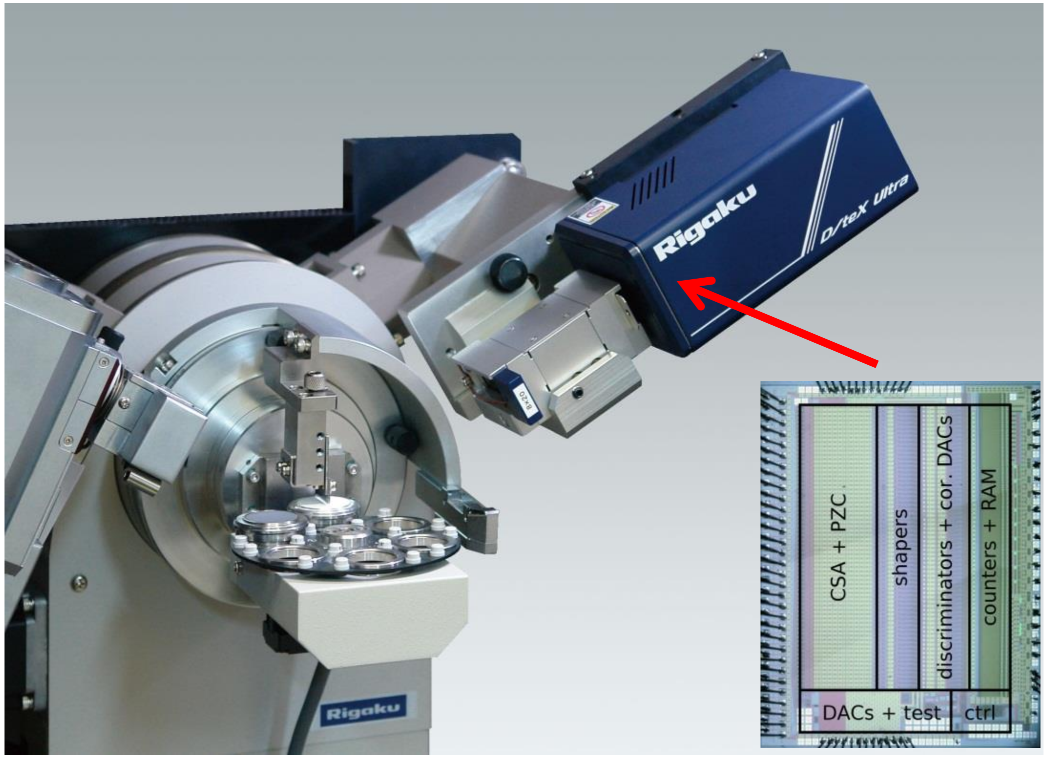
pixel chip in 40nm to solve charge sharing problem

AGH University:
- IEEE SSCS Chapter Poland
- Cadence Academic Network

Most of designs are mixed-mode ASICs
Technology used: 0.35 um => 40 nm or 3D

ASIC for High Energy Physics, X-ray Imaging, Neurobiology Applications

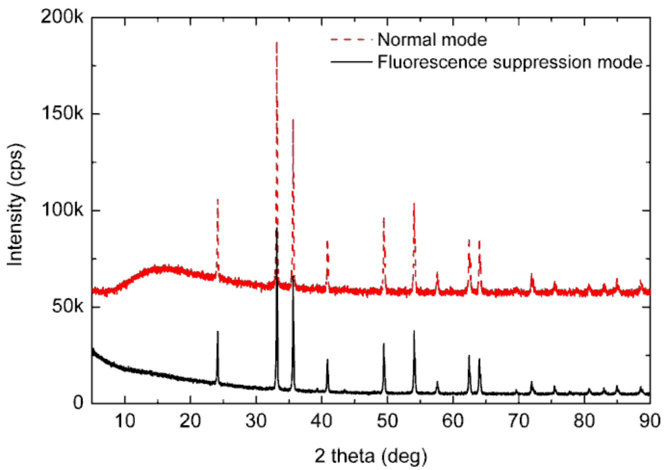
D/teX ultra module, Rigaku Corporation, Japan

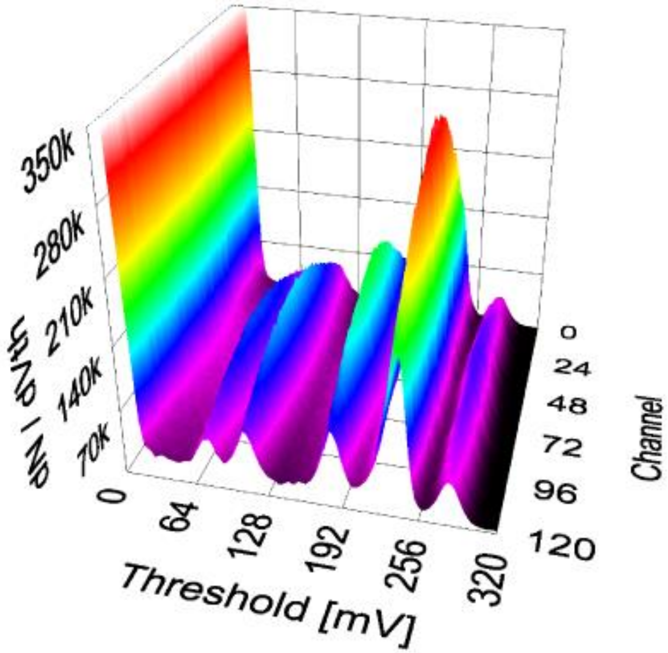


Technical specifications:

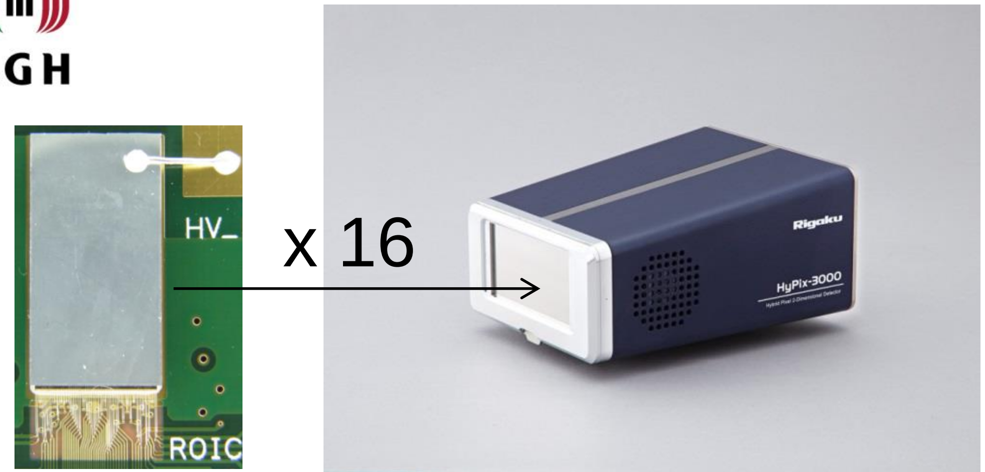
- Strip pitch: 0.1 mm
- Strip length: 20 mm
- Channel number: 128
- Count rate: $>1x10^6$ counts/strip/s
- Energy Range: 5 – 30 keV
- Dynamic range: 20 bits
- Trim DAC: 8 bits
- Energy resolution: < 25% (@8keV)
- Control board based on FPGA and a micro controller with ethernet link
- Dimensions: 93(H)×63(W)×151(L) mm^3

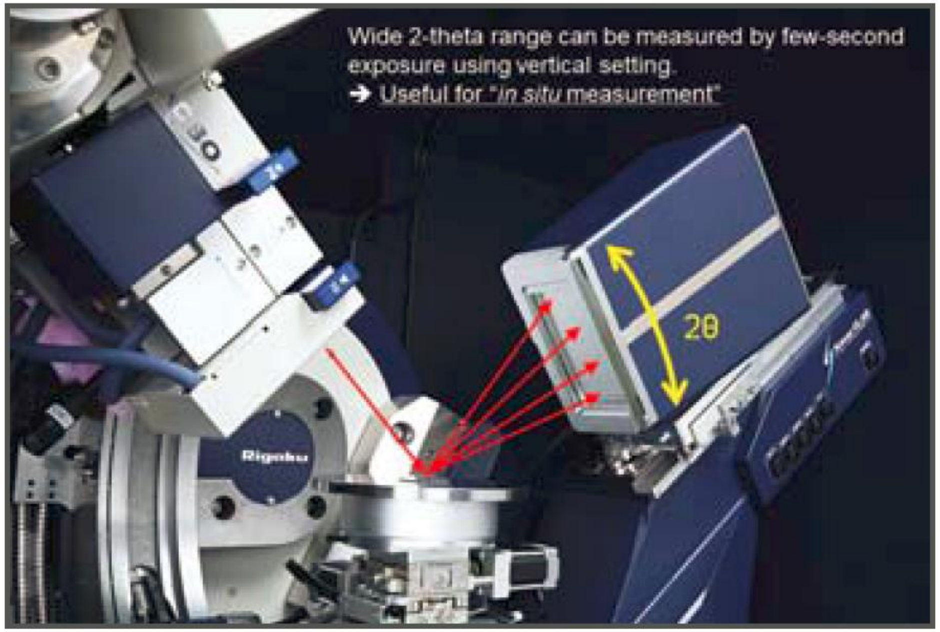
Replacing a conventional scintillation counter with D/teX Ultra on an in-house X-ray diffraction (XRD) system, **one can reduce the data acquisition time by 1/100**, or improve the sensitivity 100 times when the same data acquisition time is applied.





AGH chip PXD18k is used in by Rigaku Corporation, Japan





- Cement
- Chemistry
- Coatings
- Cosmetics
- Education
- Environmental
- Food & food ingredients
- Forensics & conservation
- Geology & minerals
- Materials science
- Metals & alloys
- Mining & refining
- Nanotechnology
- Petroleum & petrochemicals
- Pharmaceuticals
- Photovoltaic manufacturing
- Polymers, plastics & rubber
- Process control
- Semiconductor manufacturing
- Synchrotrons & beamlines

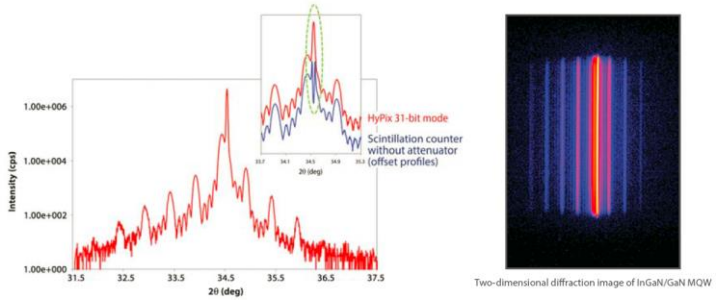
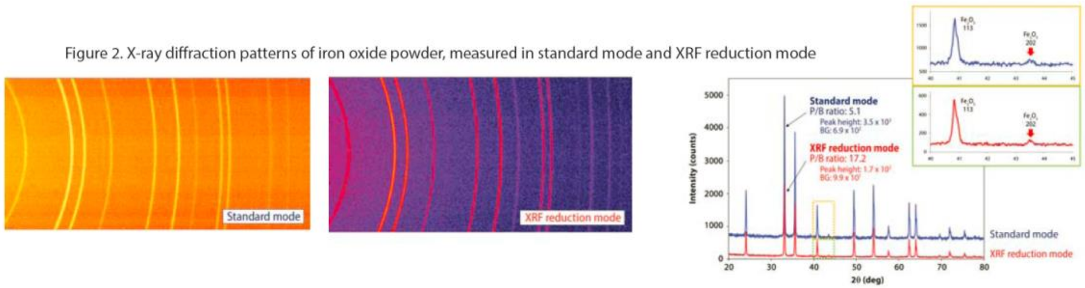


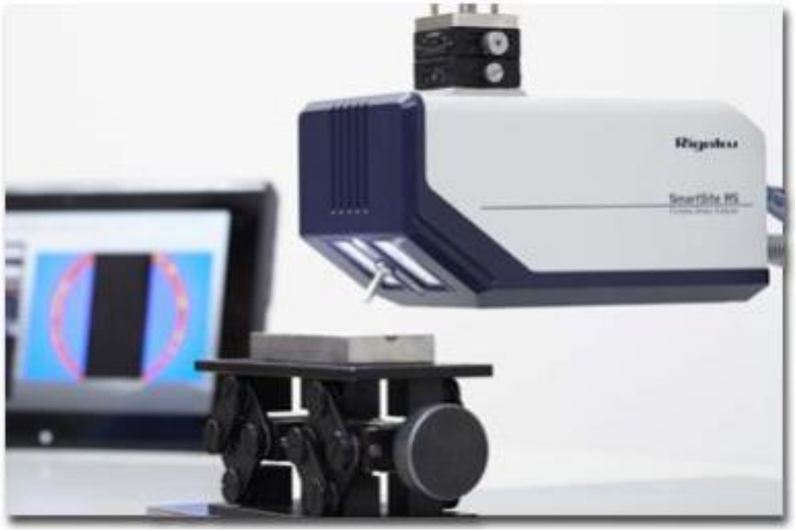
Figure 3. High resolution rocking curve profiles of InGaN/GaN MQW

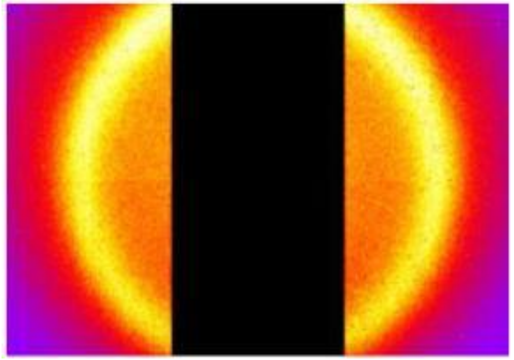
Figure 2. X-ray diffraction patterns of iron oxide powder, measured in standard mode and XRF reduction mode



PXD18k is used in Portable Stress Analyzer – SmartSite RS

The **SmartSite RS is the world's smallest portable stress analyzer** that is especially designed for field analysis. It enables to characterize residual stress of metal parts ranging from large construction projects to individual products, e.g. bridges, maritime vessels, aircraft, aerospace equipment, pipelines, heavy machinery and automobiles.



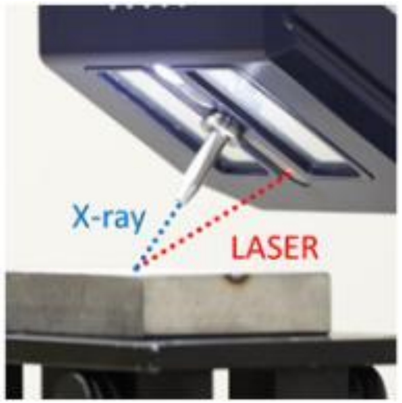


α-Fe 211 Debye ring

Applications

- Welded industrial products
- Aircraft & aerospace
- Marines
- Automobile

- Single exposure method
- High-speed 2-dimensional semiconductor detector
- 60 sec. (or less) for stress measurement

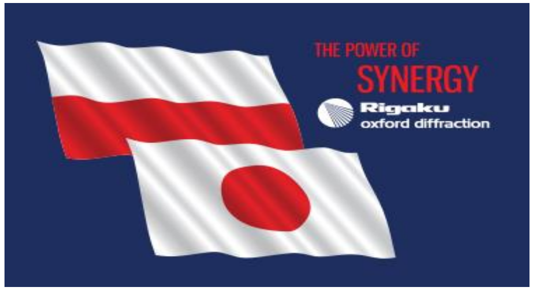


Arrangement of head unit and sample

www.rigaku.com

Rigaku Oxford Diffraction in Poland (Wroclaw)

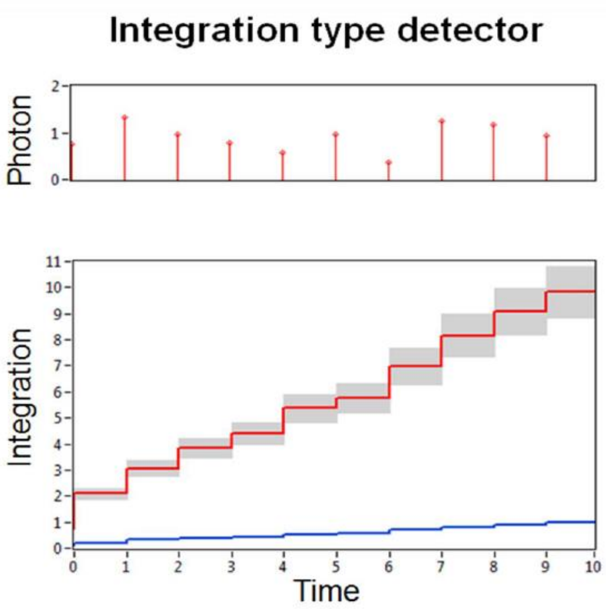
AGH

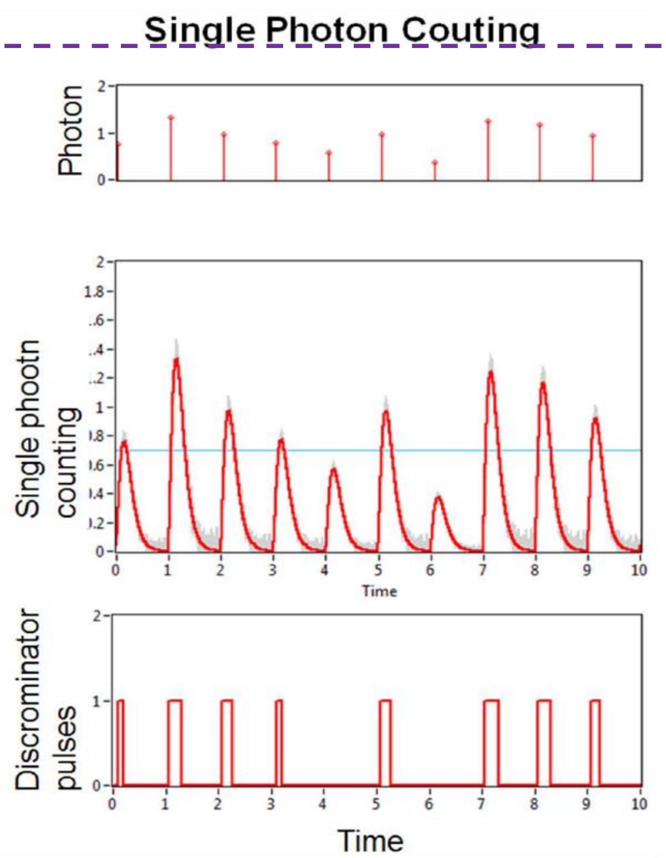


Rigaku Oxford Diffraction now offers the HyPix-6000HE Hybrid Photon Counting (HPC) detector. Like all HPCs, the HyPix-6000HE offers direct X-ray photon counting, single pixel point spread function and extremely low noise. The HyPix-6000HE HPC offers a small pixel size of 100 microns, which allows you to better resolve reflections for long unit cells as well as improving reflection profile analysis. The HyPix-6000HE has a high frame rate of 100 Hz, as well as a unique Zero Dead Time mode providing the ultimate in error-free shutterless data collection.

www.rigaku.com

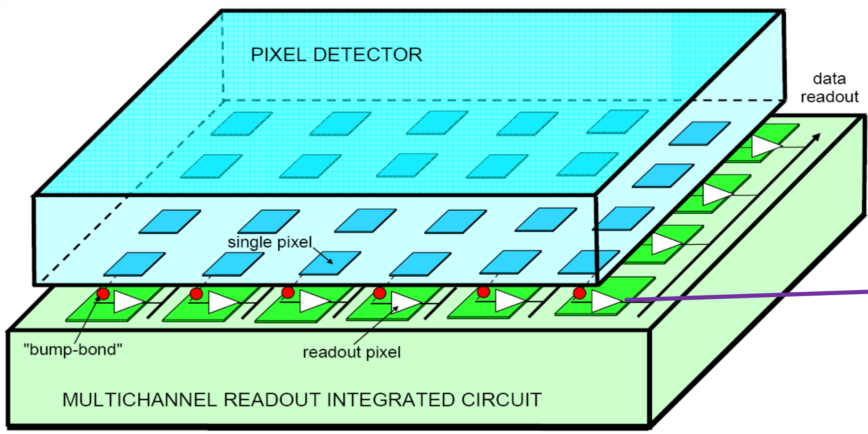
Readout type: Integration vs. Single Photon Counting

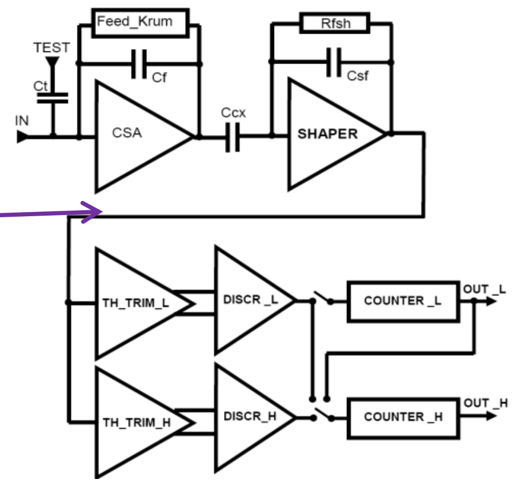




SPC:
- noiseless imaging,
- energy windows possible

Detector material suitable for given application and X-ray energy range: **Si**, Ge, GaAs, CdTe, CZT for IC designers : detector leakage current compensation + pulse polarity





Limitation:
1. Area
2. Power
3. Noise
4. Speed
5. Matching
6. Q sharing

Examples: Pilatus, Medipix, XPAD, Eiger, PIXIE, PXD18k, etc

www.agh.edu.pl

UFXC32k
Ultra Fast X-ray Chip with 32k channels

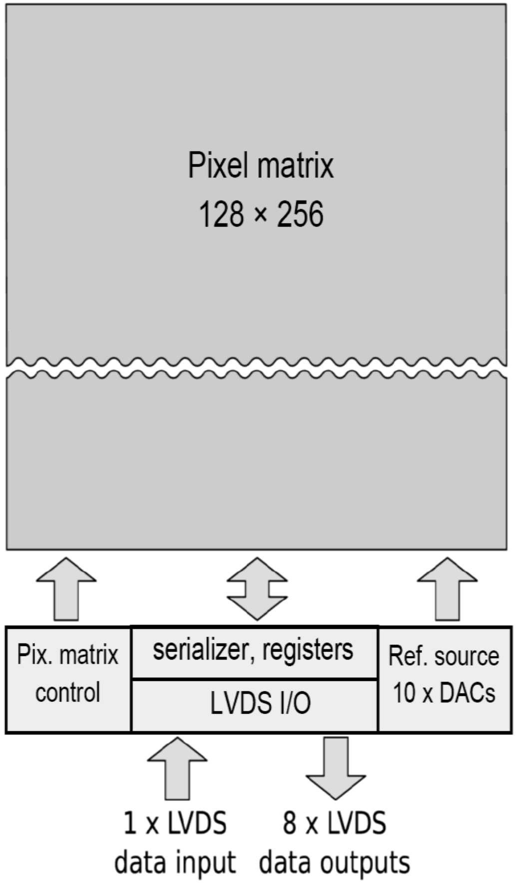
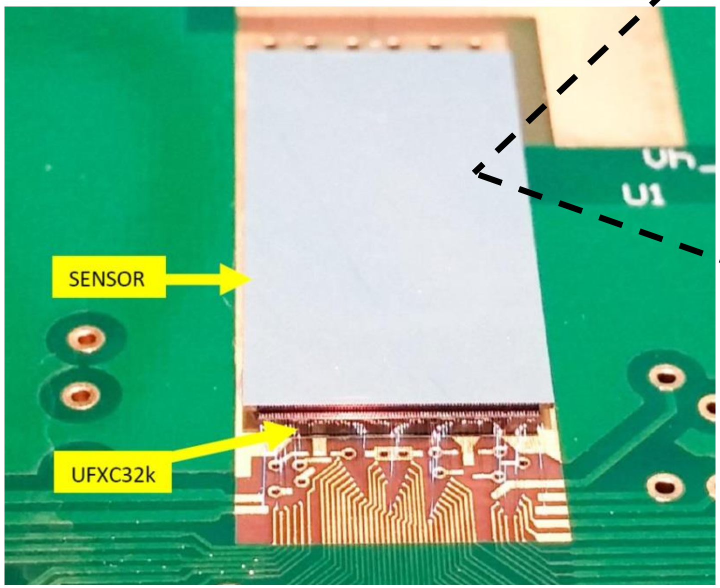
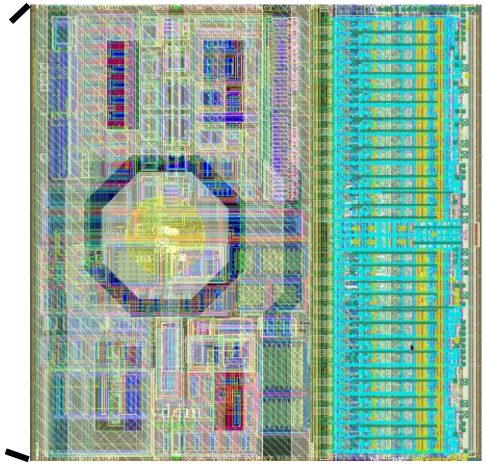


Photo of UFXC32k
with bump-bonded sensor



75 µm x 75 µm pixel layout

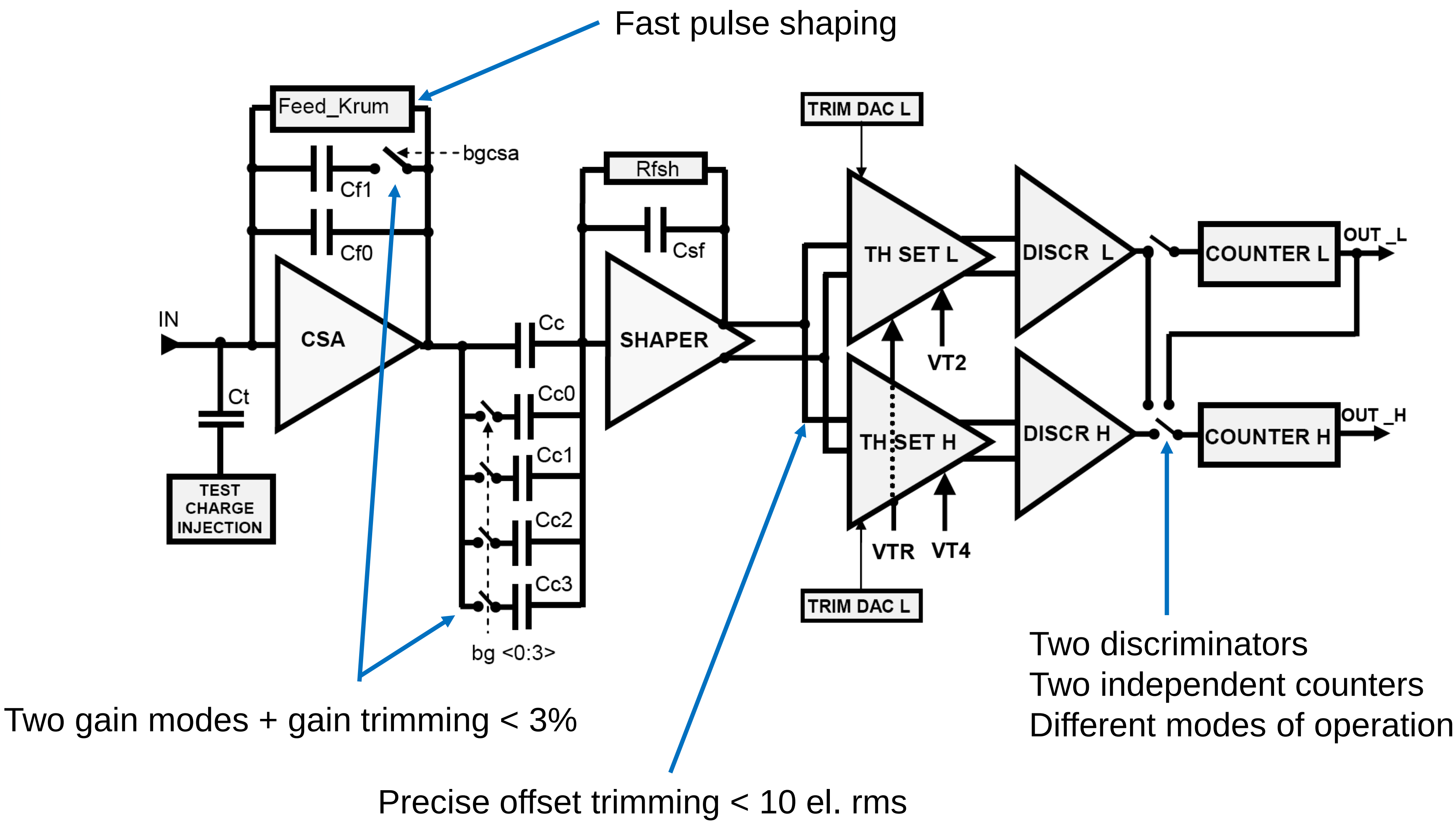


32768 pixels (75x75 µm^2)
CMOS 130 nm (~50M transistors)
chip size 9.63 × 20.15 mm^2

Functionality & parameters:

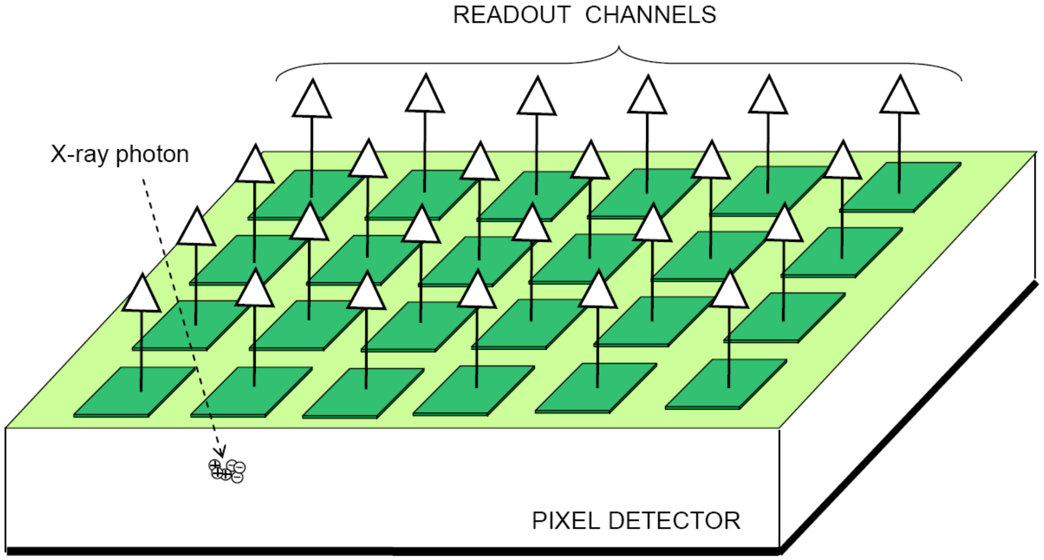
- single photon counting with energy window,
- input pulse: holes and electrons,
- good matching (offset and gain),
- high count rate, low noise
- continuous readout with high frame rate

UFXC32k
Single Pixel Architecture

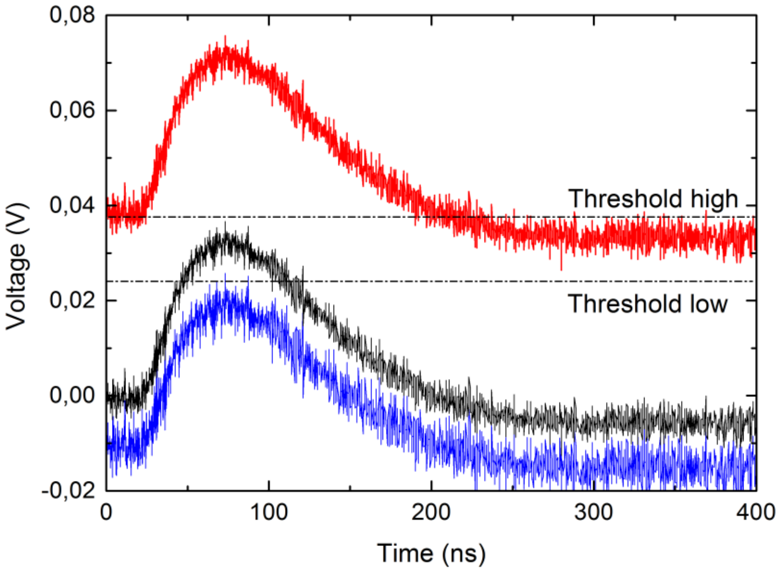


P. GRYBOŚ, P. KMON, P. MAJ, R. SZCZYGIEŁ: *32k channel readout IC for single photon counting pixel detectors with 75um pitch, dead time of 85 ns, 9 el rms offset spread and 2% rms gain spread*, Transactions on Nuclear Science; 2016 vol. 63, pp. 1155–1161

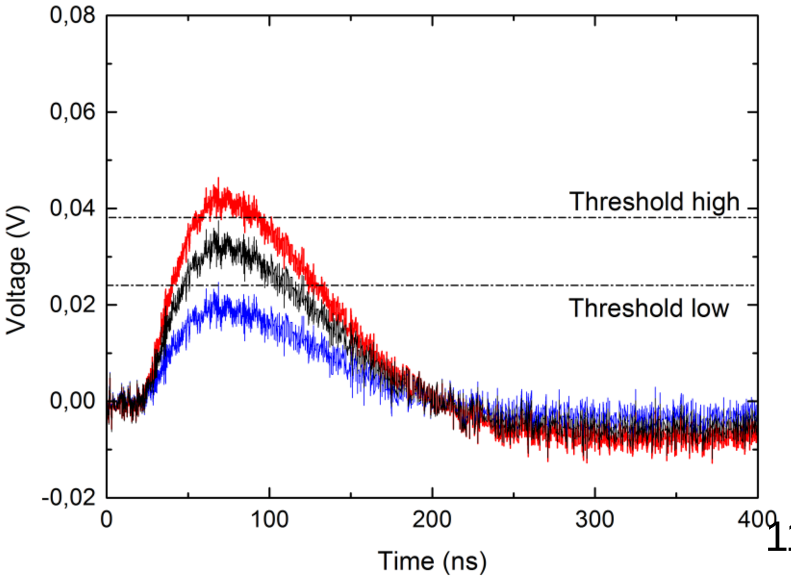
Problem of mismatch in pixel matrix



Example - offset spread

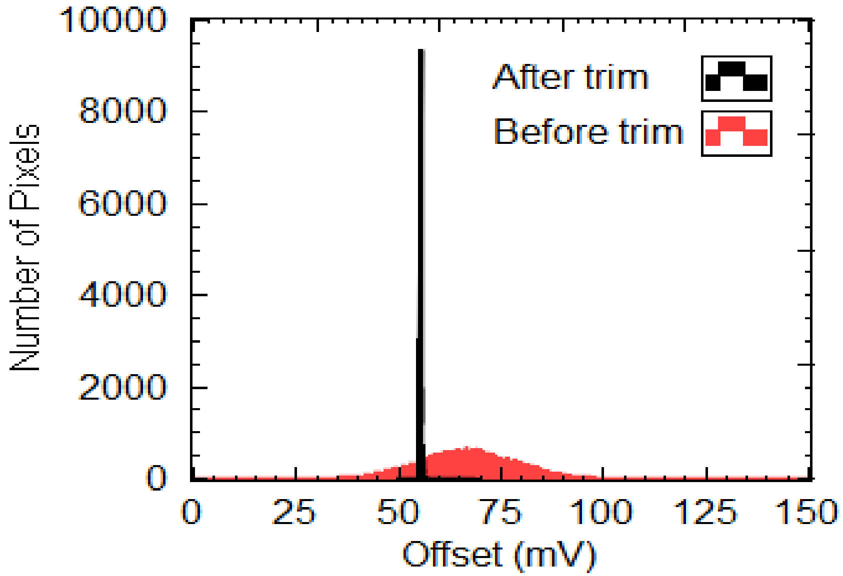


Example - gain spread



Trimming Capabilities

DC offsets before and after correction



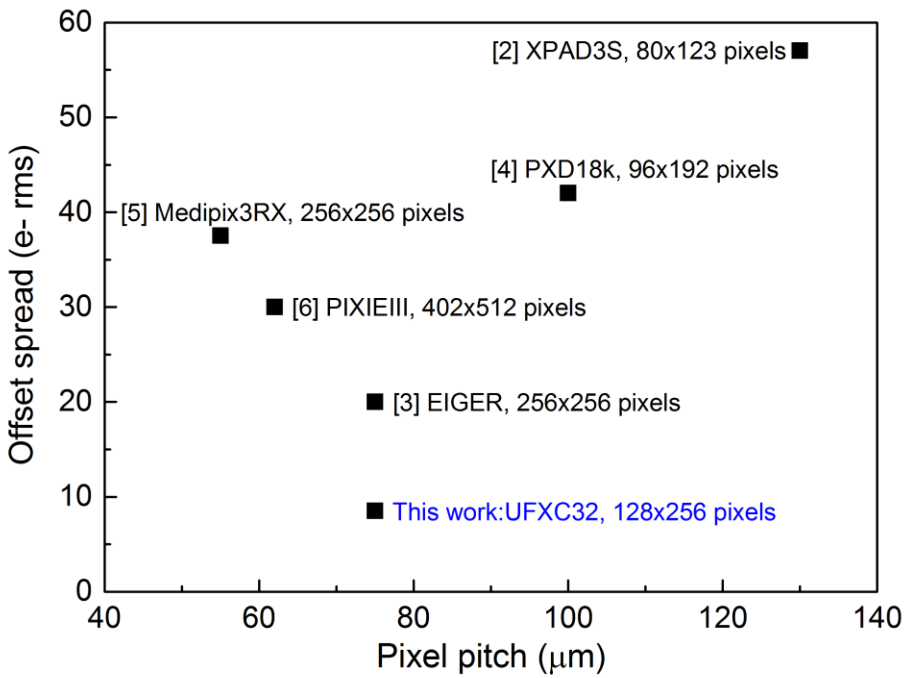
Before trim: sd = 12.1 mV

After trim: sd = 0.43 mV

nominal gain

After trim: sd = 8.5 e⁻ rms

Comments:
correction time: 20 - 60 sec

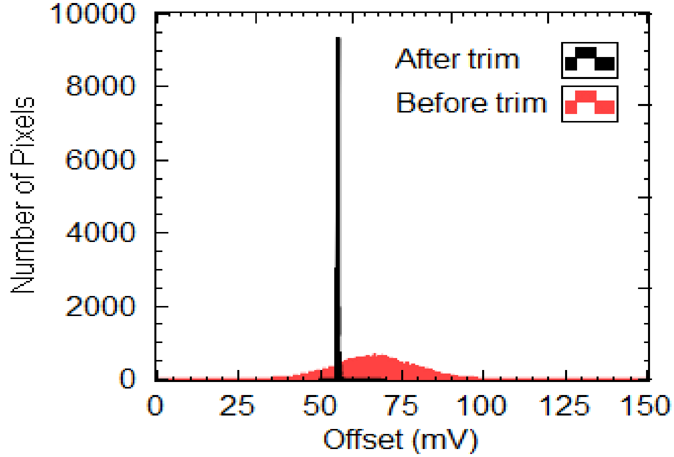


Offsets spread in large area integrated circuits working in the single photon counting mode vs. pixel pitch – reference and pixel matrix size is speficied for each solution.

Trimming Capabilities

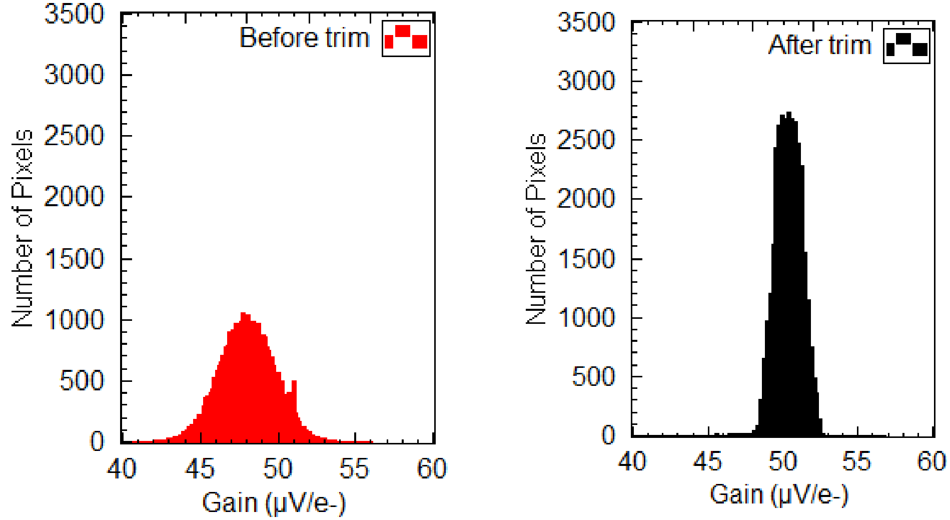
Measurements with X-ray source (8.4 keV)

Offset



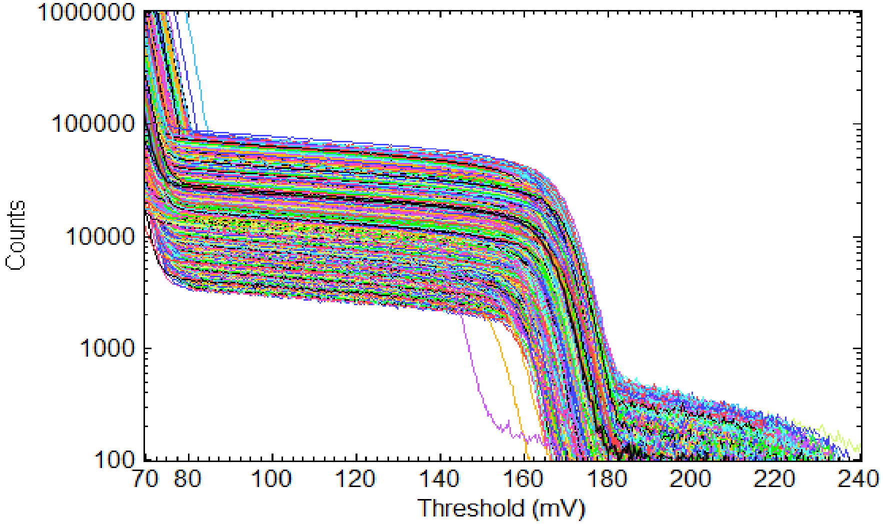
After trim: sd = 8.5 e^{-} rms

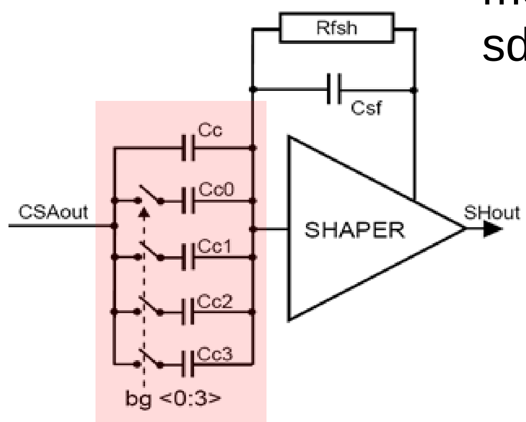
Gain



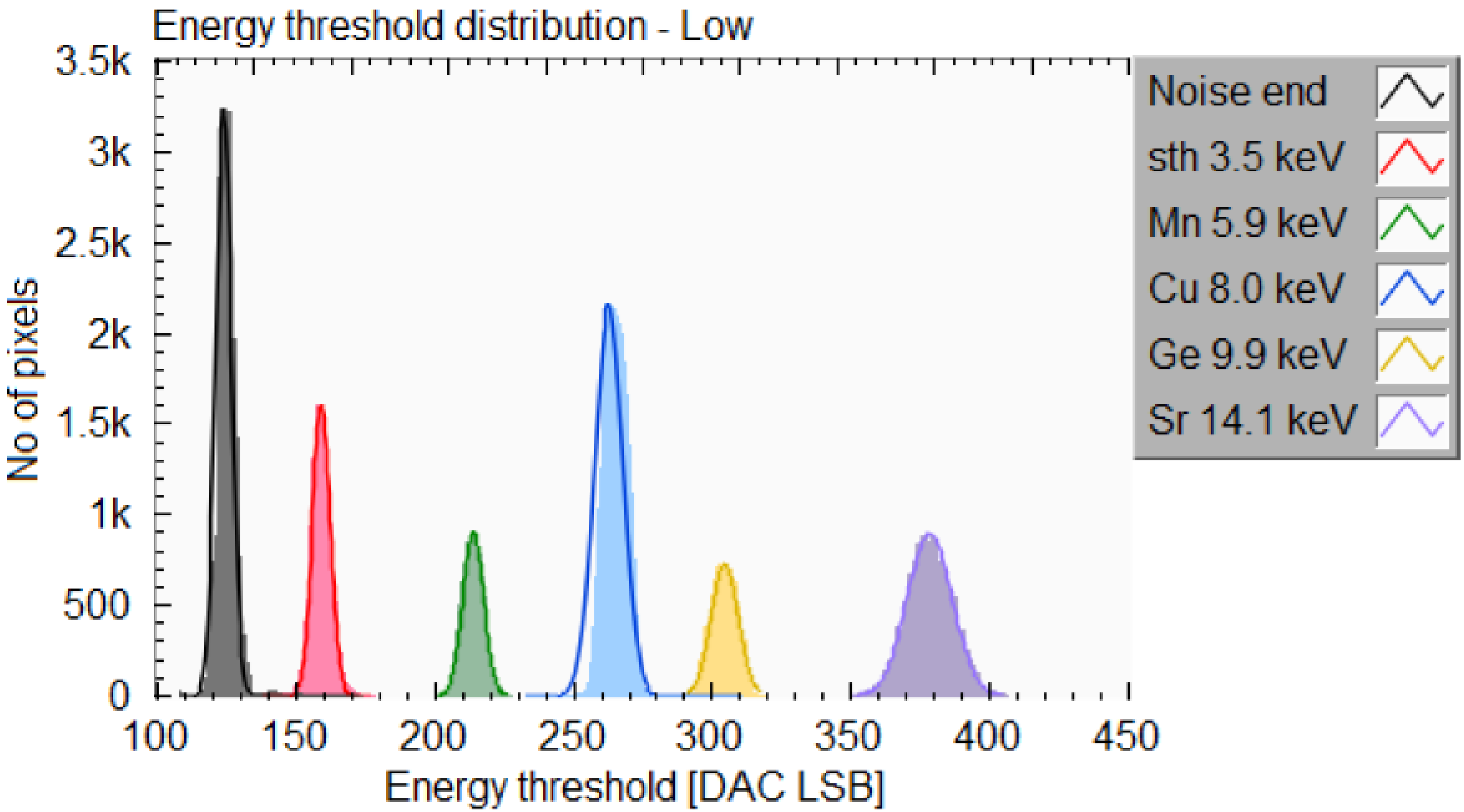
mean = 50.3 $\mu V/e^{-}$
sd/mean = 1.9%

Integral spectra





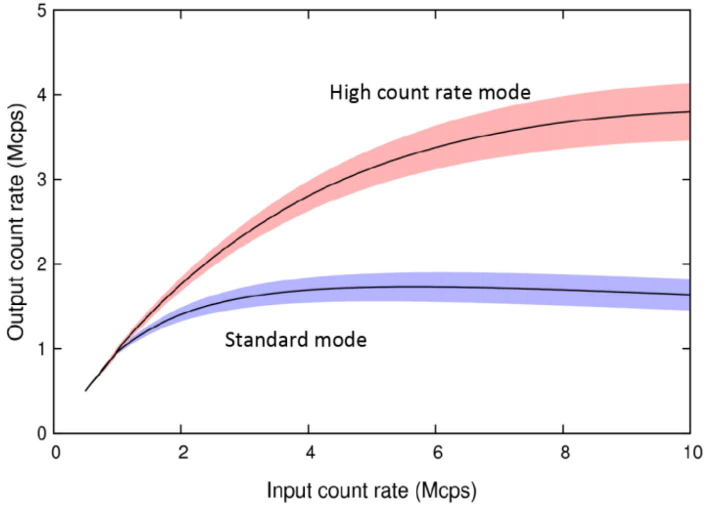
Tests in SOLEIL in March/April 2017

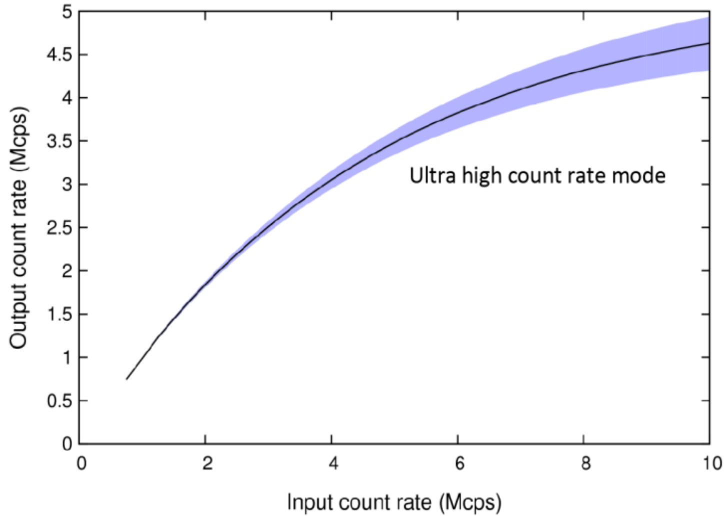


High Count Rate Capability

1. X-ray tube with Cu anode (8 keV) operated at 45 kV and the current: from 20 mA up 190 mA
2. The results of the threshold scans for nominal setting in bias current of CSA feedback: *Ikrum* = 10 nA (SD mode) and *Ikrum* = 36 nA (HCR mode)
3. The illuminated detector area with the input pulse rate above 10 Mcps per pixel ⇒ 1200 pixels
4. Model of paralyzable photon counter
5. Noise calculated using measured integral spectra of X-ray source

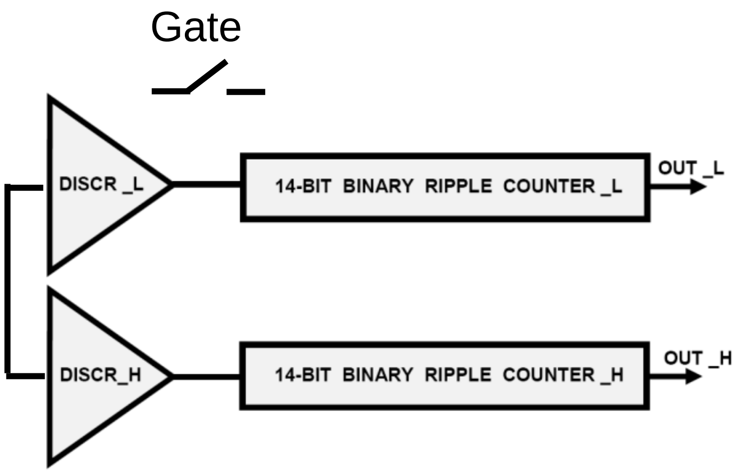
$$N_{OUT} = N_{IN} \exp(-N_{IN}\tau_P)$$



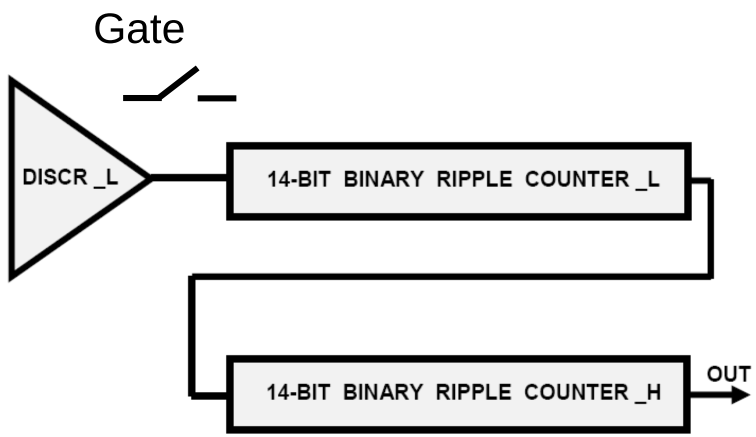


UFXC32k mode (operating condition)	Equivalent Noise Charge [e⁻ rms]	Mean dead time [ns]
Standard mode	123	232
High Count Rate mode	163	101
Ultra High Count Rate mode	235	**85**

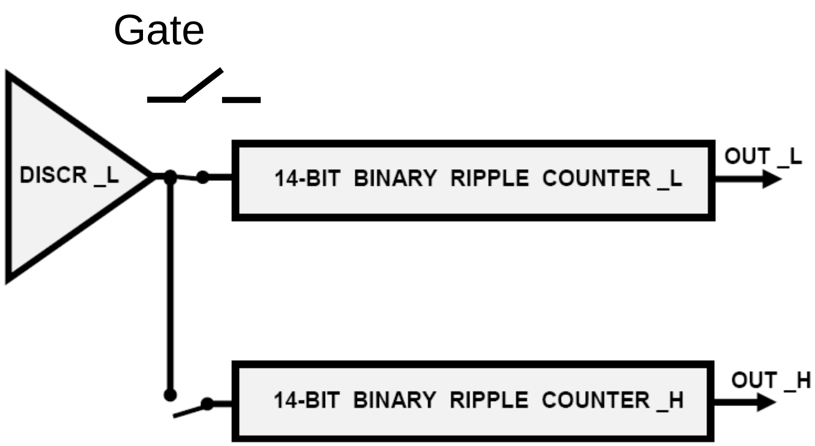
Default modes of operation



Standard Mode (Energy Window):
DISCR_L ⇒ COUNTER_L (N bits)
DISCR_H ⇒ COUNTER_H (N bits)



High Dynamic Range Mode
DISCR_L ⇒ COUNTER_L + COUNTER_H (28- bits)



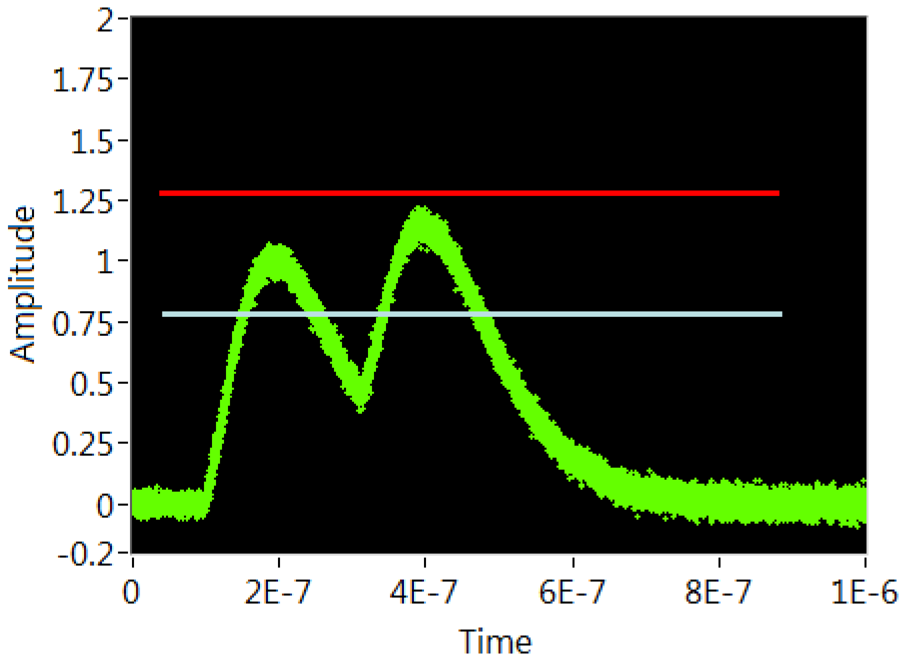
Zero Dead-Time Mode
Phase 1 : DISCR_L ⇒ COUNTER_L (N-bits)

Phase 2: DISCR_H ⇒ COUNTER_H (N-bits),
COUNTER_L(M-bits) ⇒ data readout

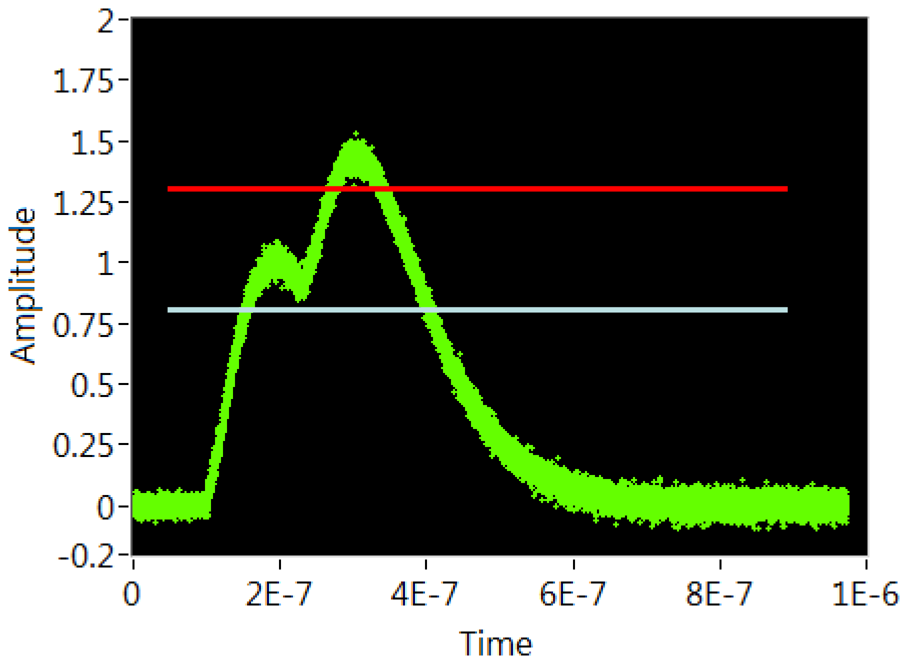
Number of readout bits N: 2 / 4 / 8 / 14

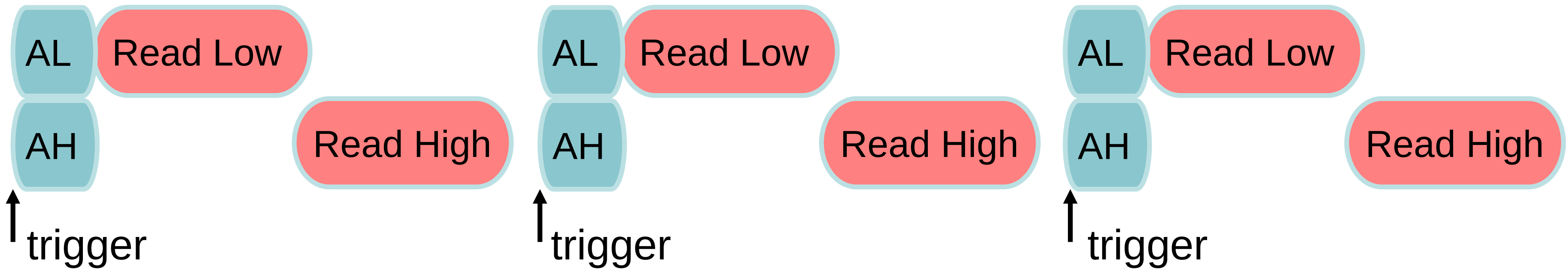
Double pulse

UFXC can distinguish two photons hitting the detector within 84 ns with single threshold



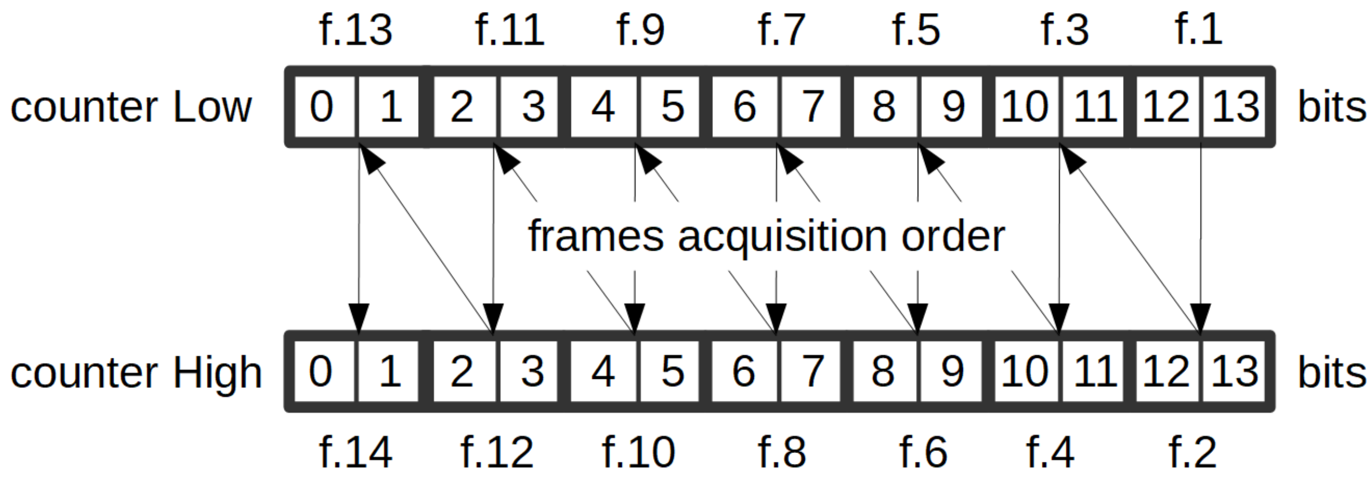
UFXC can distinguish two photons hitting the detector at the same time with two thresholds





To be verified in the experiment

Burst Mode



[1] S. Ross et al. JSR 23, 196 (2016)
[2] E.M. Dufresne et al., Opt. Express **24**, 355 (2016).

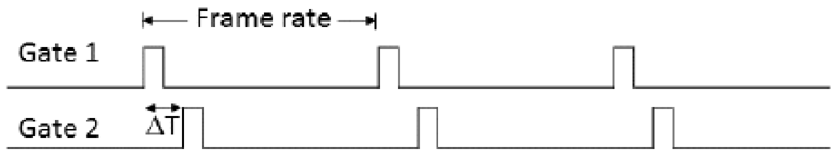
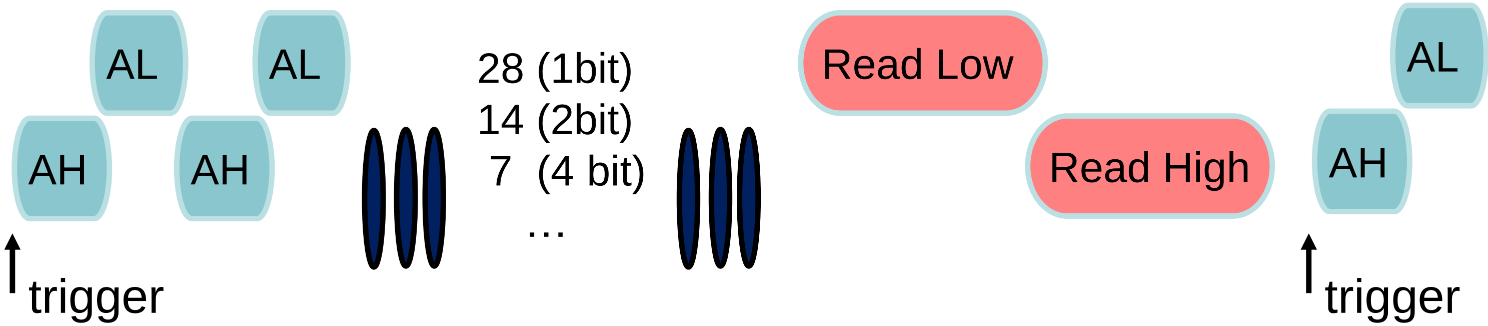


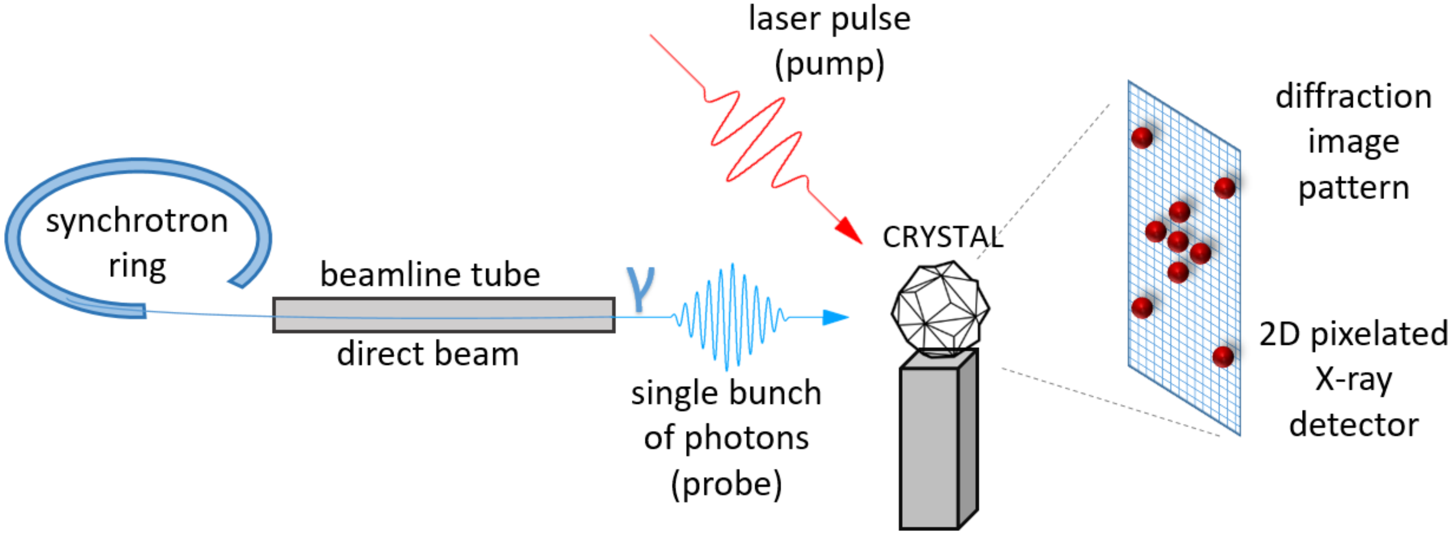
Fig. 1. The novel detector timing diagram applicable to two pulse XPCS. Varying the time delay ΔT between the gate 1 and 2 signals allows measurement of time correlation functions at small delay times. Note that the time difference between pulses in the two channels can be much smaller than the overall frame pair rate.

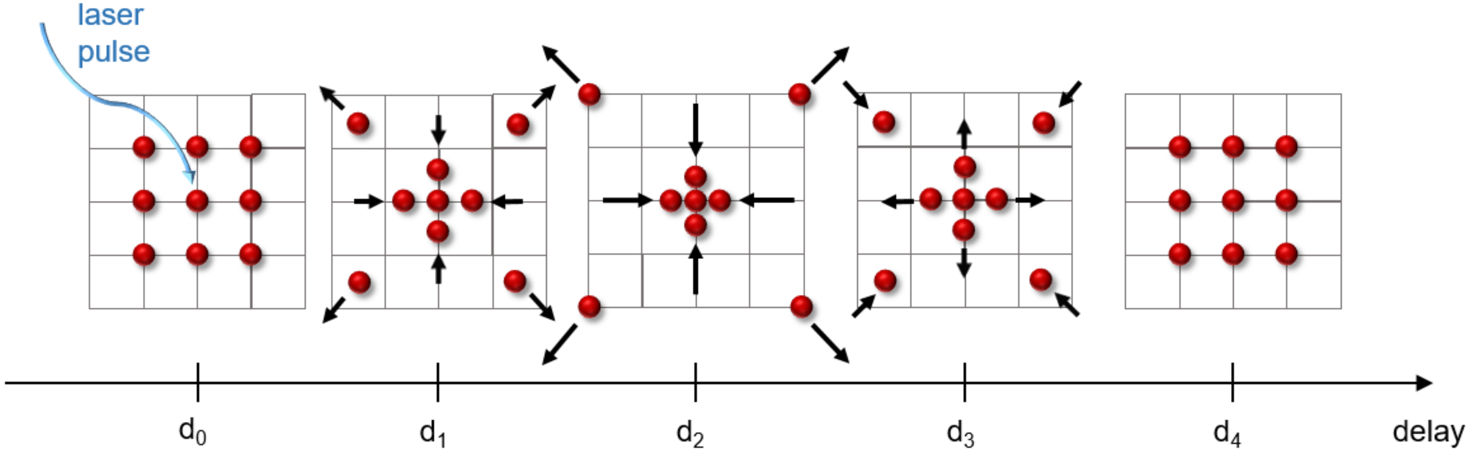
Burst mode of operation



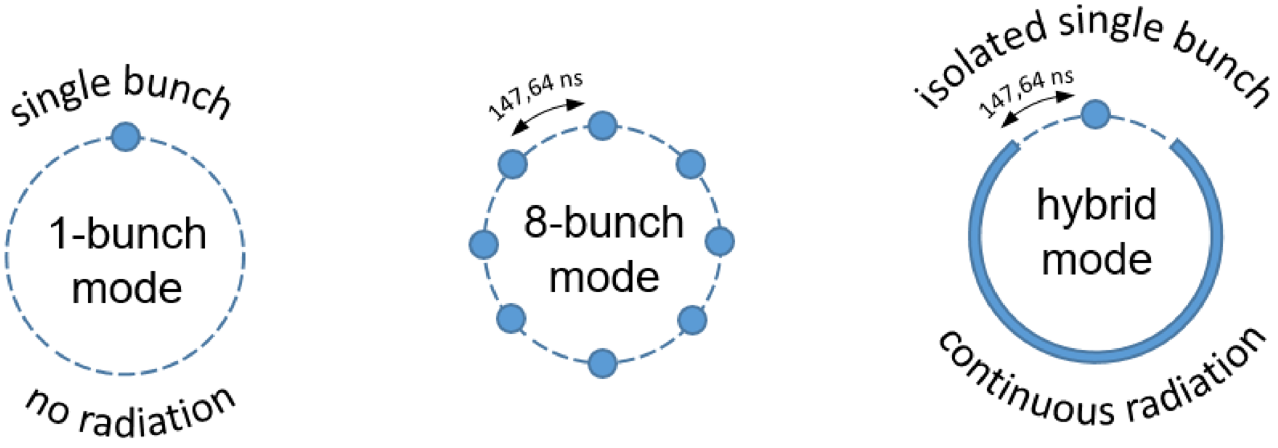
To be verified in the experiment

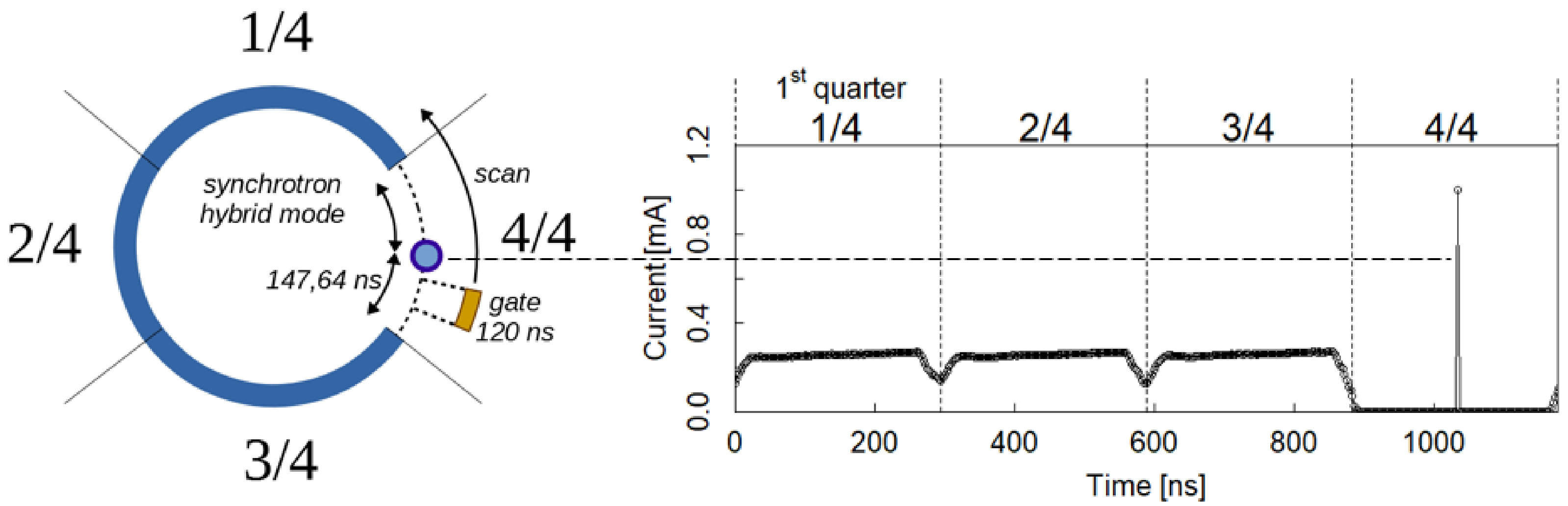
Tests for pump-probe experiment in SOLEIL





Tests for pump-probe experiment in SOLEIL





Tests for pump-probe experiment in SOLEIL

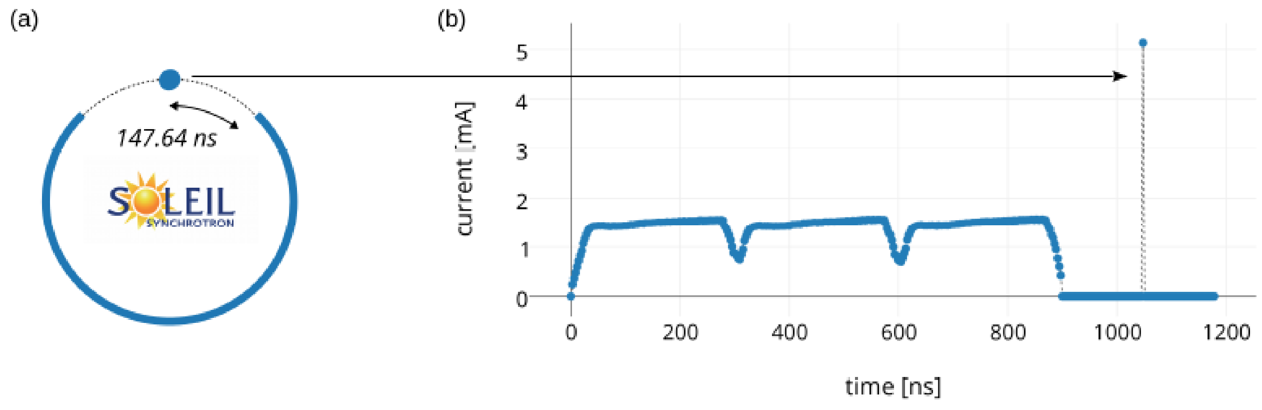


Figure 3. The hybrid filling mode at SOLEIL: (a) schematic view and (b) time-distribution of current per packet.

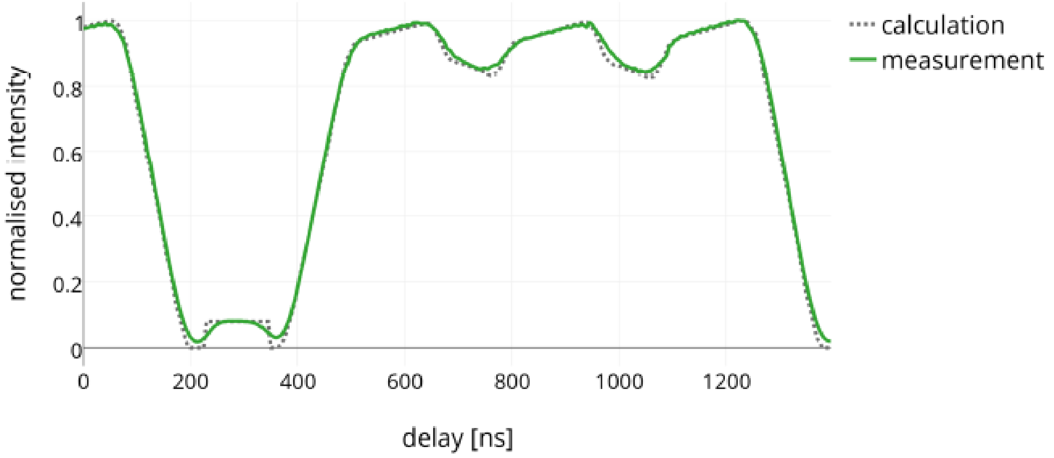
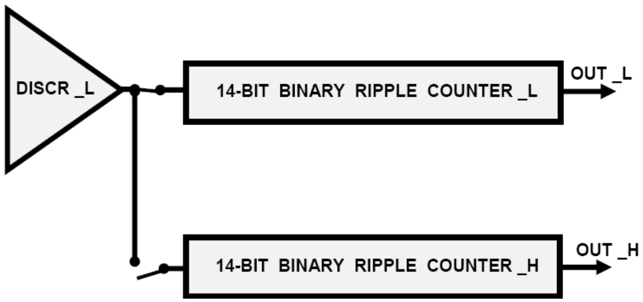
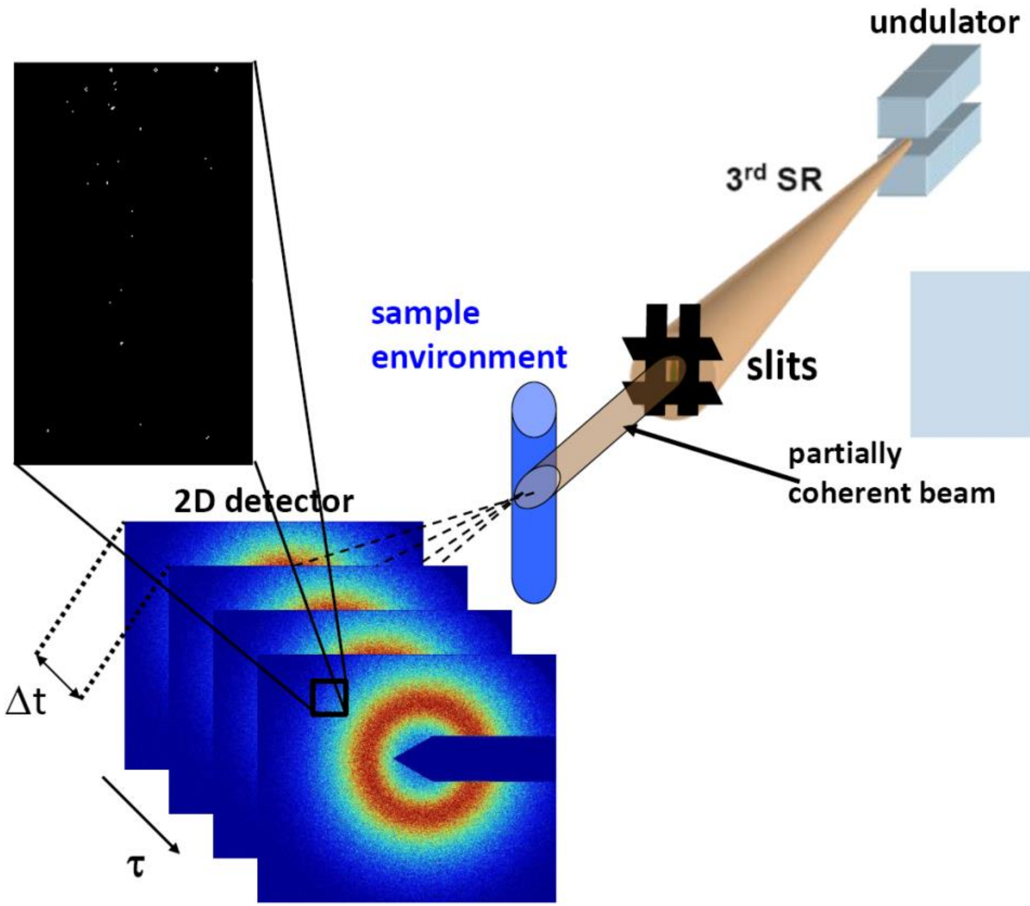


Figure 5. The hybrid filling mode of SOLEIL storage ring measured with the UFXC32k detector (green line) and calculated from the actual machine current values per packet (grey-dashed line). The measured scan was obtained by illuminating the detector with Ge fluorescence radiation (K_α = 9.9 keV), and registering a large number of frames of 120 ns with precisely controlled delay with respect to the storage ring clock.

X-ray Photon Correlation Spectroscopy at Advanced Photon Source in ANL

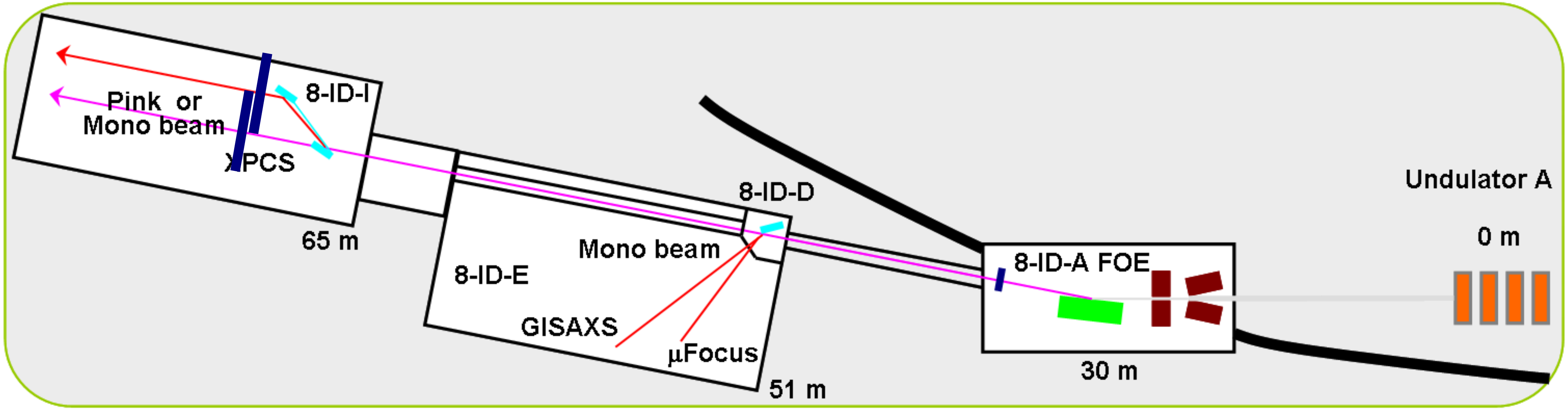
Unique technique to probe the motion of nanoscale structures over a wide range of length (100 nm – 1 nm) and time scales (10^{-6} – 10^{3} seconds) in materials



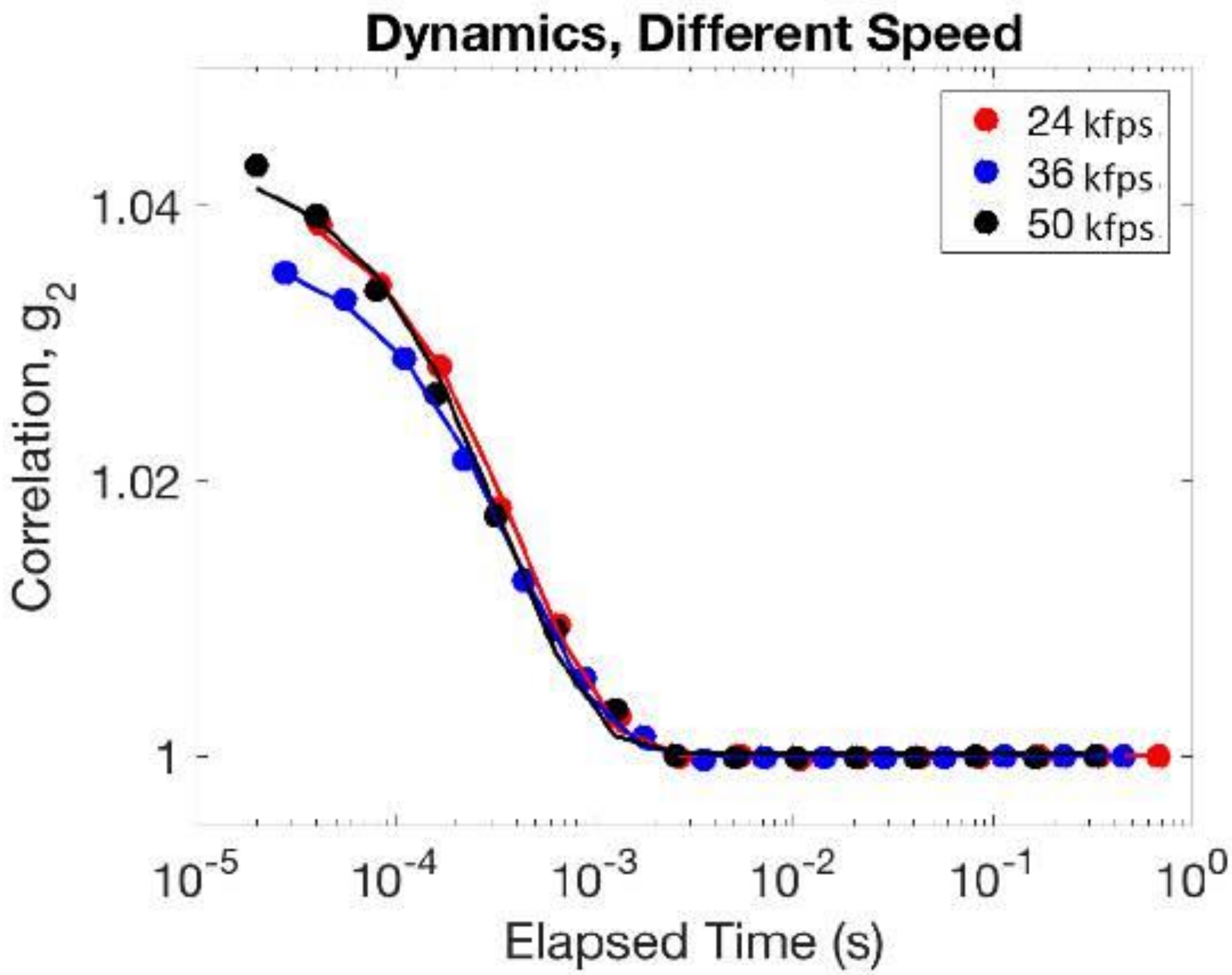


Overview of Small-Angle XPCS at 8-ID-I

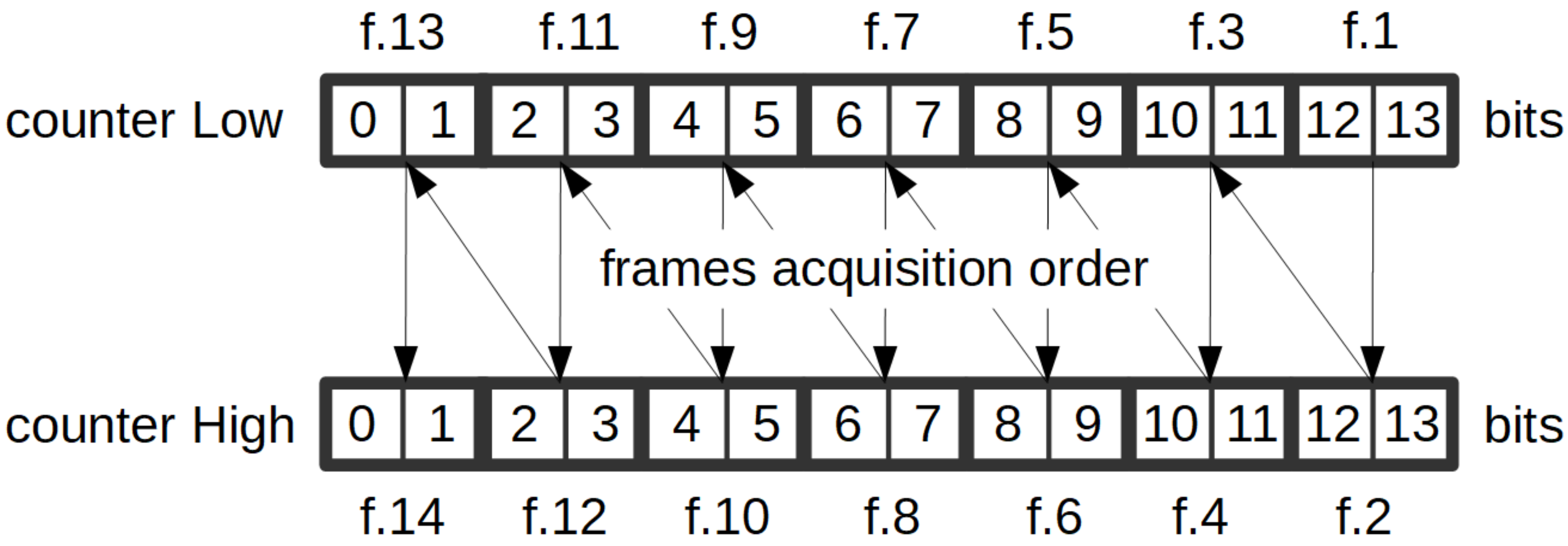
- Simple undulator beamline, all water cooled optics → improved stability
- 2 phased undulator A (at 7.35, and 11 keV) using the full straight section
- Minimal beam size – only central cone into optics enclosure
- Mirror first optics in 8-ID-A
- Beam splitting monochromator in 8-ID-D for 8ID-E, DCM in 8-ID-I



Tests for UFXC32k usability for XPCS experiments at APS at ANL

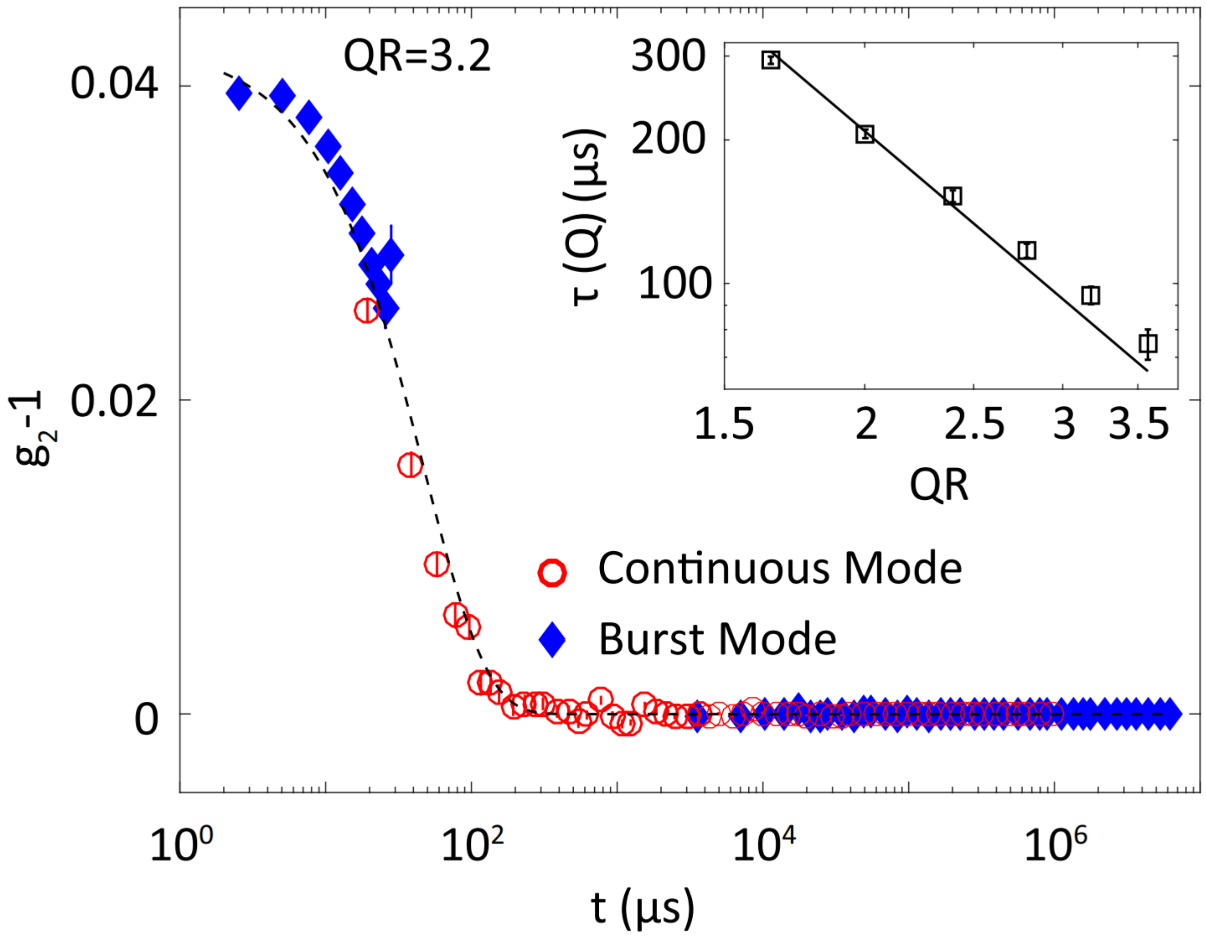


Burst Mode


f.13
f.11
f.9
f.7
f.5
f.3
f.1
counter Low
0 1 2 3 4 5 6 7 8 9 10 11 12 13
bits
frames acquisition order
counter High
0 1 2 3 4 5 6 7 8 9 10 11 12 13
bits
f.14
f.12
f.10
f.8
f.6
f.4
f.2

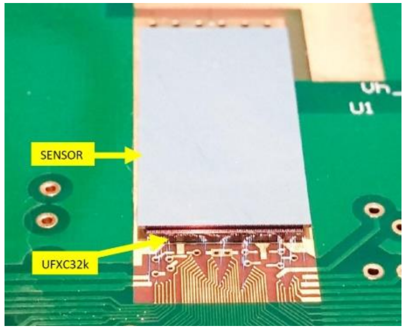
Hybrid mode

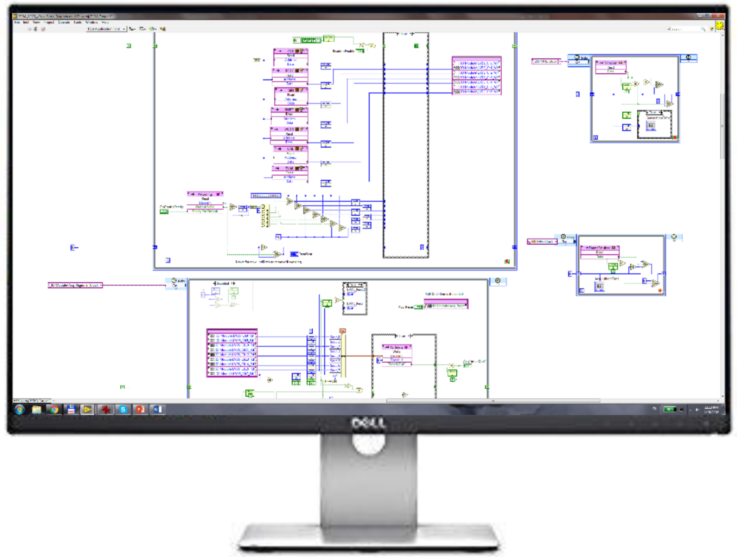
Zero-dead time mode + Burst mode

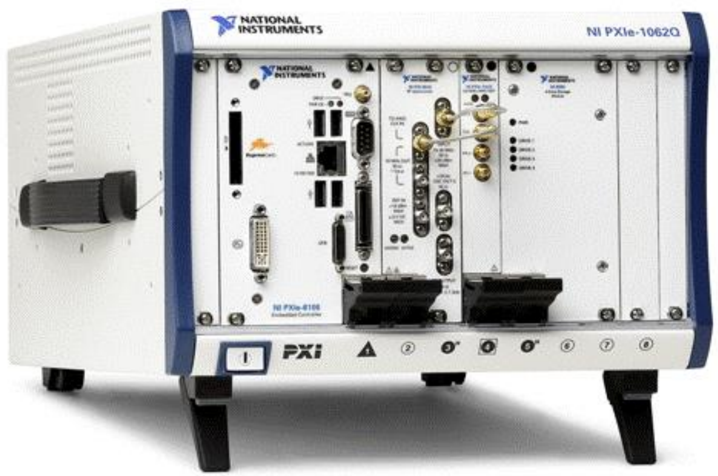


Measuring setup

LabVIEW

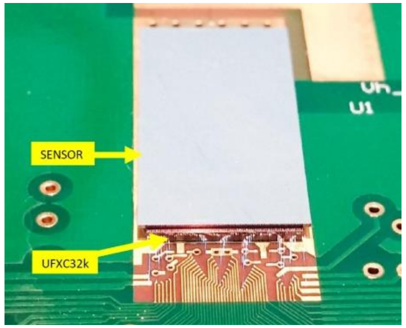






Data Throughput

EPICS



HS DIO 3.2 GB/s

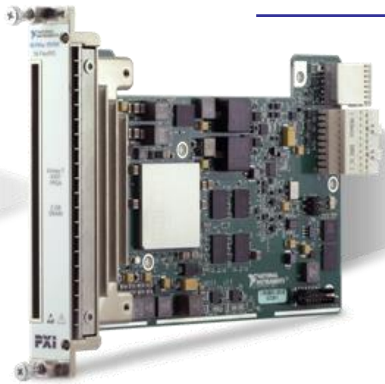
Data Transfer For Calculation

Large Data Set
Slow Data Handling

FPGA to DRAM 3.2 GB/s

NI 6589

FlexRIO Adapter Module

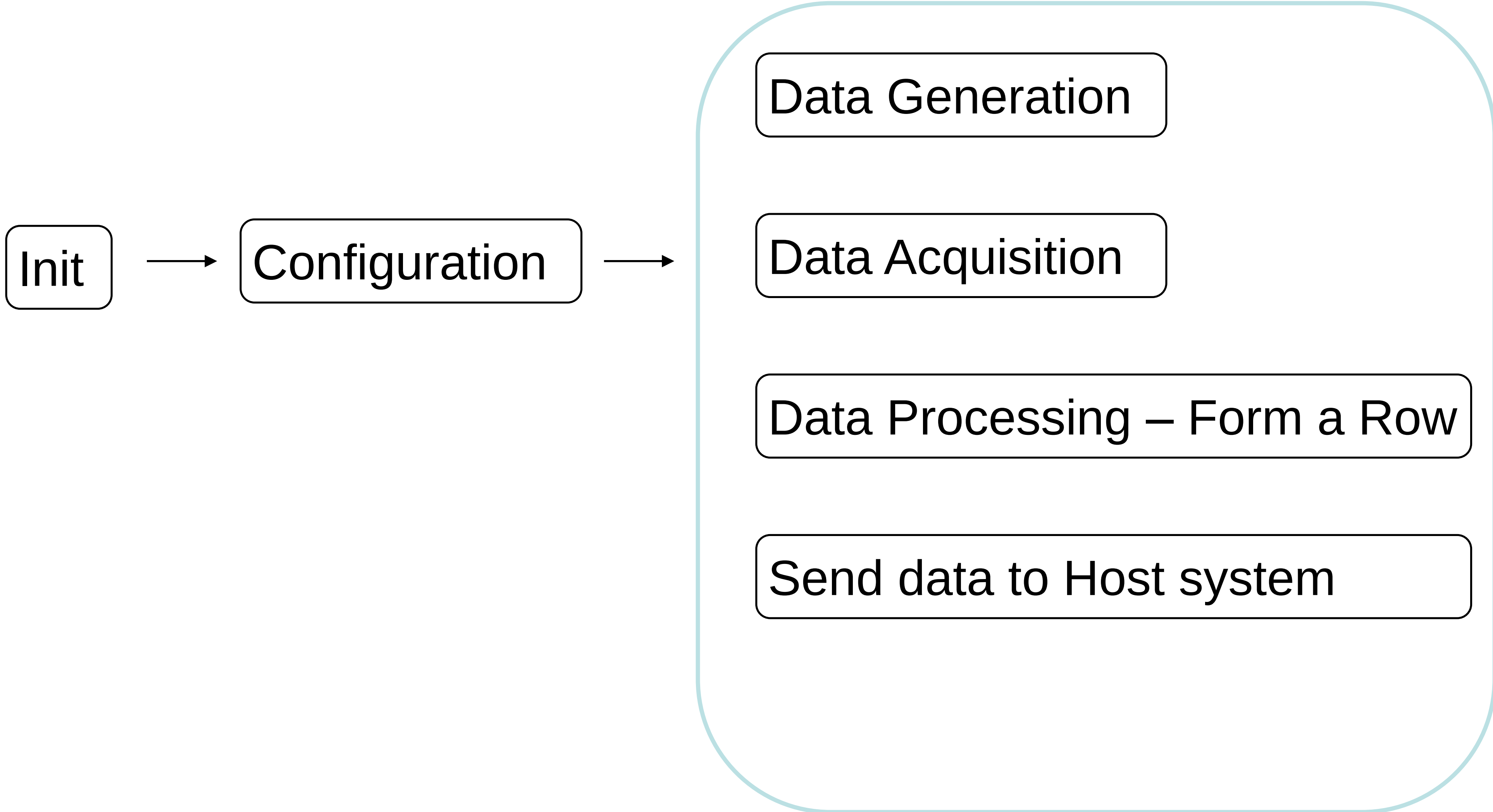


FlexRIO Module

PXI System

Streaming to RAM = 3.2 GB/s

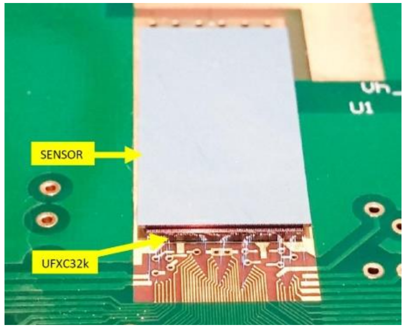
FPGA Program



AGH

Data Throughput

EPICS



HS DIO 3.2 GB/s

Too Large data set
slow transmission

Too Large data set
Too slow processing

FPGA to DRAM 3.2 GB/s

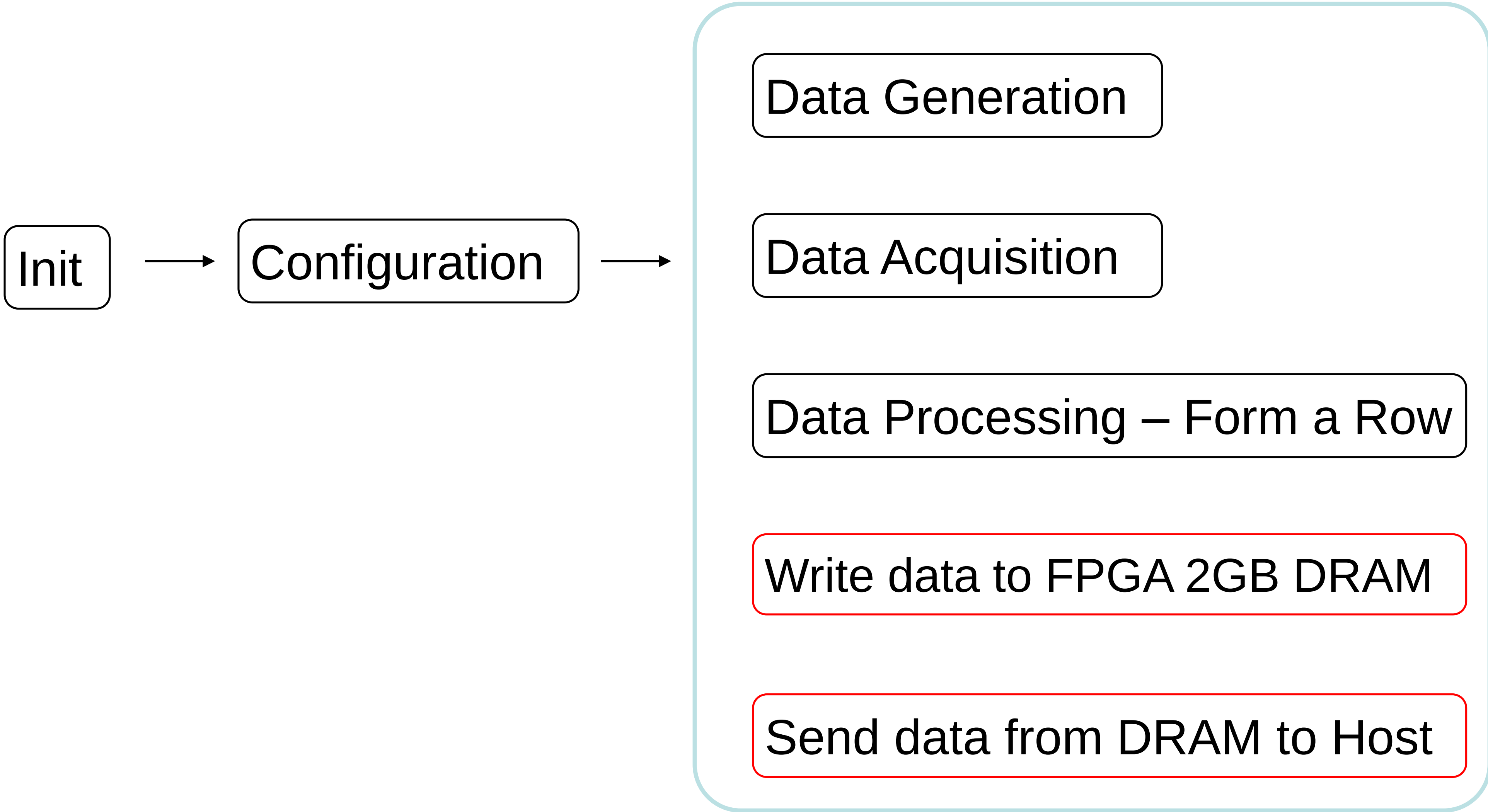
NI 6589

FlexRIO
Adapter
Module

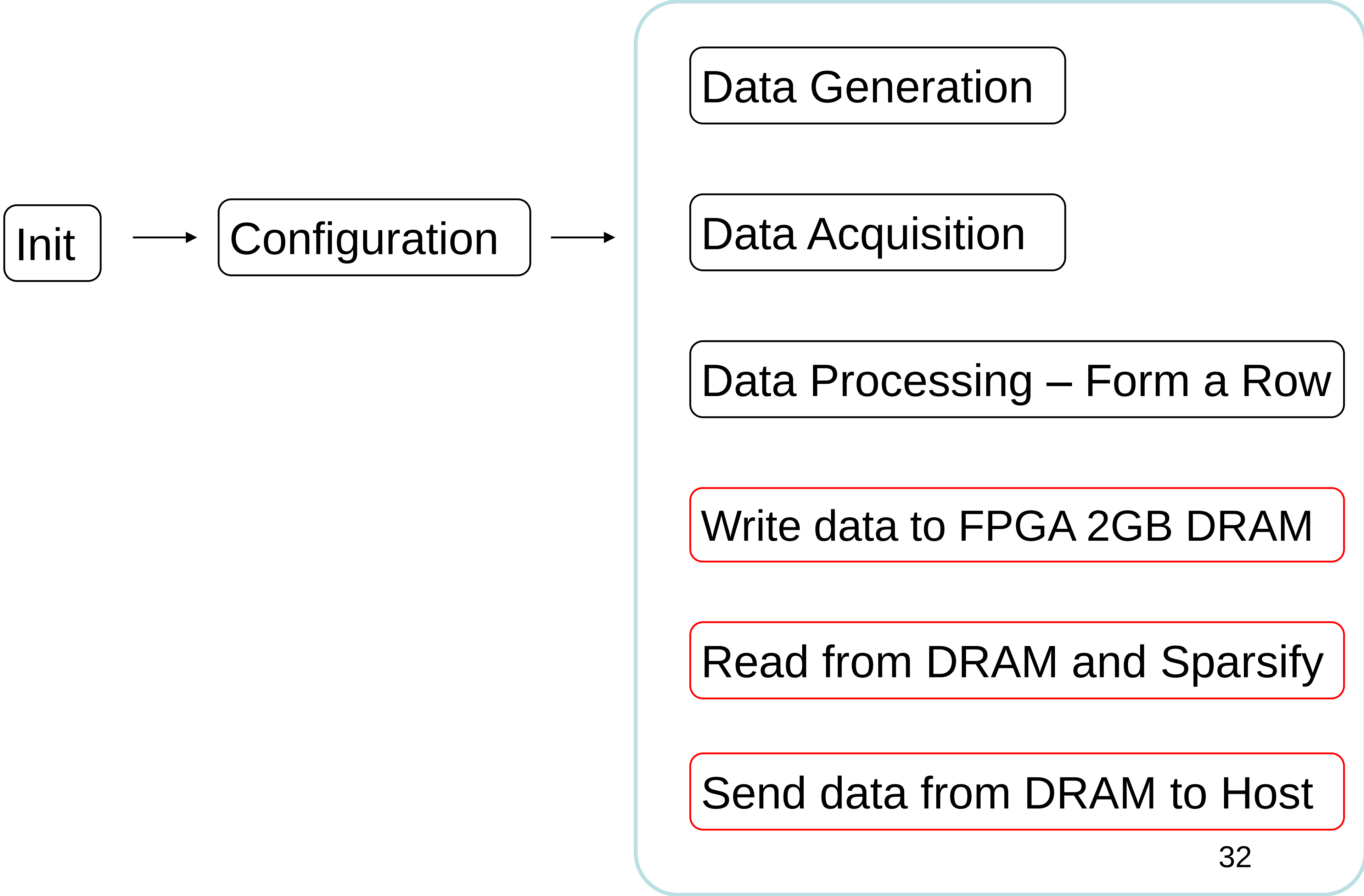
Streaming to RAM = ~~3.2 GB/s~~ 0.25 GB/s

Onboard RAM - 3.2 GB/s

FPGA Program

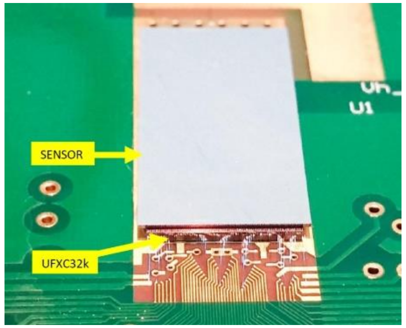


FPGA Program



AGH

Data Throughput



HS DIO 3.2 GB/s

NI 6589

FlexRIO Adapter Module

FPGA to DRAM 3.2 GB/s

Onboard RAM - 3.2 GB/s

Fast as file size > up to 100 MB

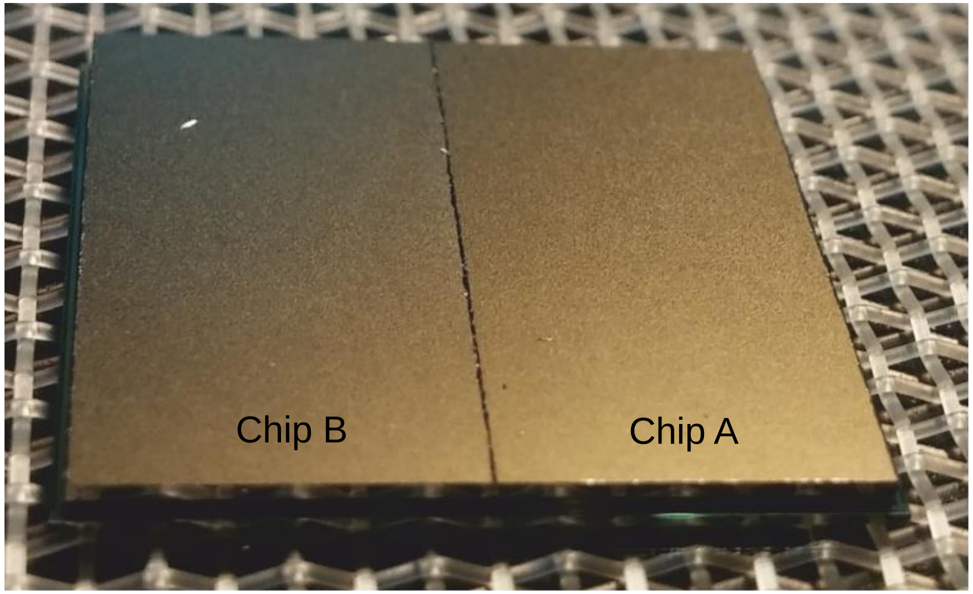
Fast as file size > up to 100 MB

EPICS

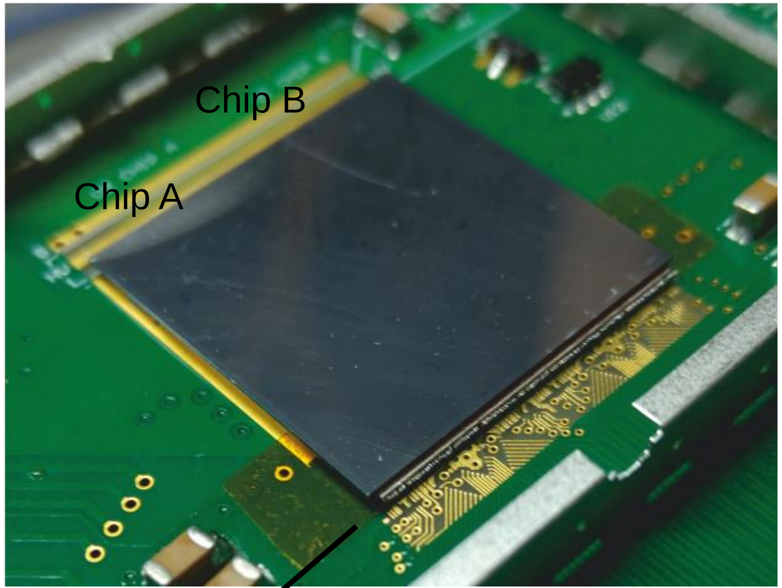
Sparsification – send the address of a hit pixel only

Next Experiment with final setup – April 19-23, 2018

UFXC32K 2-chip module Camera



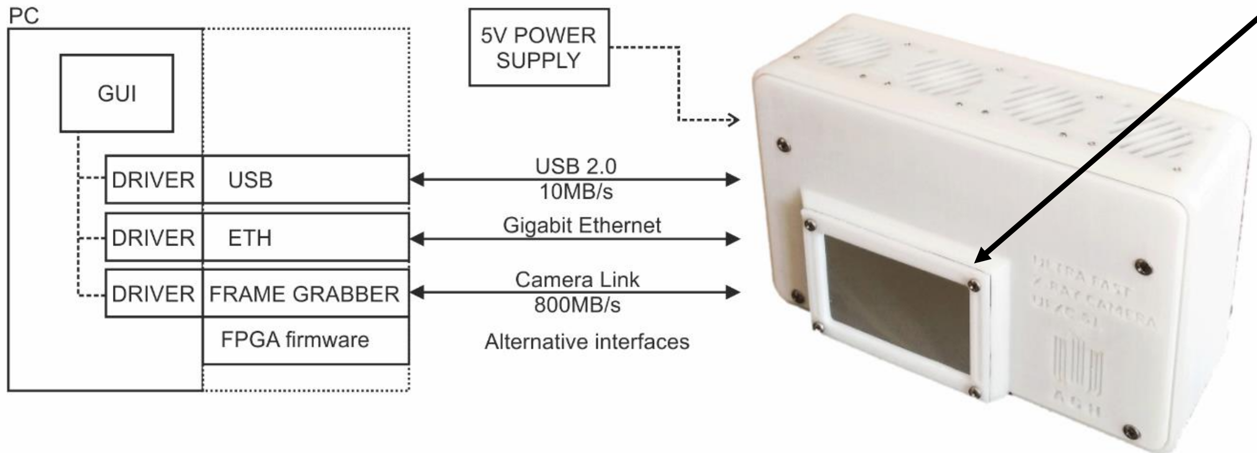
2-chip module for wire-bonding (ASIC side)

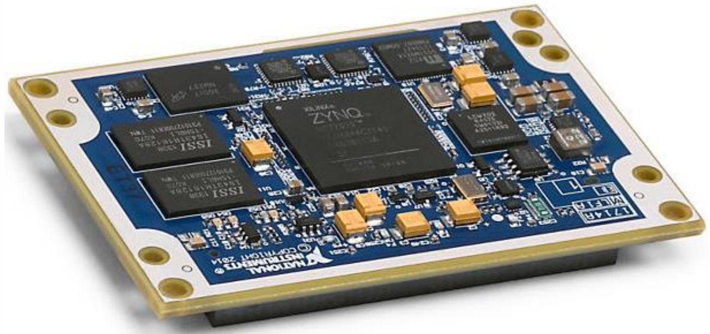


2-chip module (sensor side)

Successful tests at:
- synchrotron sources
- diffractometers

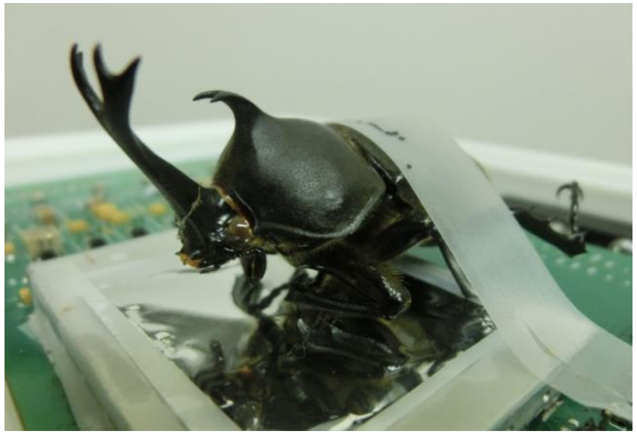
Prototype all-in-one camera

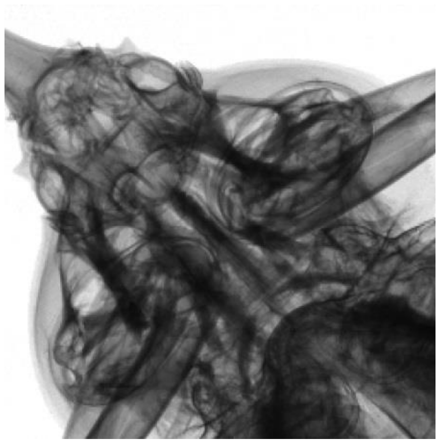


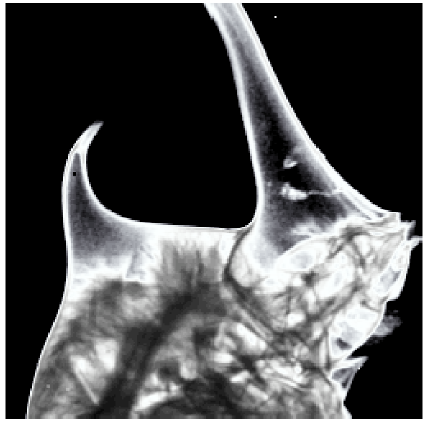


AGH

Images with UFXC using 2-chip module

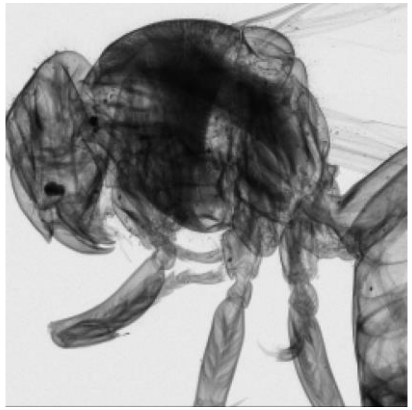




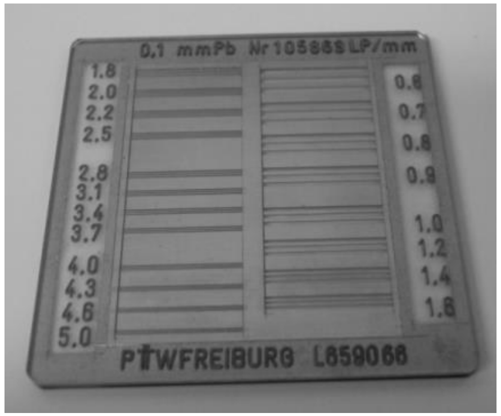


rhinoceros beetle

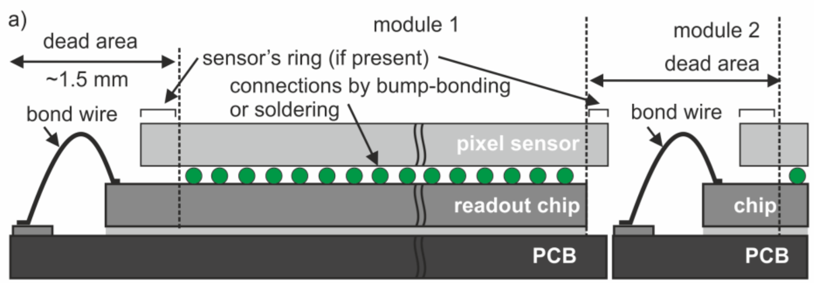
giant hornet

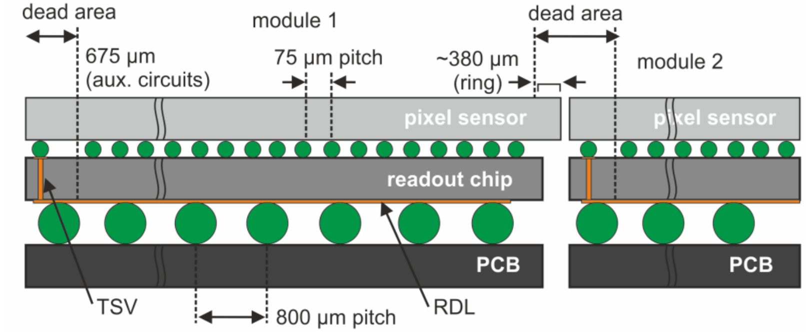


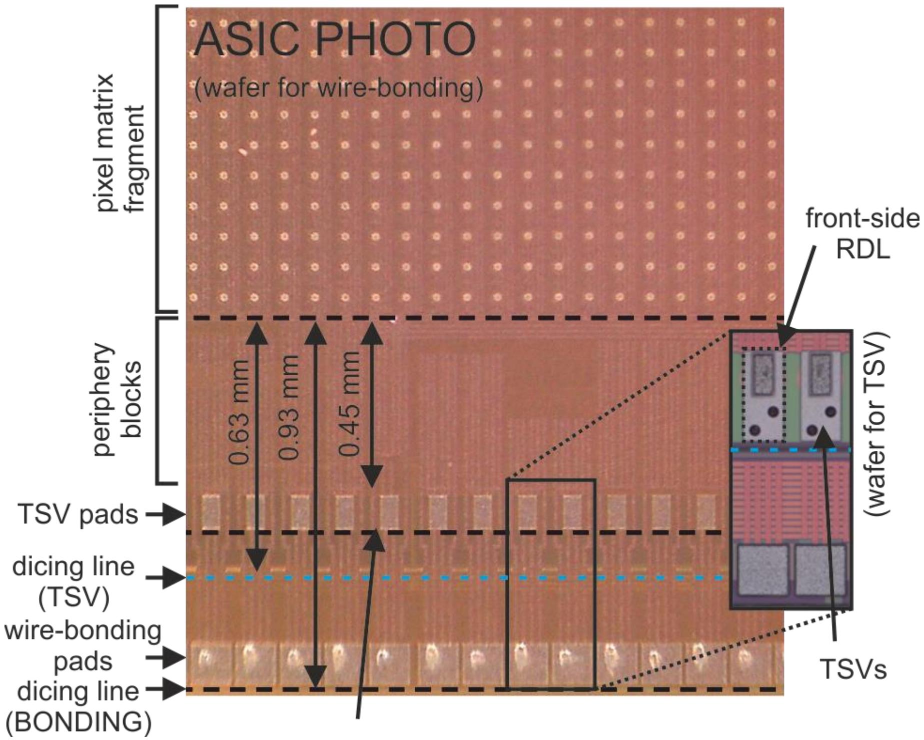
l/mm



2-chip module with TSV

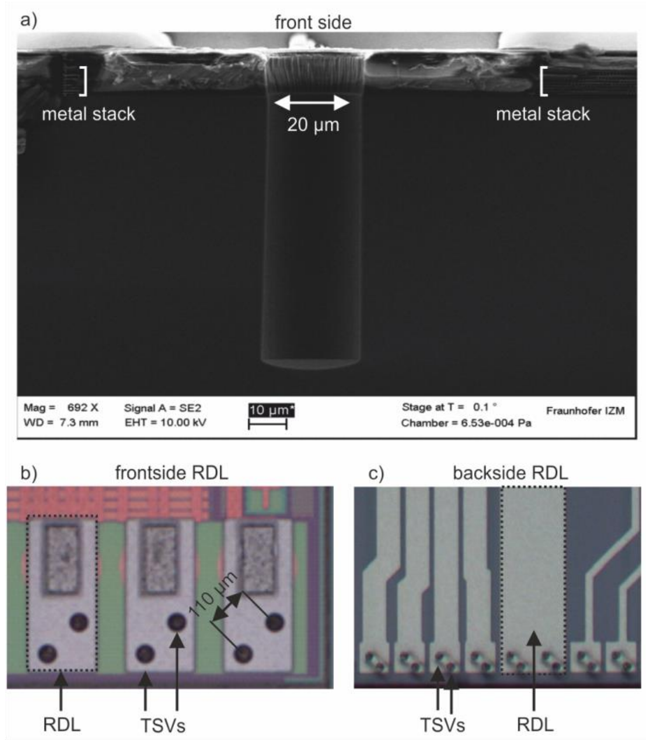




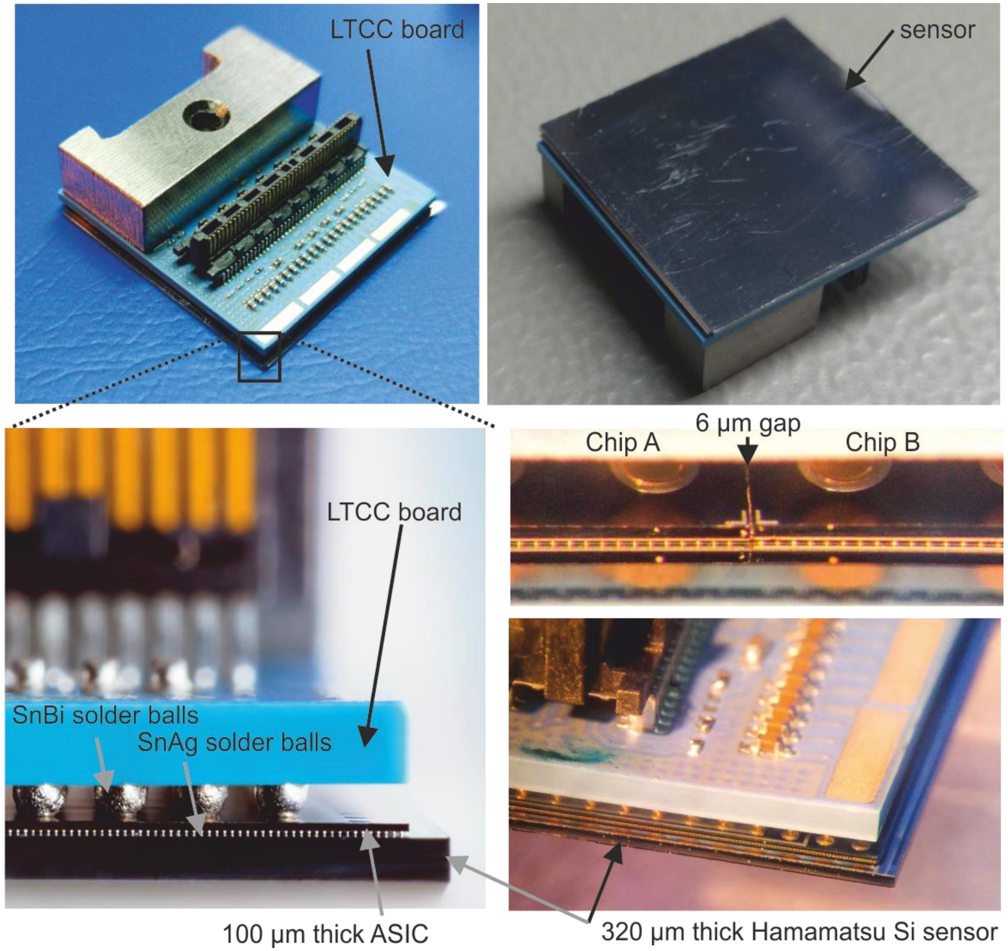


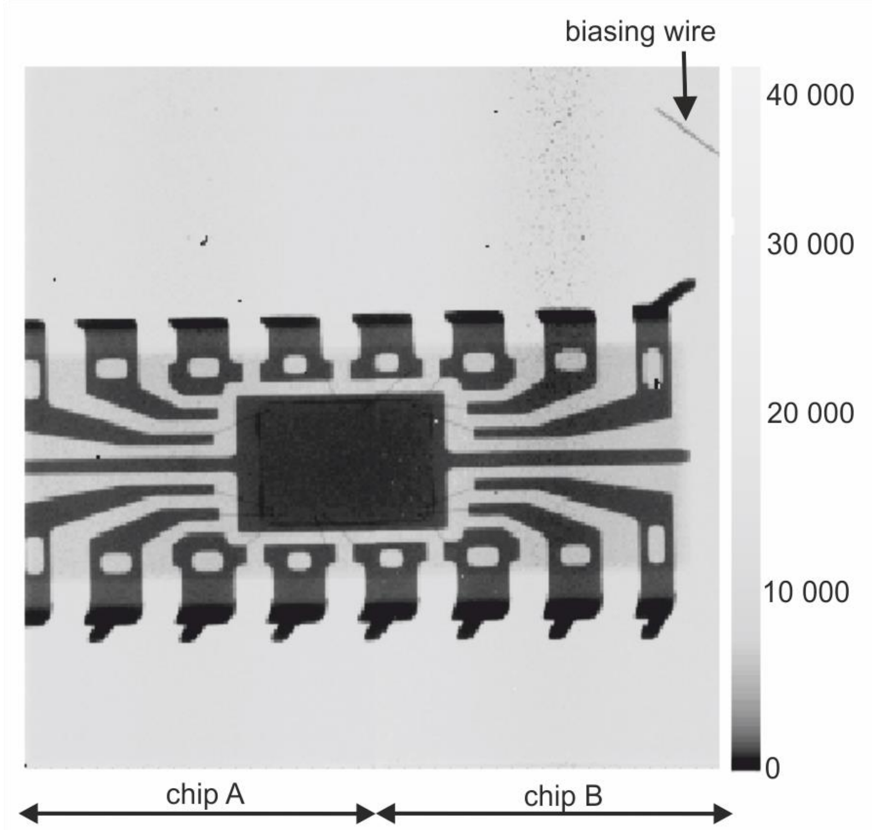
K. Kasinski et. al. NSS, Strasburg 2016
Submitted to IEEE TNS 2017

TSV & backside RDL



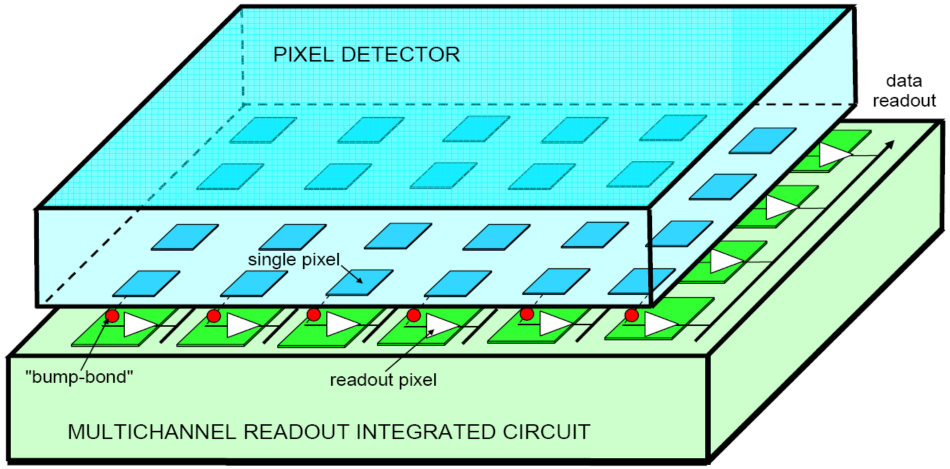
2-chip module with TSV

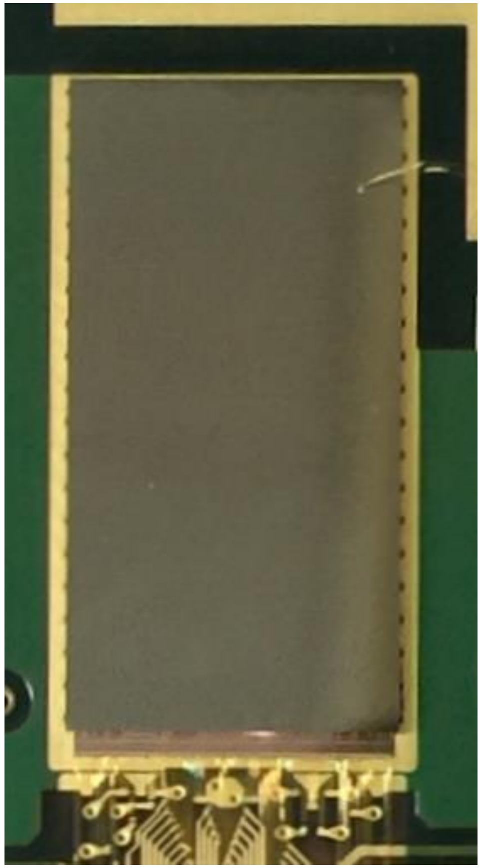




An example of DIL radiogram acquired with the fully assembled 2-chip module.

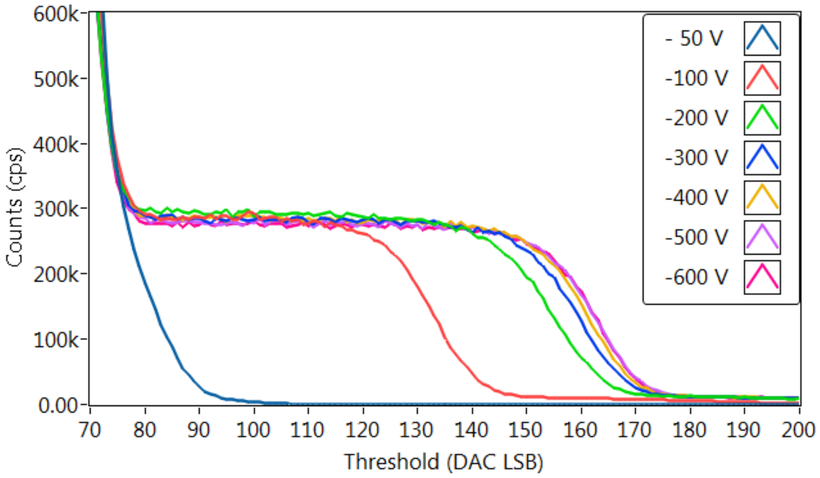
UFCX32k with CdTe from Acrorad





Parameter	Si	Ge	GaAs	CdTe	CdZnTe
Average Z	14	32	31/33	48/52	48/30/52
Energy bandgap [eV]	1.12	0.67	1.43	1.44	~1.6
Density [g/cm^3]	2.3	5.3	5.4	6.1	5.8
Energy for e-h pair generation [eV]	3.64	2.96	4.2	4.43	~4.6
Mobility [cm^2/Vs] - electrons - holes	1350 480	1900 3900	8000 400	1100 100	~1000 ~100
Carrier lifetime [µs]	~250	250	0.001 –0.01	~0.1–2	~0.1–2

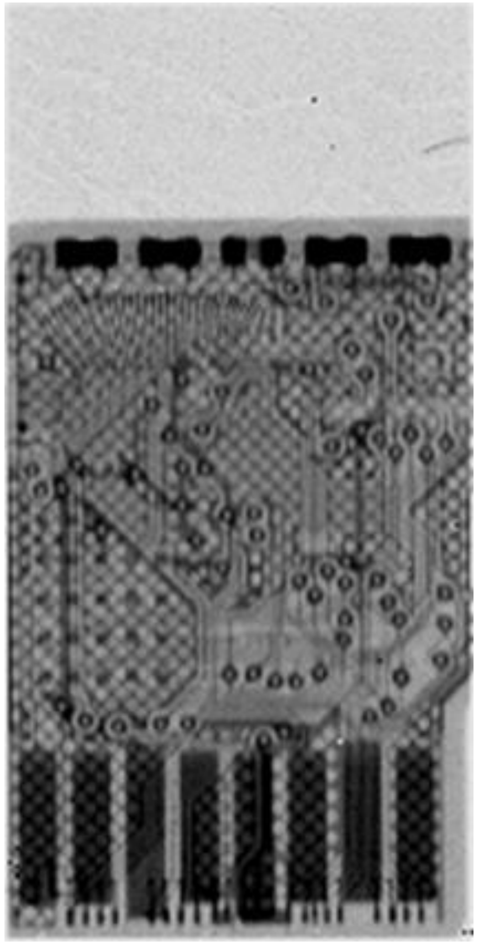
UFCX32k with CdTe – 750 µm thick (detector bias @ 400V)



UFCX32k with CdTe

Examples of raw X-ray radiograms of micro SD card taken with X-rays of energy 17.4 keV and the UFXC32k chip bump-bonded to

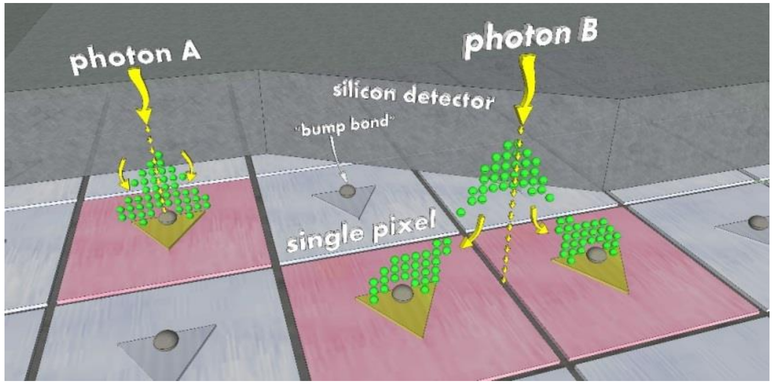
a) CdTe detector (750 μm thick)
3x higher efficiency



b) Si detector (320 μm thick)

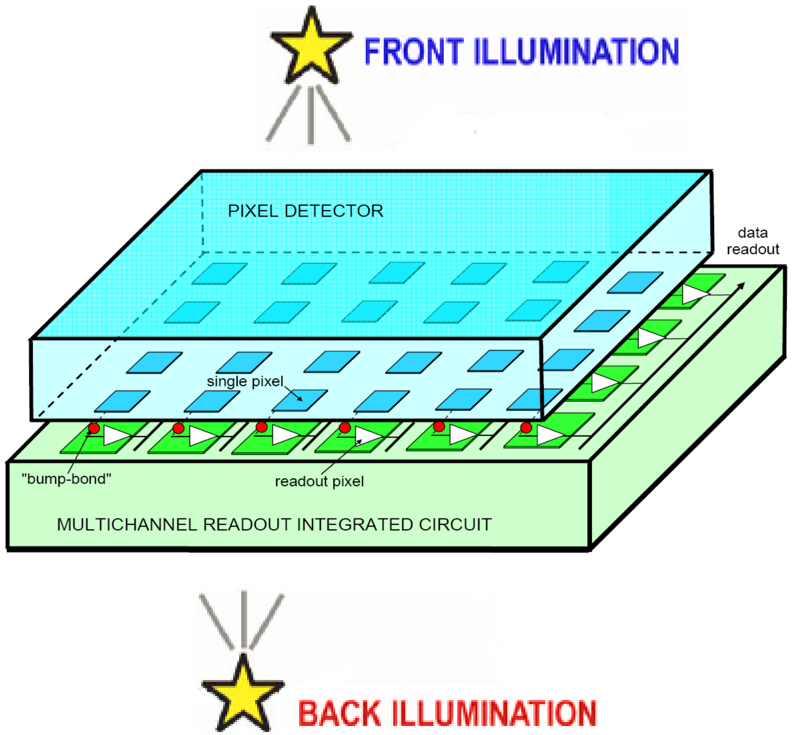
CdTe detector, pitch 75 μm, thickness 750 μm

charge sharing clearly visible (photon energy 17.4 keV)

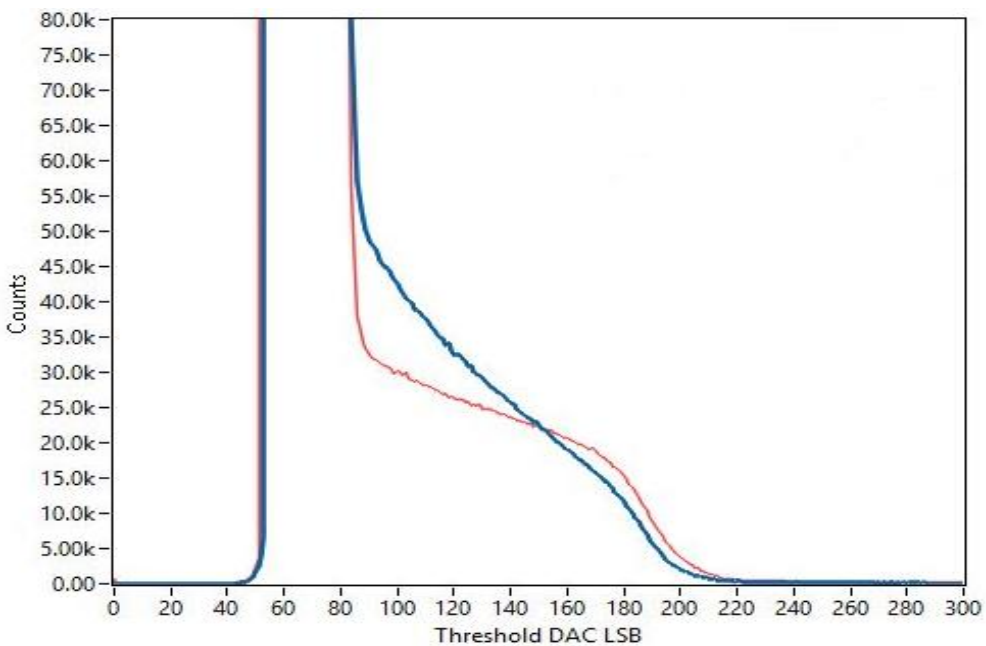


Charge sharing:

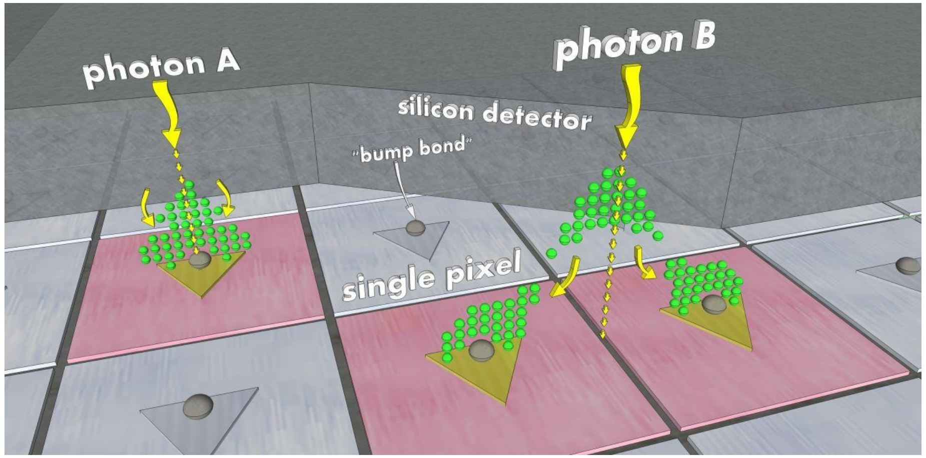
- some chips implement algorithms to solve the problem (i.e. Medipix3RX, PIXI-III, miniVIPIC, Chase Jr, etc),
- several groups use charge sharing to improve position sensitive resolution (ofen used method – center of gravity)

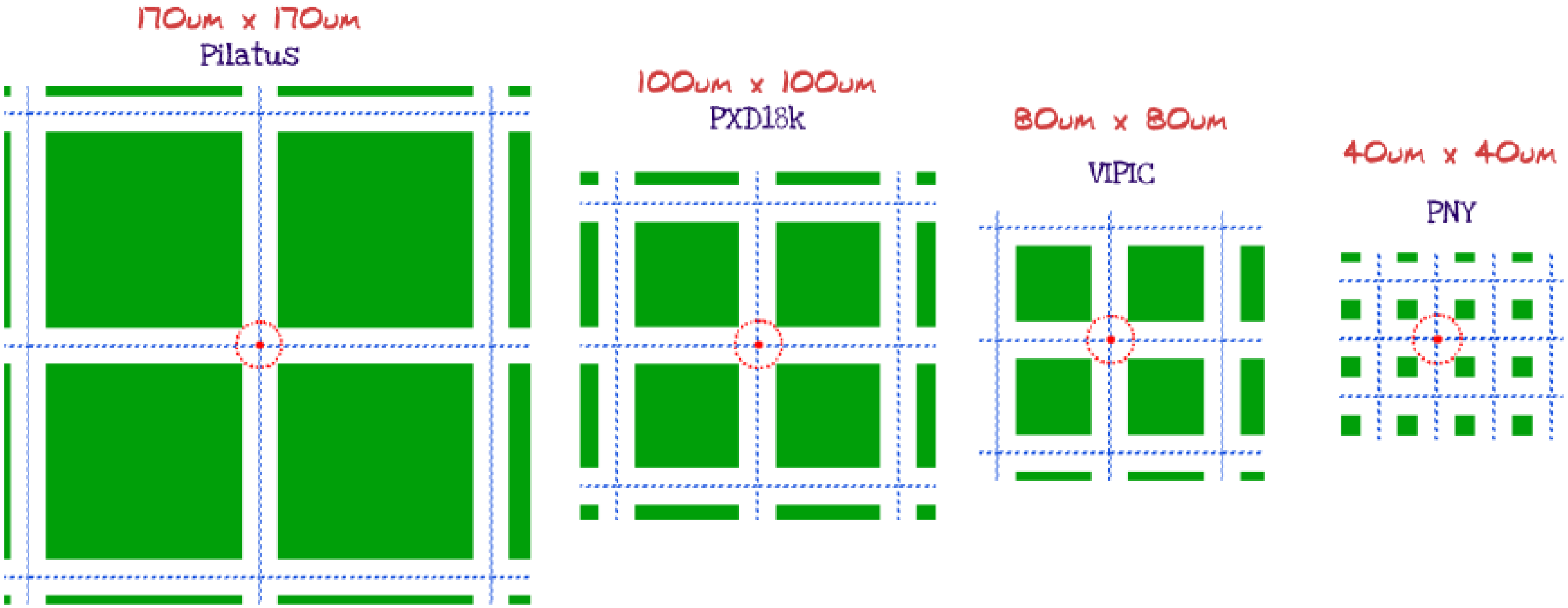


Normalized integral spectra



Charge sharing effect

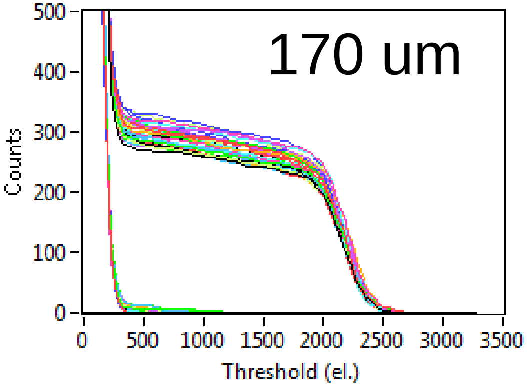


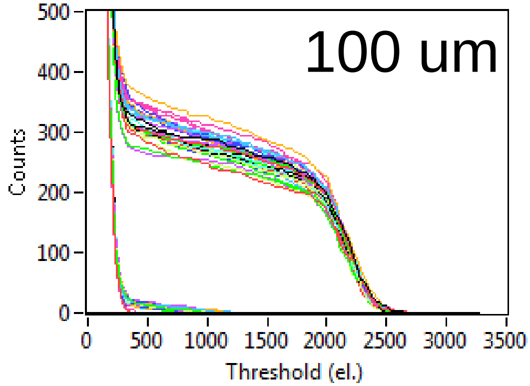


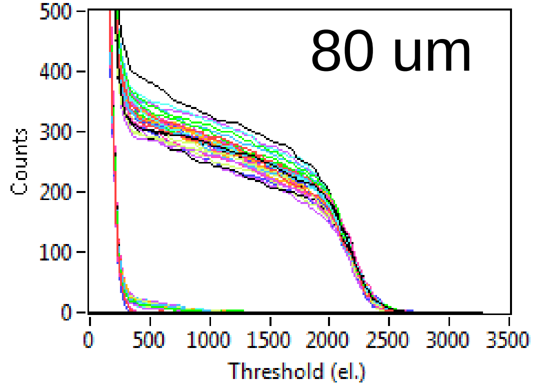
The first solution of this problem was proposed by CERN and consequently it was implemented in the Medipix III chip. However, due to pixel-to-pixel threshold dispersions and some imperfections of the simplified algorithm, the hit allocation was not functioning properly.

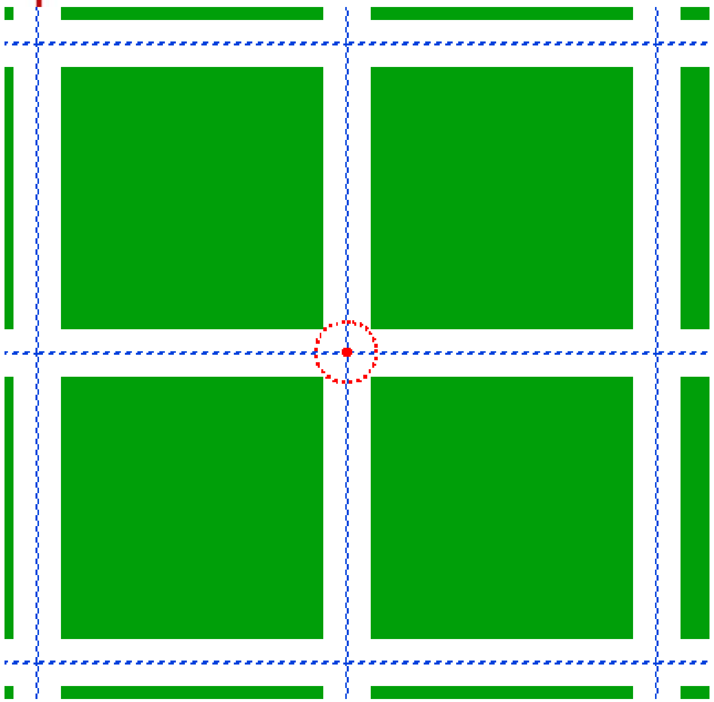
Charge sharing (energy distortion, hit position uncertainity)

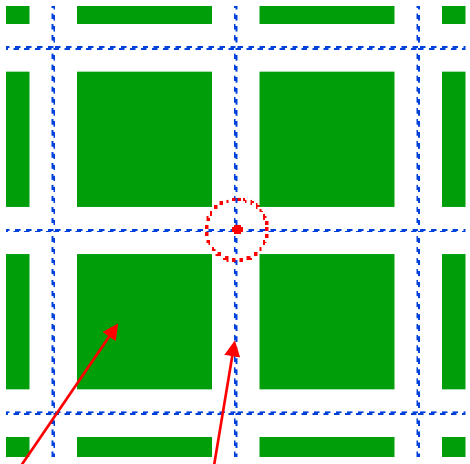
Example of simulated integral spectra:
8 keV photons is Si detector 300um thik, diffrent pixel size

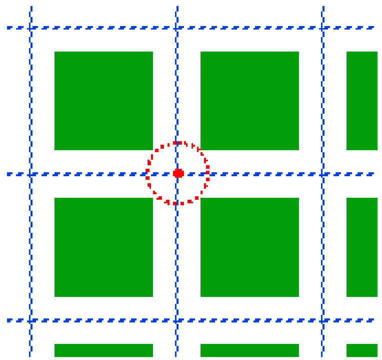












Area without charge sharing

Area affected by charge sharing

The pixel ICs with compensation of charge sharing:

- Medipix3RX,
- PIXIE,
- miniVIPIC,
- Chase Jr.

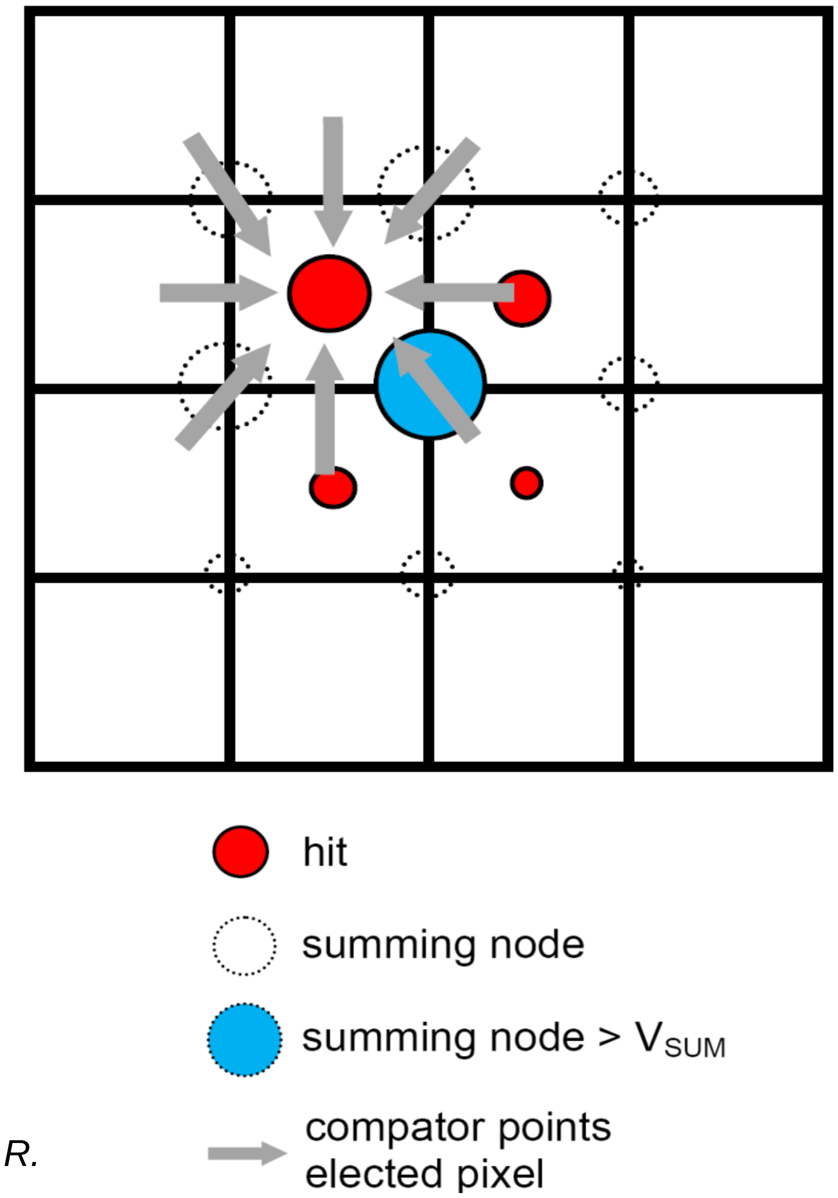
Maj P., et al.
IEEE UKSim, 2013

Solving the charge sharing problem - C8P1 algorithm

1) pulse at summing node is above a threshold

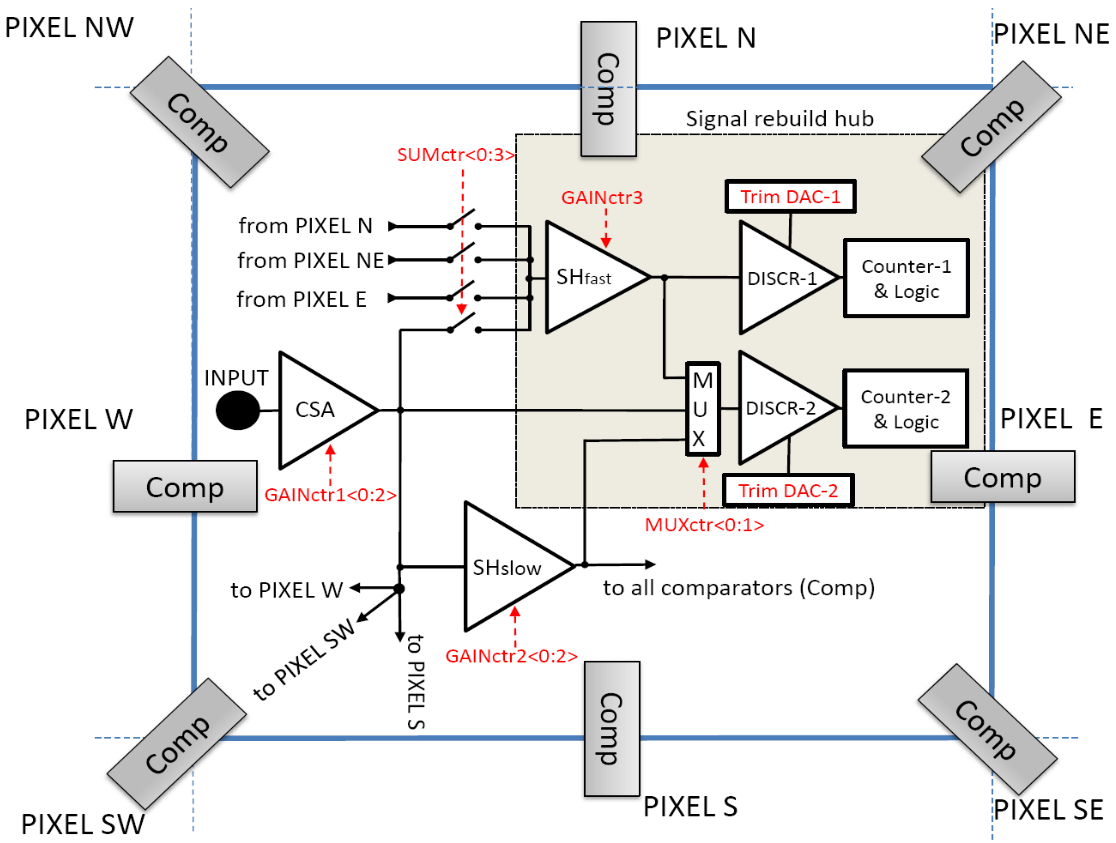
2) comparision of pulse amplitude in a single pixel with its 8 neighbours

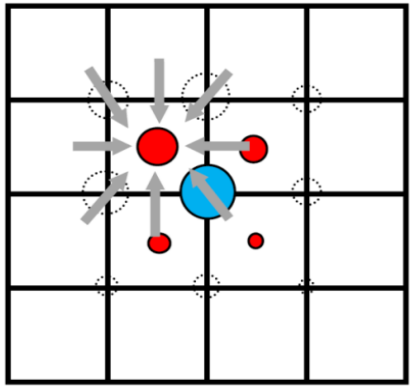
Selected pixel: one of its summing node is above the threshold AND all 8 comparators point out this pixel



*A. *Baumbaugh, G. Carini, G. Deptuch, P. Grybos, J. Hoff, P. Maj, P. Siddons, R. Szczygiel,M Trimpl, R. Yarema,* **Analysis of Full Charge Reconstruction Algorithms for X-Ray Pixelated Detectors, Proceedings of IEEE NSS 2011, Valencia, Spain,** Page(s): 660 – 667, Publication Year: 2011 ,

Single pixel architecture and inter-pixel communication -SPC chip in 40 nm technology





MATCHING:

1) Shfast: 7-bit offset trim

2) Shslow: 3-bit gain tim

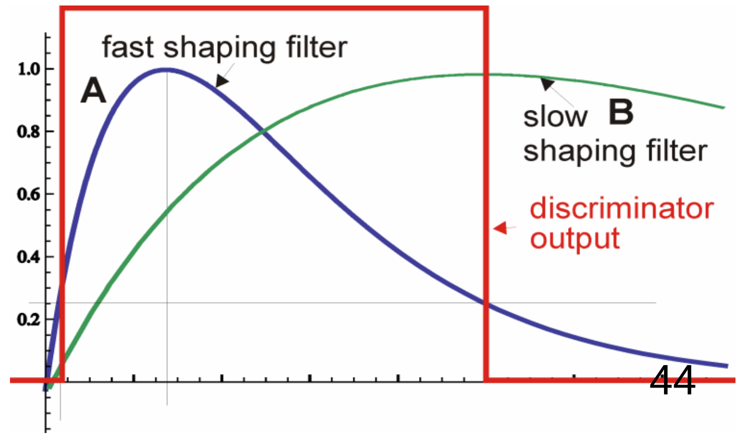
3) COMP: auto-zero correction trigged by DISCR output

4) Latching of COMP triggered by DISCR rising edge is controlled by timing curcuitry ; 5 bit trim

5) Additionally: **CSA** – 3-bit gain control

FAST signal processing path:

CSA + SHAPERfast (t_{peak}=48ns) - SUMMING ⇒ **TOTAL CHARGE**



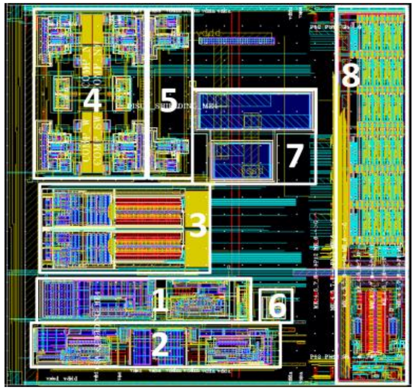
SLOW signal processing path:

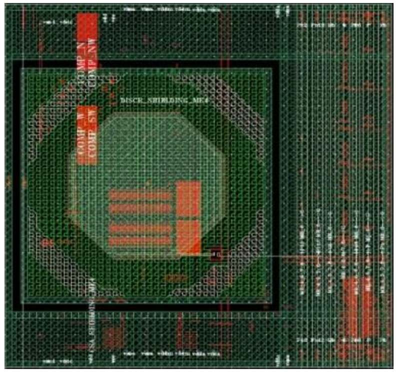
CSA + SHAPERslow (t_{peak}=80ns) – COMPARISION ⇒ **HIT ALLOCATION**

P. Maj, et al..IEEE Trans. Nucl. Sci., vol. 62, 2015, pp. 359–36.

Layout (TSMC 40nm)

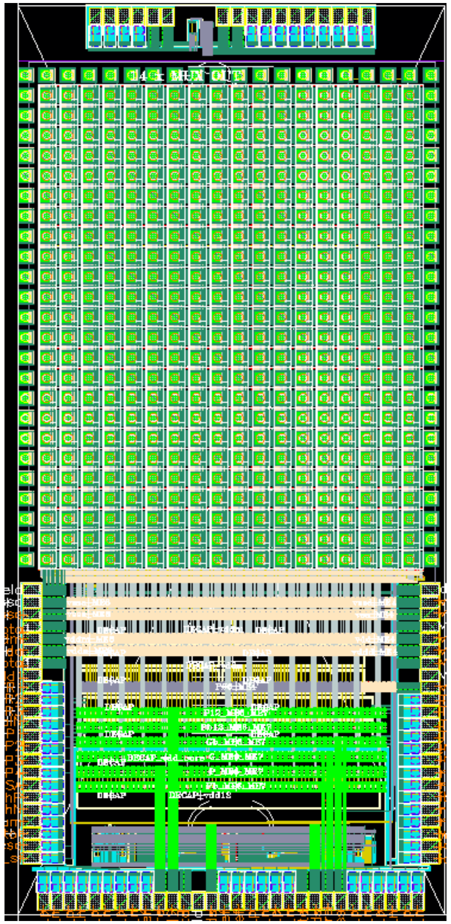
Single pixel 100x100 um²



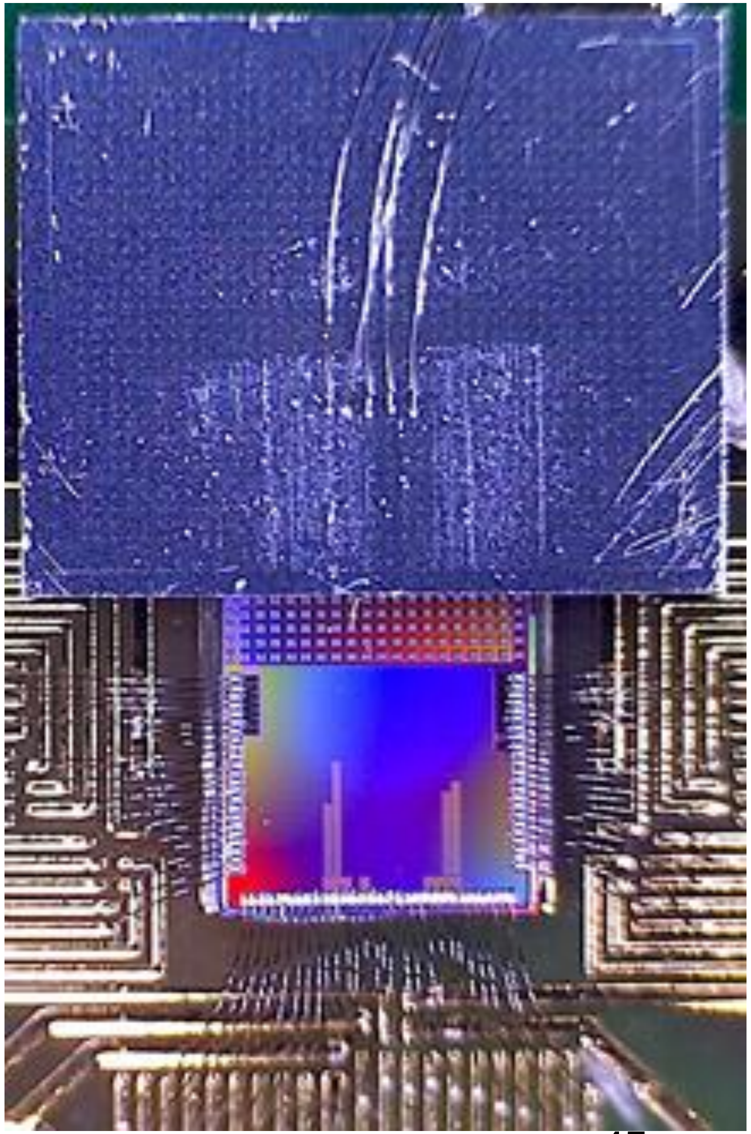


Chip 2.5x4 mm²

pixel matrix 18×24



Chip photo

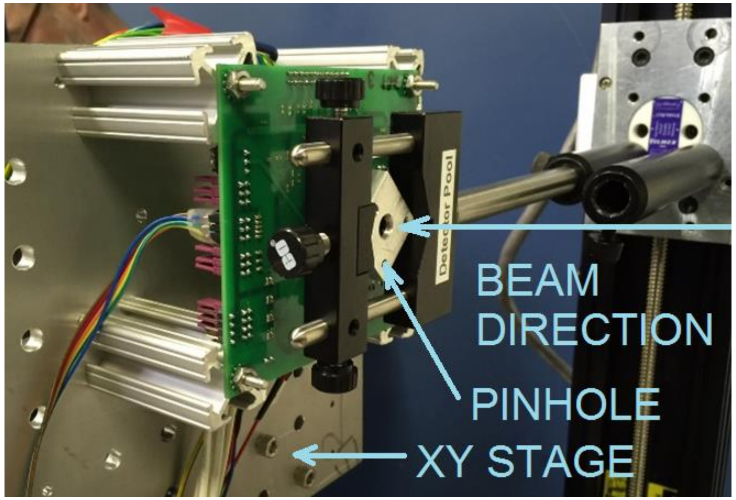


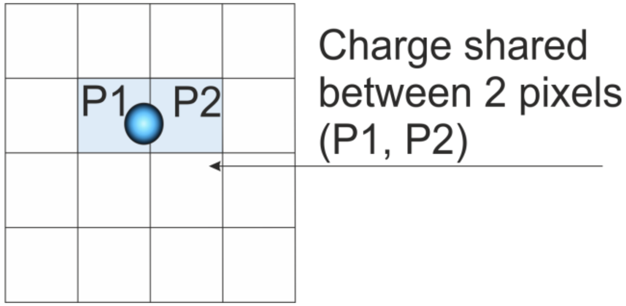
Because in our case the bump bonding is done on the chip-to-chip basis it has pitch limitation. As a result of that, the prototype has the pixel size of **100 x 100 µm²**, despite the fact that significantly smaller pixels could be achieved in this technology node.

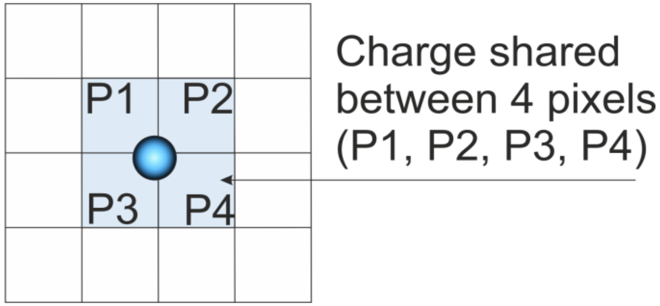
Standard counting vs. C8P1 (X-ray measurements)

The module tests:

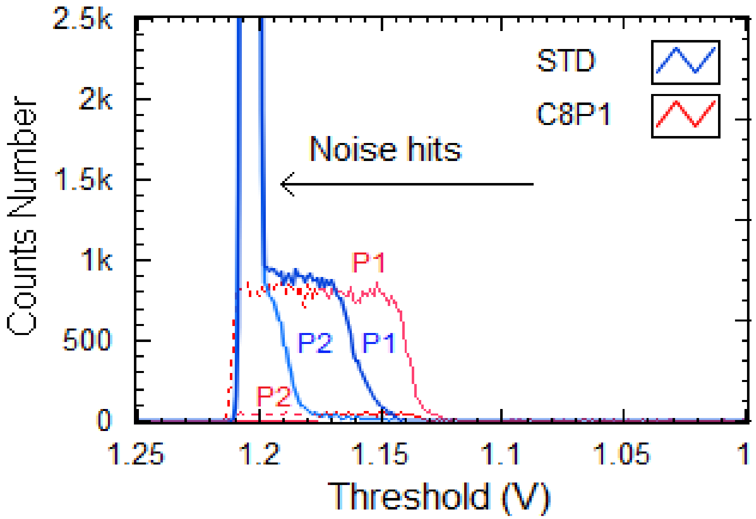
- the APS at the ANL, the 1BM-B beam line
- 8 keV energy beam (target for future application),
- the pinhole diameter 3.5 µm
- the beam intensity of 10-30 kphotons/s per pixel
- Step motor -XY positions adjusted with step 5 um

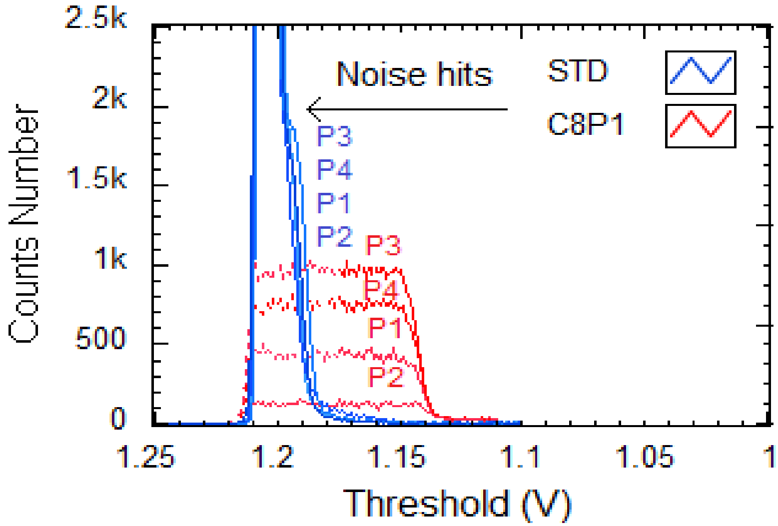






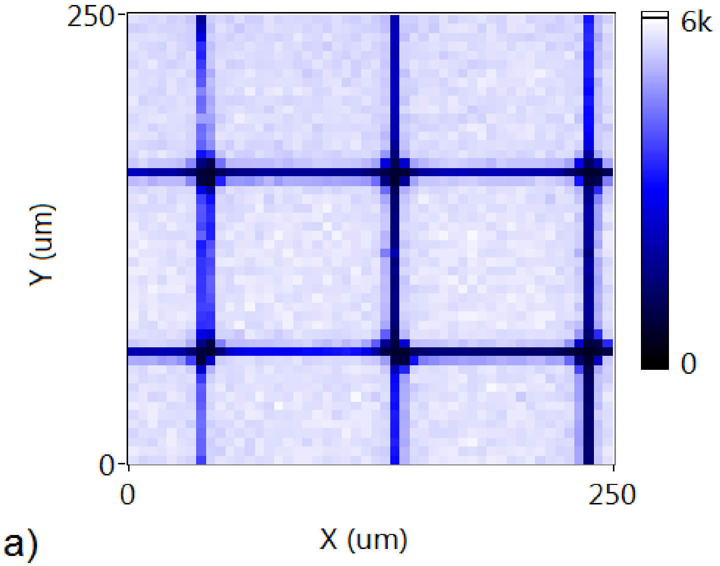
Example of measure integral spectra



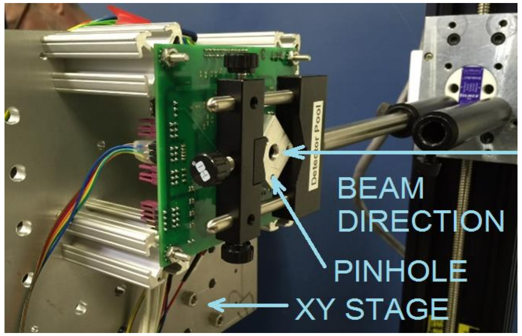


XY scaning with step 5 um (pencil beam ϕ= 3.5um) - ANL

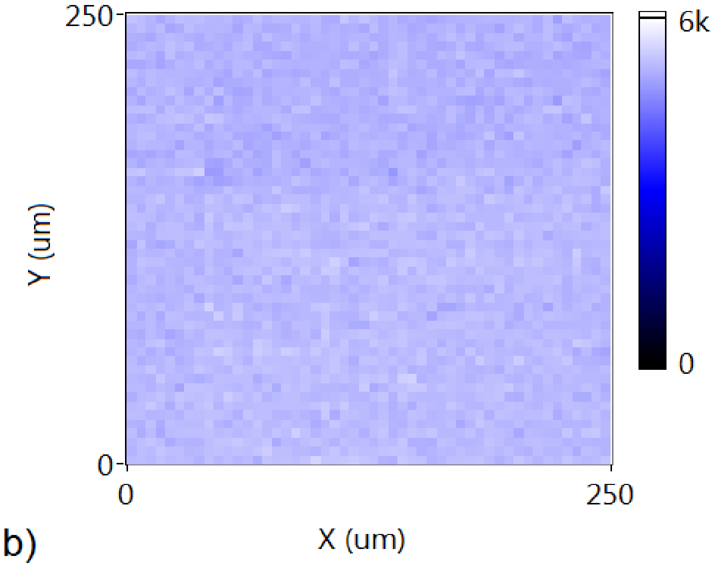
Standard counting



a)



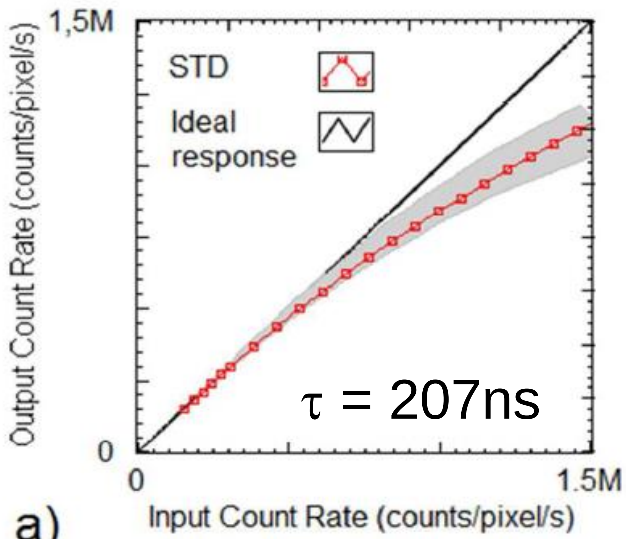
C8P1



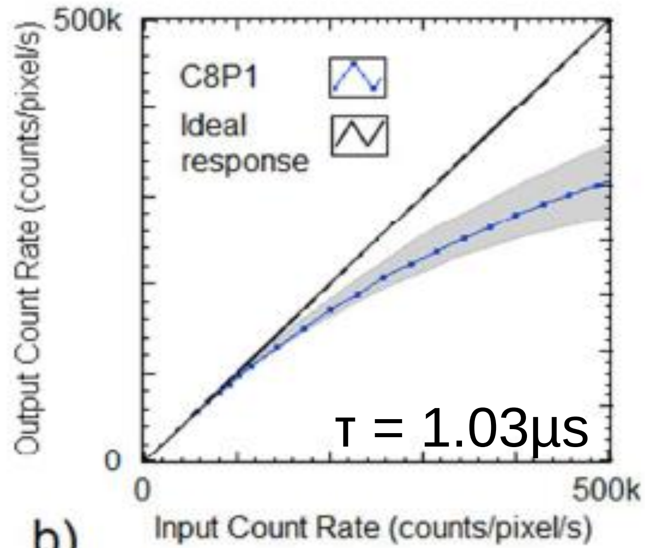
b)

Count rate performance

$$N_{out} = N_{in} e^{-\tau N_{in}}$$



a)

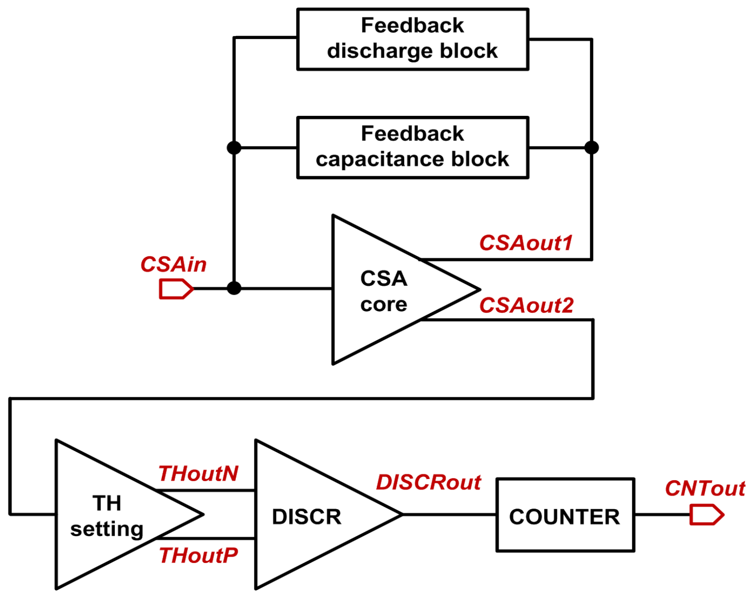


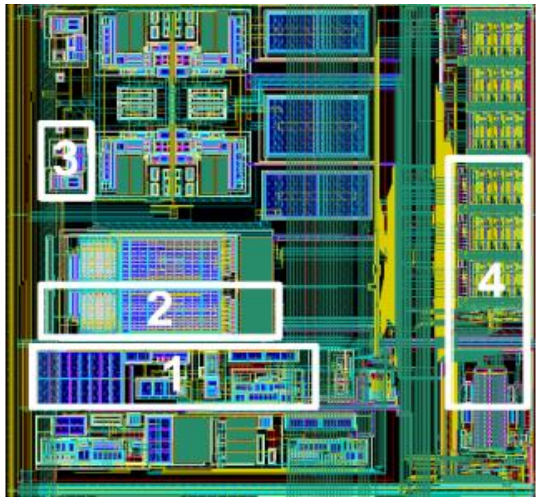
b)

A. Krzyzanowska et. al
Submitted to IEEE TNS 2017

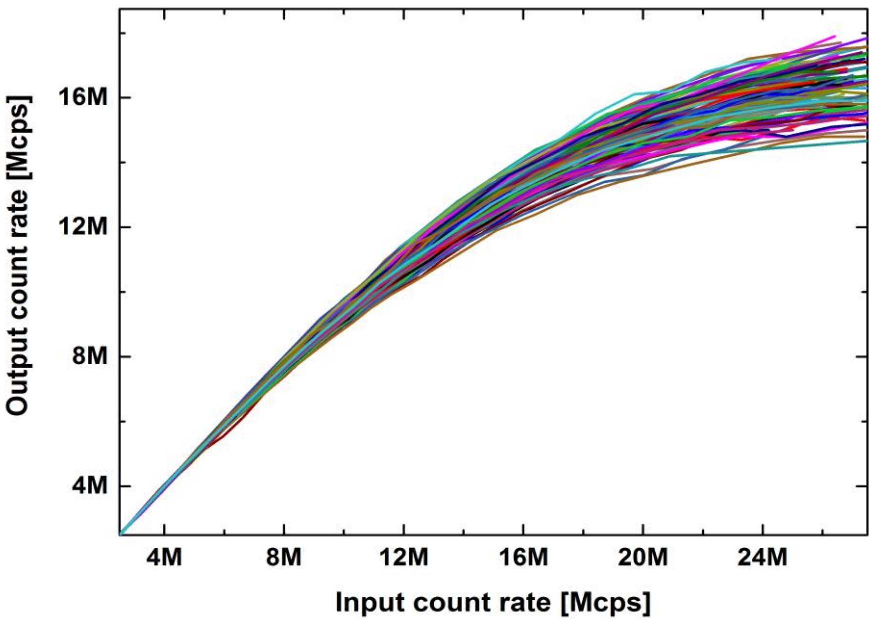
1. Can we count faster in single photon counting mode?
2. 2. New algorithms for elimination of charge sharing are necessary.

Ultra fast single photon counting IC in CMOS 40 nm





Layout of a pixel – **pitch 100 um:** 1 – CSA, 2 – Threshold setting block, 3 - Discriminator, 4 – Counter and logic



Mode	This work	
	FAST_HC	FAST
Process	40 nm	
Pixel size [μm^2]	100×100	
Power/pix. [μW]	103	46
ENC [e$^-$ rms]	185	212
10% dead time loss input rate # [cps/pixel]	12 M	12 M
10% dead time loss input rate # [photons mm^{-2} s^{-1}]	1.2 G	1.2 G

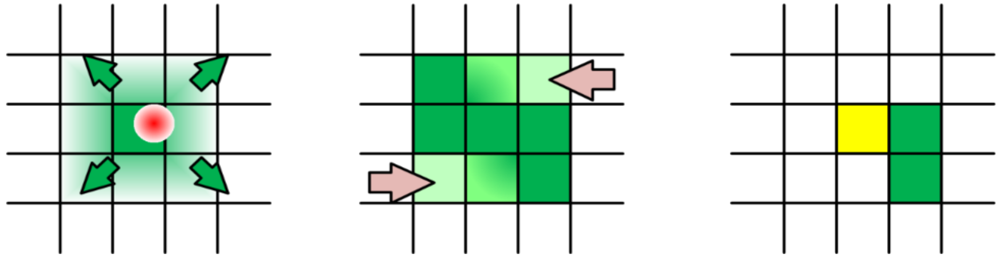
for count ratio $N_{OUT}/N_{IN} = 0.9$

Measured with low energy X-ray of 8 keV data for > 100 pixels

R. Kleczek, et al., IISW, Hiroshima 2017

Pixel Readout with Asynchronous Approximation of a Center of Gravity of a Charge Distribution from a Radiation Conversion Event

New approach based on pattern recognition. Allocate a hit to a single pixel basing only on the form of the area affected by the charge cloud



Formation phase ⇒ Contraction phase ⇒ Resolution phase

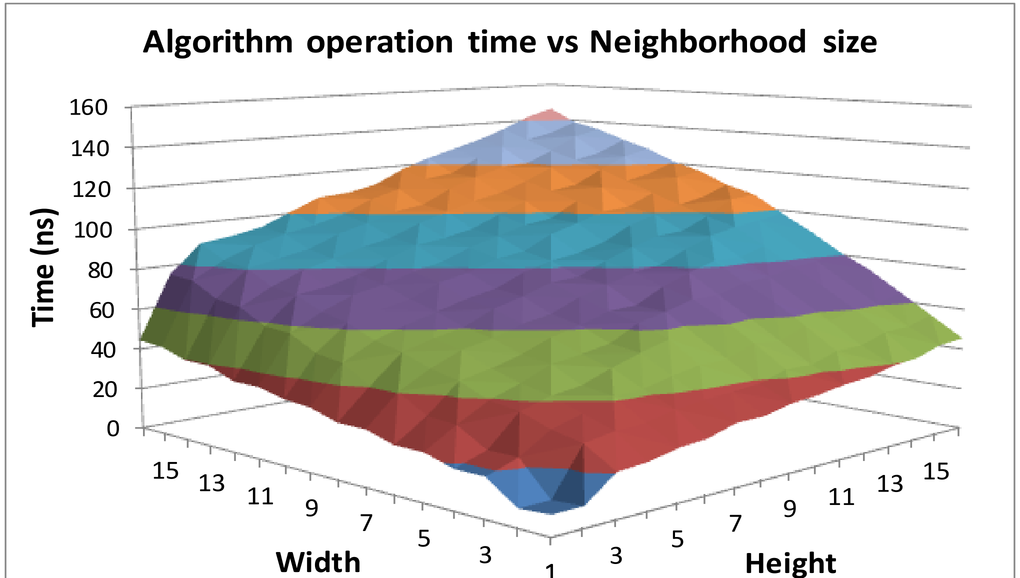
Advantages:

- Limited analog processing circuitry (shaper/amplifier, summing node, discriminator).
- Shorter hit processing time.

Challenges:

- Dealing with asynchronous nature of the events
- Identification of pixels belonging to the same event.
- Hit allocation algorithm.

Tested prototype in GF 55nm (digital part only)



P.Otfinowski, G. Deptuch, P. Maj
IEEE JSSC 2017