# Status of Technical Proposal

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# Quick Overview

- TP second draft was ready by the March 16 deadline
  - With modifications based on the comments received from consortium
- Last week (week of April 9) we received comments from two internal reviewers of the TP chapter
  - Referees are outside of the consortium, but DUNE members
- Some additional information was added to improve the draft according to the suggestions from the referees
- Currently the TP is in the final stages of editing performed/coordinated by the overall editors of the two volumes before submission to LBNC in May
- The latest version of the document is always publically available on the DUNE github (https://github.com/DUNE/Technical-Proposal)

# Modifications

- The charge readout electronics must be able to measure signals of up to 1200 fC without saturation; this has been optimized following Monte-Carlo studies on the maximal occupancy per channel in shower events [2]. For a nominal CRP gain of 20 a MIP signal is expected to be around 30 fC — the lowest limit that assumes a particle travelling horizontally with an azimuthal angle of 0 degrees — giving the maximal operation range of up to 40 MIPs.
- The electronic noise in the CRO analog electronics is required to be $<2500\,e^-$. This condition can be derived from the requirement on the minimal S/N, which should be greater than 5:1 once the charge attenuation is taken into account. Given the maximum drift distance of 12 m, the largest attenuation factor due to electro-negative impurities assuming the nominal 3 ms electron lifetime and the drift field of 0.5 kV/cm is 0.08. The smallest MIP signal with the CRP effective gain of 20 is therefore 2.5 fC (15,600 $e^-$).
- The peaking time of the FE analog amplifiers should be 1 µs. This requirement is driven by the the need for optimal vertex resolution, determined in turn by the single track resolution and the power to separate two or more tracks that are close to one another.
- The sampling frequency should be 2.5 MHz to match the peaking time of the FE electronics.
- The power dissipated by the FE analog electronics must be below 50 mW/channel in order to minimize the heat input to the cryostat volume.
- The FE analog electronics should be replaceable without the risk of contaminating the main LAr volume to guarantee the long-term reliability of the system.
- The ADC resolution should be such that that the noise is at the level of an ADC, while dynamic range wide enough to match the response of the FE amplifier. This can be achieved with a 12 bit ADC.
- The digital electronics to be placed outside of the cryostat in the warm environment can adopt standard industrial components and solutions.

This was the most substantial addition to the draft in Section 5.1.2 “Design Considerations”

Based on docdb-6428

The structure of this list of requirements is similar to the one found in the chapter on the SP TPC electronics

Actually the requirements are the same (minimal S/N, shaping time, frequency, power dissipation, ADC dynamic range …)

# Modifications

Also in Section 5.1.2 "Design Considerations"

The magnitude of the noise also has an effect on the quality of the lossless compression of the raw data.A compression factor of about 10 could be achieved with the RMS noise level below 1 ADC, while with the noise at around 1.5 ADC the compression factor of 4 is obtained.

The compression factor for 1.5 ADC RMS was investigated for the 3x1x1 data
With the uTCA link of 10 Gbit/s and total data rate for charge readout is 18 Gbit/s, so the required minimal compression factor is < 2

In section 5.2.3 and 5.2.4 we added some further explanations on down-sampling from the ADC native rates of 40/65 MSPS

fig:dpele-amc-scheme

Figure 5.7 shows block diagram of the AMC functionality. Each AMC generates a continuous compressed stream of 2.5 MSPS 12 bit data per readout channel. The on-board ADCs operate at a rate of 25 MHz per channel. The data are down-sampled in the FPGA to 2.5 MHz by performing ten-sample averaging, which leads to the further digital filtering of the noise. The data, consisting of only the 12 most significant bits from each digitized 14 bit sample, are then compressed using an optimized version of the Huffman algorithm and organized in frames for transmission. The frames

For normal operation, in continuous sampling mode, the time samples will be down-sampled by the FPGA to a coarse 400 ns sampling to match that of the Charge Read Out and limit the quantity of data streamed. The use of a higher specification ADC, with time-sampling of 15.4 ns, allows for greater flexibility. It is envisaged that for particular calibration runs, waveforms with finer time-sampling could be read-out which would allow studies of, for example, the liquid argon scintillation time-profiles. Even in normal operation, online pulse processing is possible within the FPGA using the finer time-sampled waveforms (before the down-sampling), which could be used to make continuous measurements such as the rise and fall times of the pulses. Even at the coarse

# Modifications

In section 5.2.4 “Electronics for Light Readout” we made clarified how signals are split between CATIROC and ADC branch

The analog signals from each PMT channel are split equally into two separate branches

fig:dpele-lro-scheme

In section 5.5.6 “Commissioning” we made explicit what validation tests could be performed on the SFT chimneys post installation

The SFT chimneys are commissioned as a first step. This consists of evacuating and then filling them with nitrogen gas at slight overpressure with respect to the atmospheric pressure. To ensure that no damage happened to the flange interfaces during installation, the chimney vacuum tightness can be verified again at this stage by checking leak rate when the chimney is under vacuum and monitoring the nitrogen pressure once it is filled.

+ fixed to minor changes to wording, typos, improvement to figures (better resolution images)

# Summary

The TP chapter for DP electronics design looks to be on track to be ready for the submission to LBNC in May at the time of the DUNE collaboration meeting