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Fermilab LLRF Systems Architecture and Overview

B. Chase/P. Varghese

Fermilab LLRF Systems

17 April 2017

LLRF System Architecture

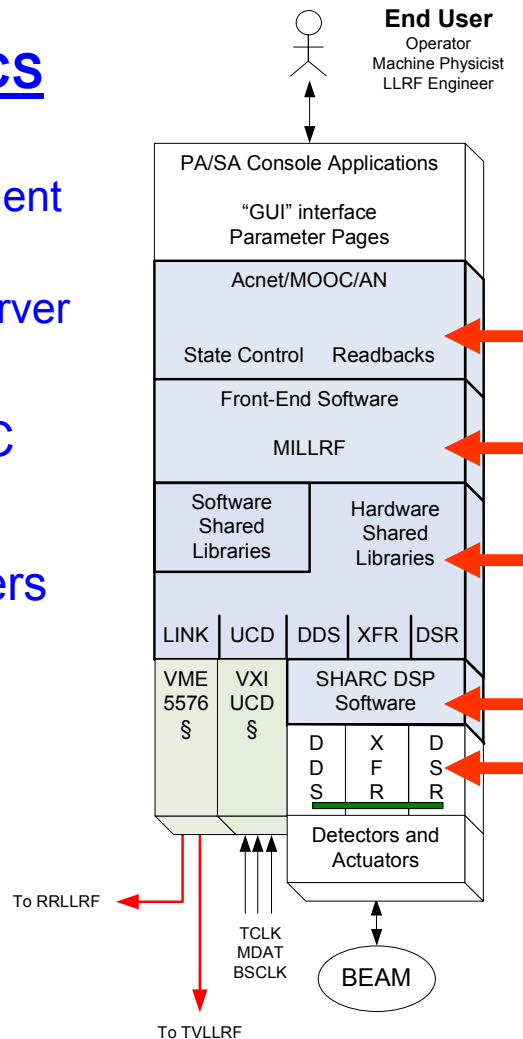
EPICS

CA Client

CA Server

IOC

Drivers

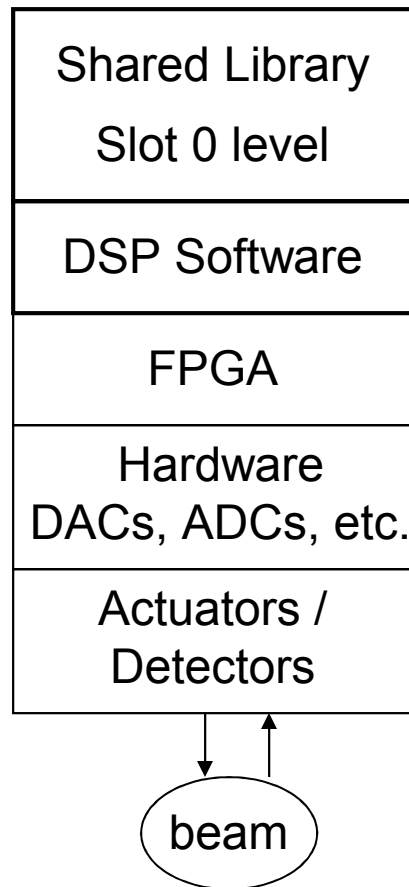


- AcNET Interface – requestor
- Front-end software - director
 - User interface
 - Scenario execution
- Shared Libraries – workers
 - Software – logger, event, cog,...
 - Hardware – link, VXI-UCD, VXI
- DSP Software – serfs
 - Patterns
- VXI Module Hardware
 - 40 MHz AD-SHARC™ DSP
 - ADCs, DACs, NCOs, Link ports

Front-End Software

- The “application program” or *.exe file (VxWorks)
 - Provides set of services or tools to end-user.
 - Coordinator of tasks within front-end by combining services provided by different modules.
 - Responds to IRQs, TRIGs or external requests for data.
 - Error detection, logging and recovery.
- Basic Control System Interface – devices (PV)
- Advanced Control Interface – I6/R6
 - Scenarios - UseManager, Multi-timer

VXI Module Software



- DSP Software Patterns
 - Vector Interrupts
 - Link Port Communication
 - Scheduler
 - Fast Time Plot Variables (PV)
- Object Based Methodology
 - Construction
 - Configuration
 - Information

Software Modules

- AN (Channel Access Server)
 - Acnet interface, callback mechanism
- Event
 - Observer pattern or Publish-Subscribe model
- Logger
 - Message queue used to log error messages
 - Different message levels, information content
- Cog
 - manages cogging beam to specific RF buckets
 - Details of cogging hidden, interface clear

DSP Software

- Multiple processing rates
 - 100 kHz, 16.6 kHz, 720 Hz
- Common software patterns
 - Scheduler – schedules work tasks
 - Vector Interrupts – slot 0 to DSP interface
 - FTP Variables – accelerator data variables
 - Link port communication - high speed data transfer between multiple modules.

MILLRF Front End Software

- Construction and Configuration
- I6 PA Interface
 - Use case scenarios
 - Multi-timer and UseManager
- Middleware
 - Gather resources to accomplish tasks, i.e. feedback state changes, machine transfers
 - Use interface of lower level libraries
- Parameter Page Devices
 - Readings/Settings
 - FTP Variables

16 Primary Application

16 VXi LLRF Novice Mode (most restrictive) 13-APP-18 15:51:26 *gk_tools*

SEQUENCE TABLE VIEWER CURVES ARRAYS required data

Sequence Table View

HrdwrID: [MILLRF] *Send To Hardware *Refresh *Save To Database
MI State: [9 RR slipstack to 120 GeV #2A] Current state: 9

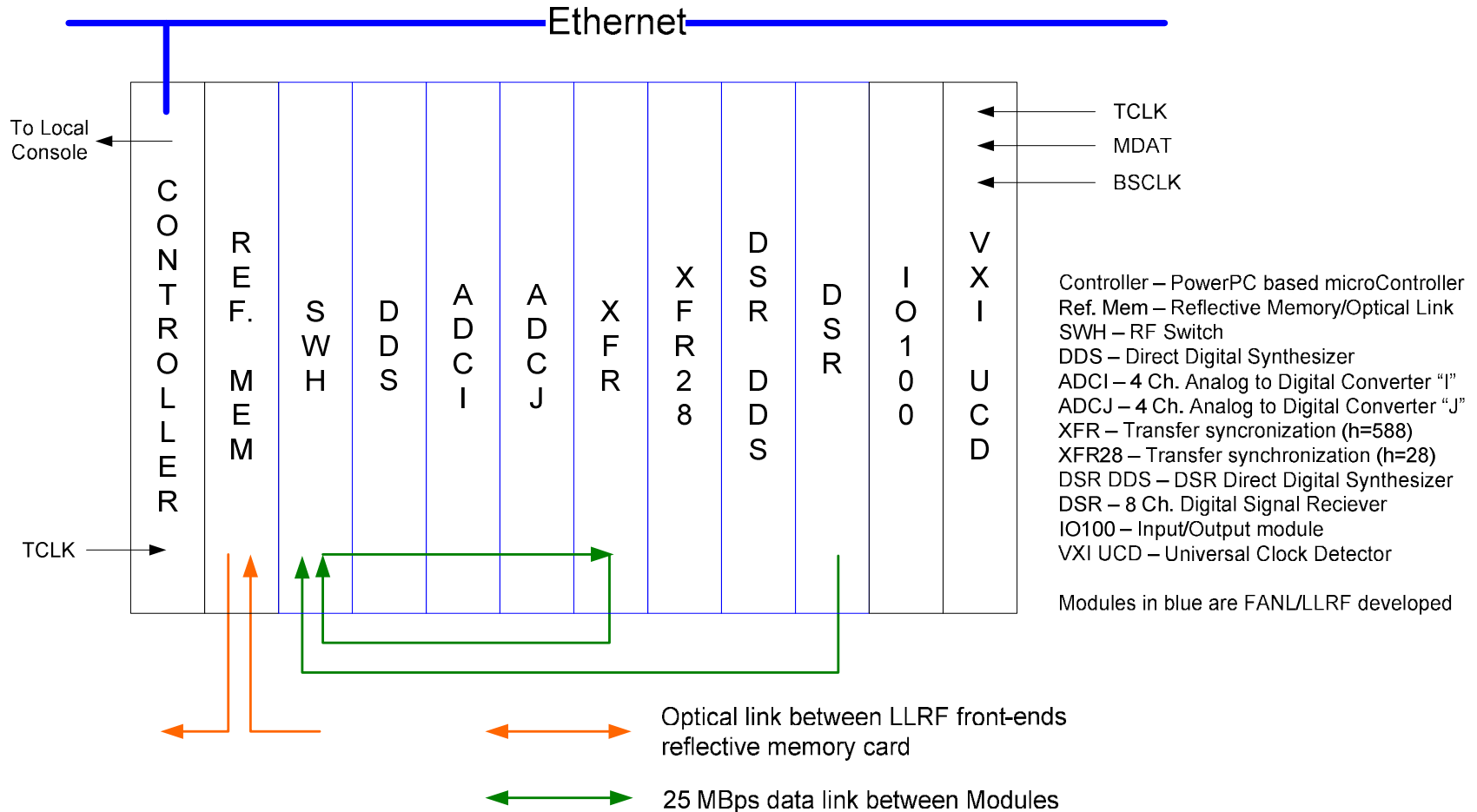
ROW	TYPE	SIGNAL	MESSAGE	DATUM1	DATUM2	DATUM3	DATUM4
0	Event	AnyReest					
1	Continue		EnergyArrATC	0	3047800		
2	Continue		SetPhiisFrontEngatten	46	22		
3	Continue		SetRposGain	0 db			
4	Continue		XfrAlignToRecycler	35	-84	-120	
5	Continue		V555 feedback	ON	10	10	
6	Continue		EnergyArrJumpToFoot	52808000	700		
7	Delay	0.0300000012	V555Appl(t)Curve	All On		.0002	Enable
8	Continue		V555 feedback	ON	10	10	
9	Event	RRPInject					
10	Delay	0.0499959998	EnergyDrpfb	-8	-8000	.08	All DSR
11	Delay	0.2249999940	EnergyDrpfb	-8	-6000	.1	All DSR
12	Delay	0.2450000048	EnergyDrpfb	-8	-8000	.04	All DSR
13	Delay	0.6250000000	EnergyDrpfb	-2	-2000	.1	All DSR
14	Delay	0.6416659951	QdotFbOn			0	120gev LFF
15	Delay	0.6516669989	EnergyRampToFoot	53103480	.022		
16	Event	EndCycle					
17							
18							
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28							
29							

Messages

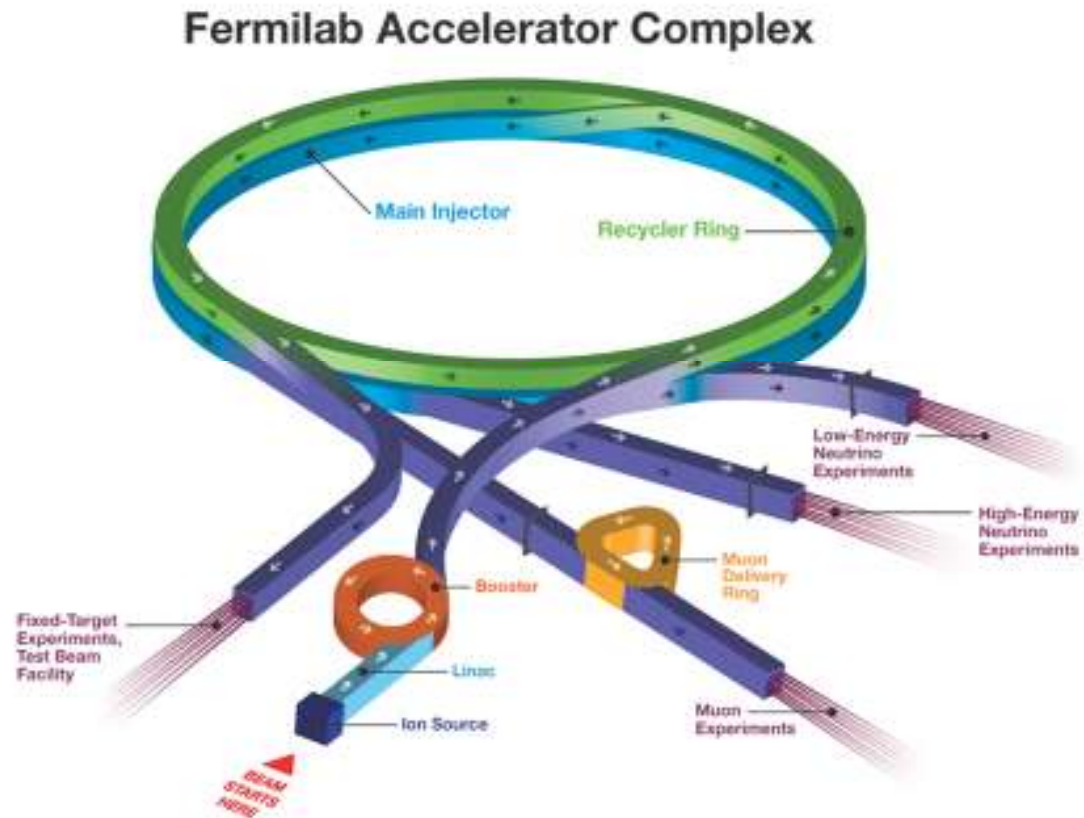
```

SEQUENCE : Receiving User Locks
SEQUENCE : Requesting User Locks
SEQUENCE : Releasing User Locks failed | LOCK_INVARS
LLRF: initialized on CNS->127
PDM: Signal help disabled
PDM: Message help disabled
PDM: Bubble help enabled
    
```

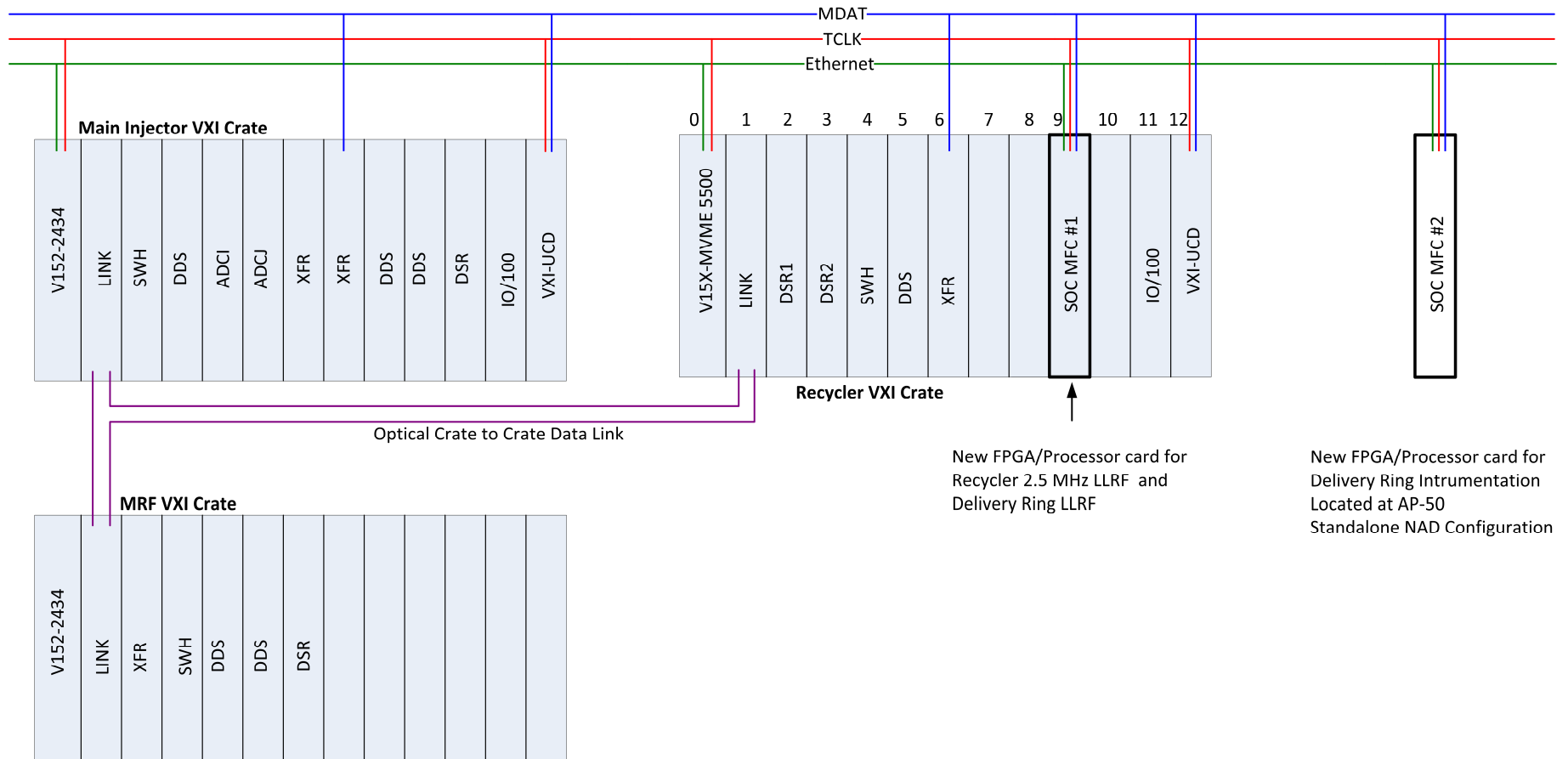

MILLRF LLRF VXI Crate



Booster, Recycler and Main Injector



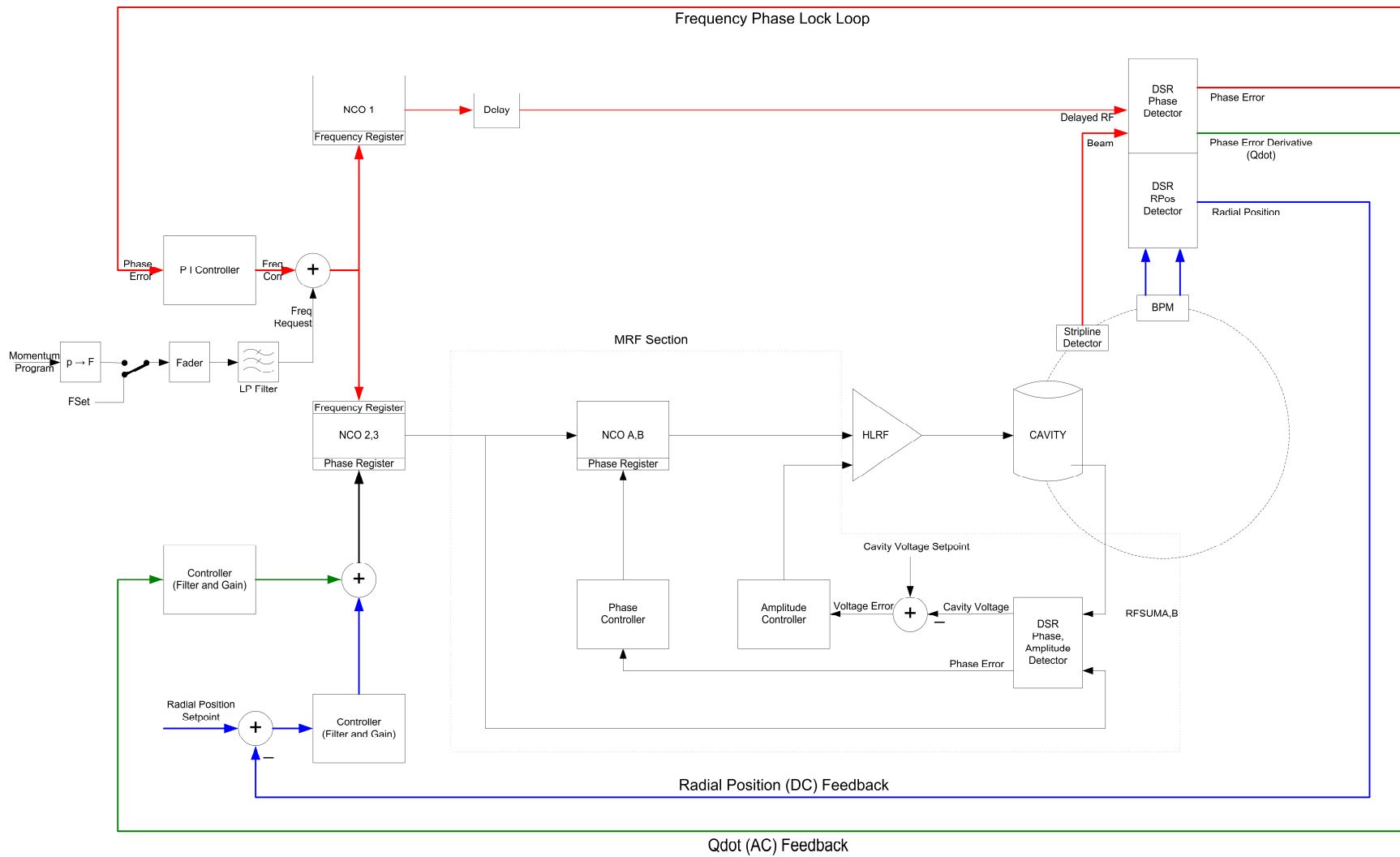
Recycler/Main Injector LLRF Systems



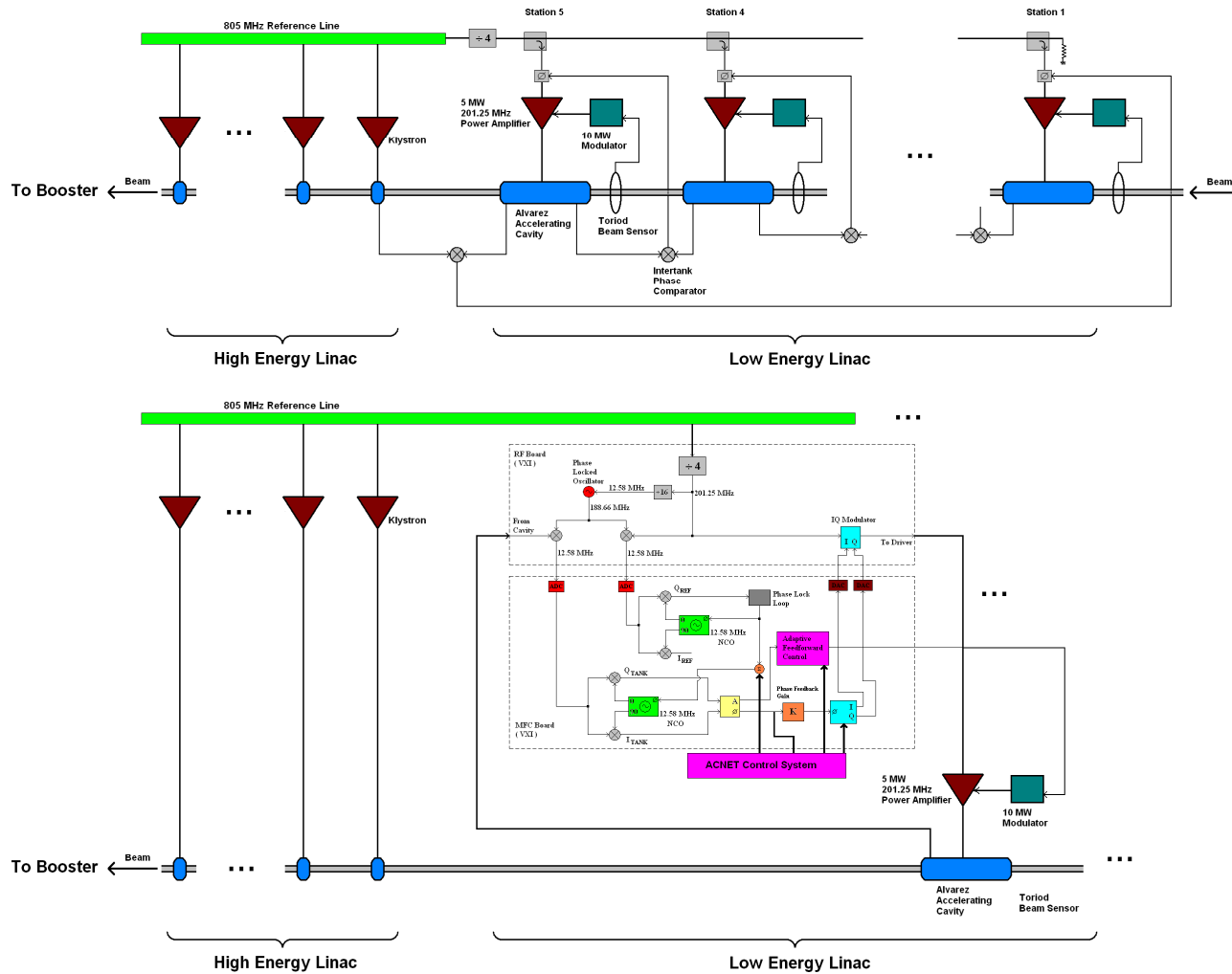
Recycler/Main Injector LLRF Systems



Main Injector Feedback Loops



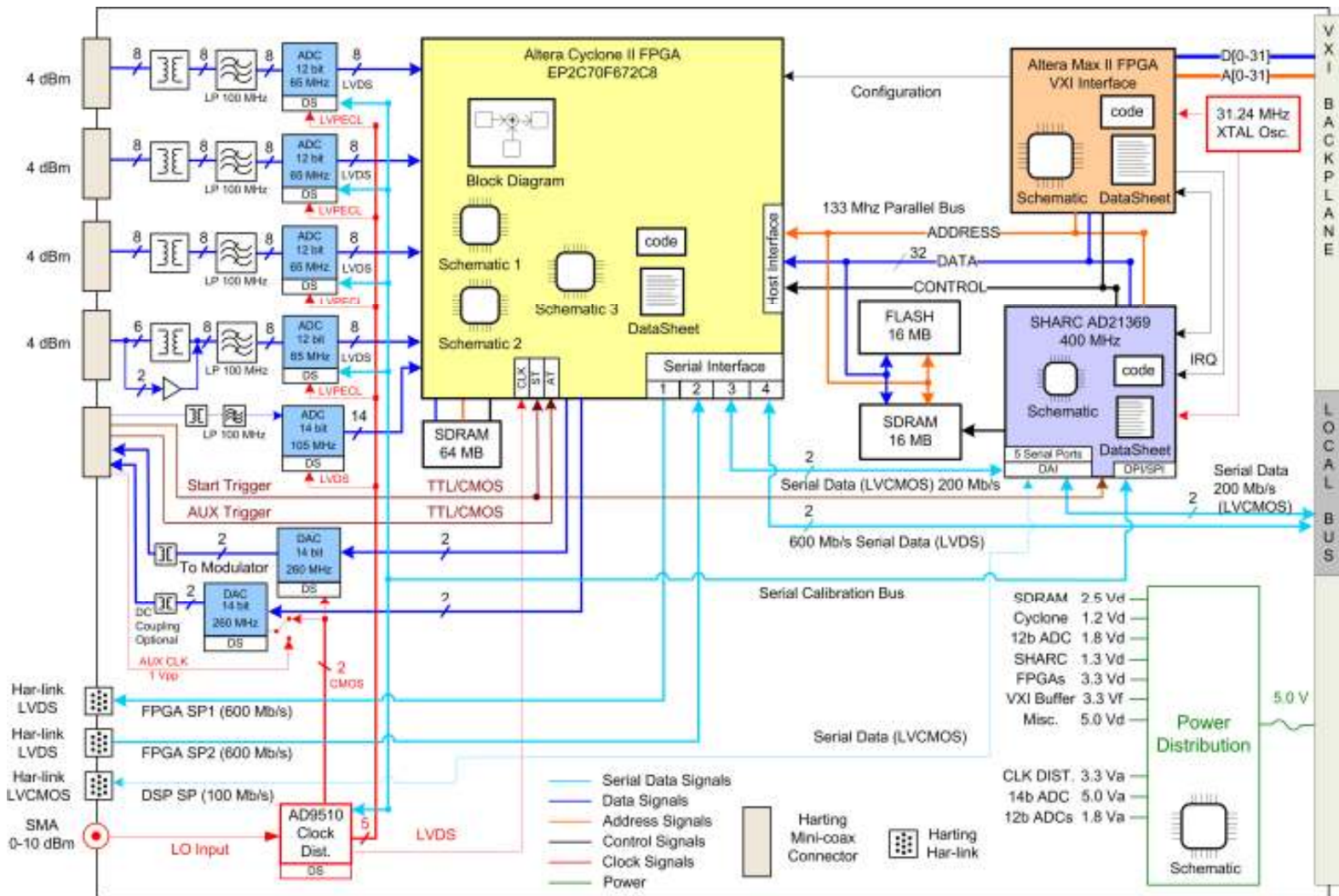
LEL LLRF System



LEL LLRF Station

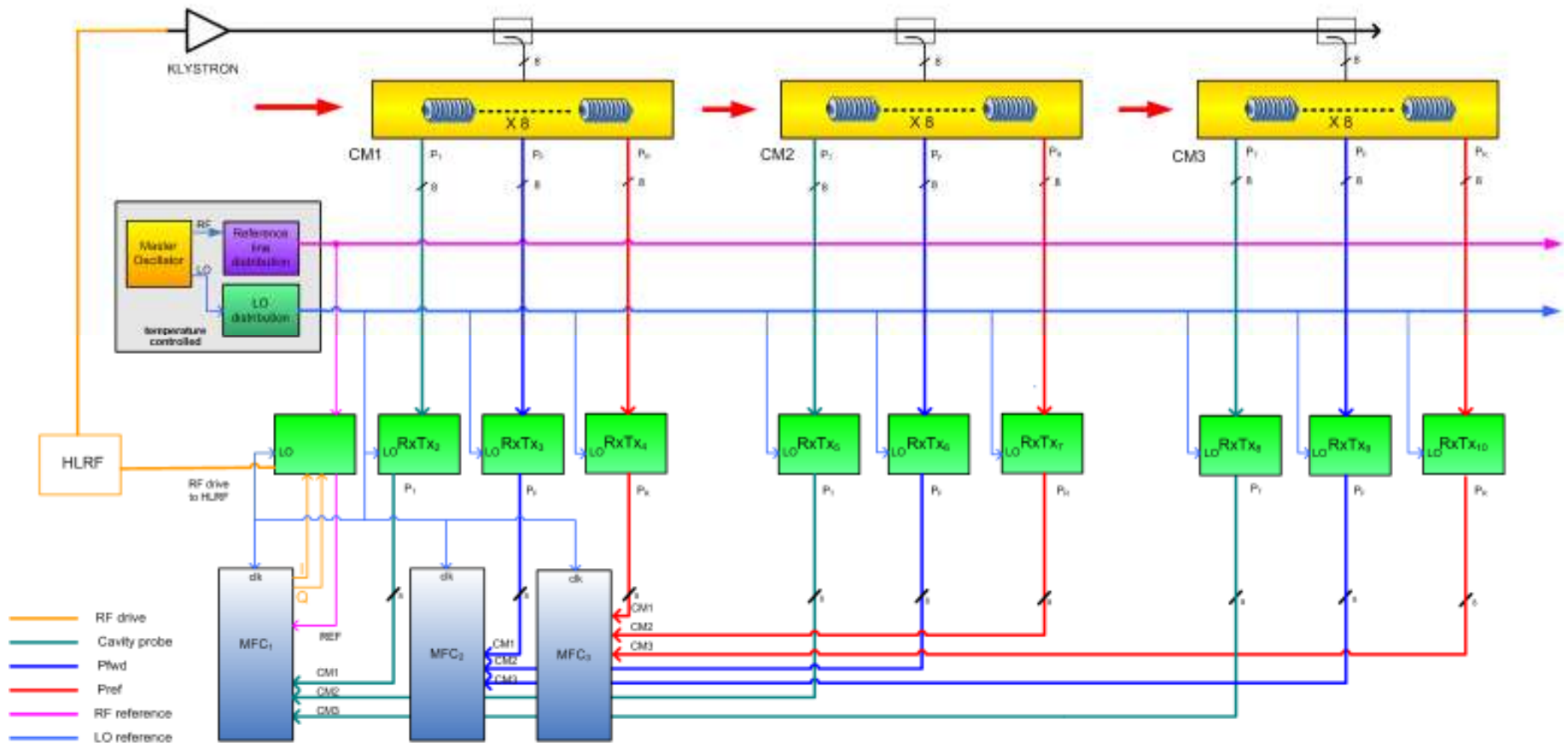


MFC FPGA/DSP Board



FAST LLRF System

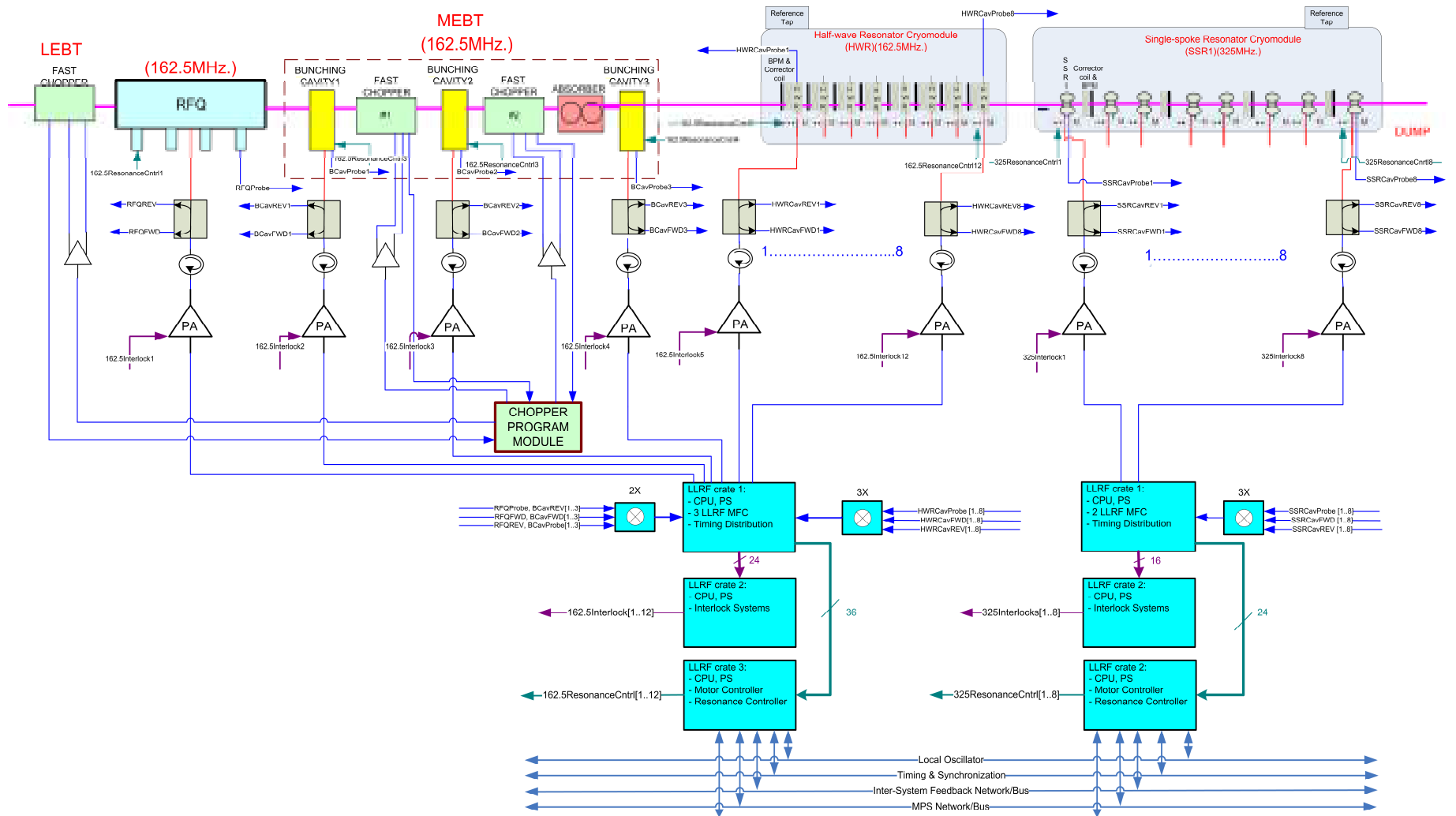
NML LLRF System



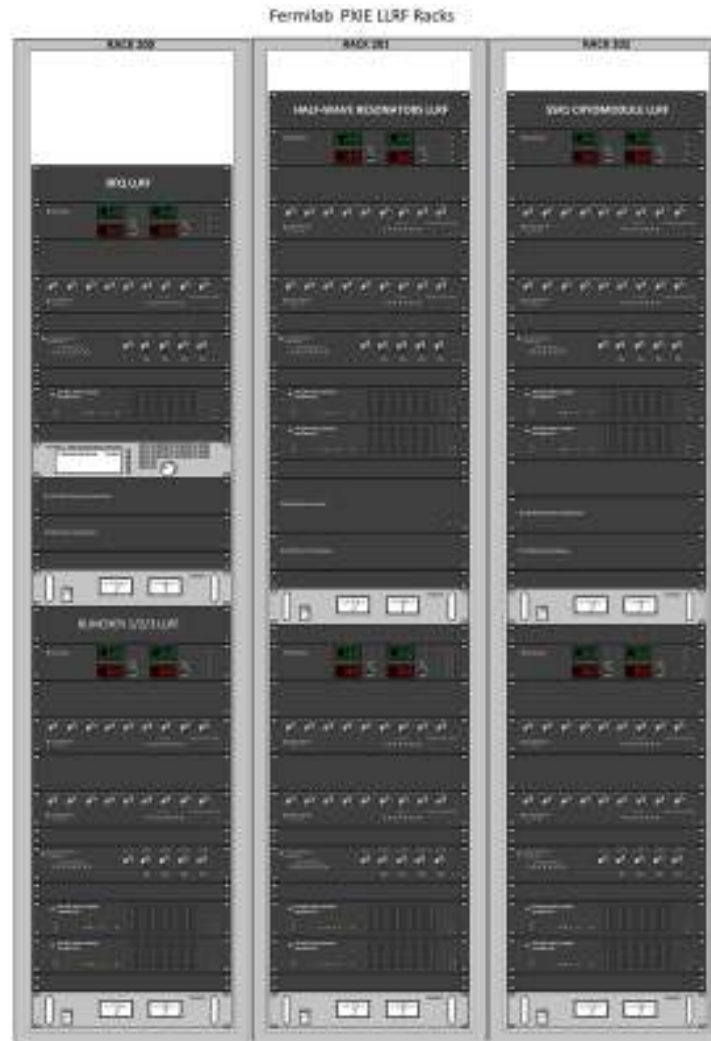
FAST LLRF Station



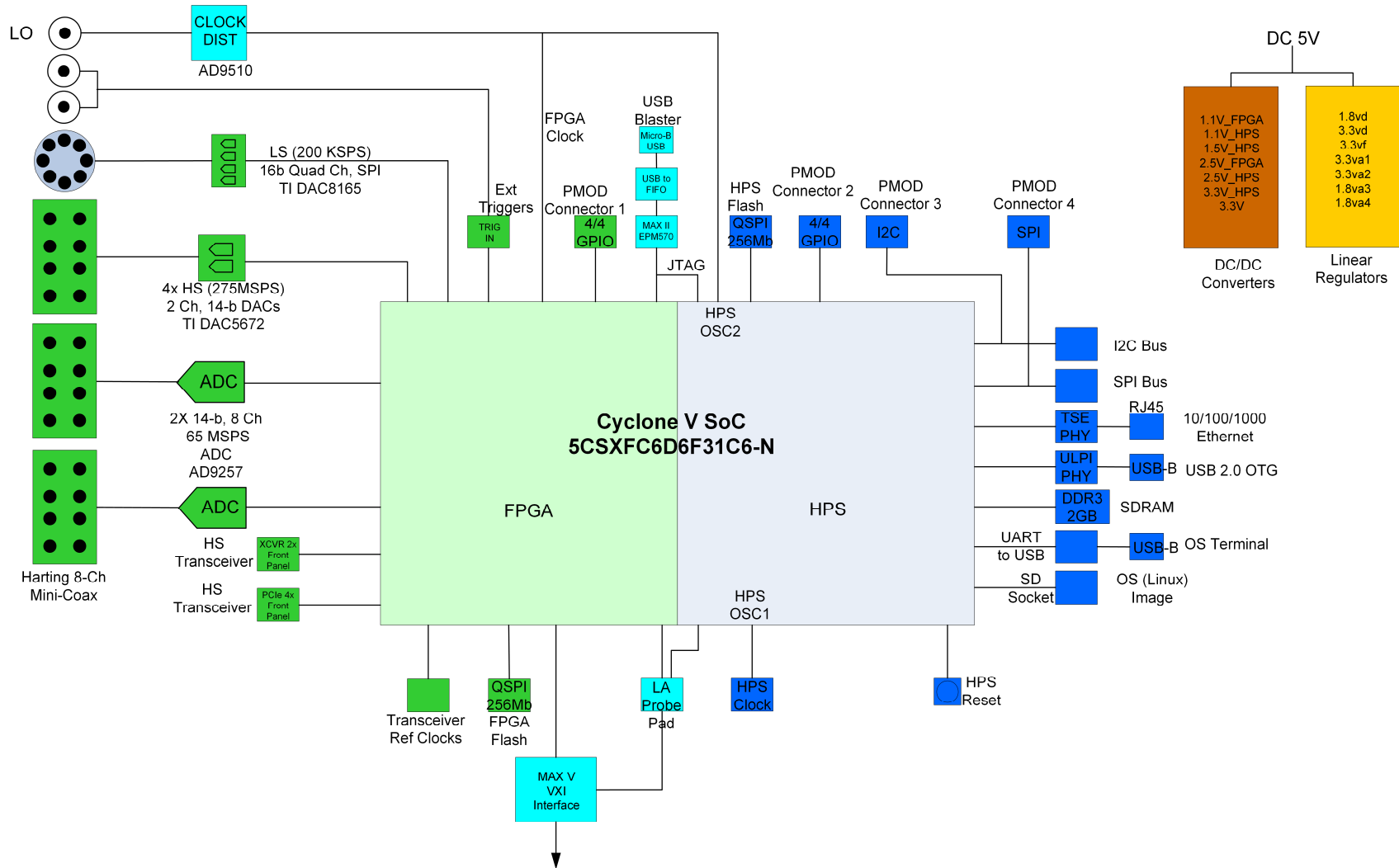
PIP-II IT LLRF System



PIP-II IT LLRF Racks



SOC MFC Overview



ARRIA10 SOC MFC Overview

