CERN

Overview of the SPS LLRF upgrade

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CERN Accelerators Complex

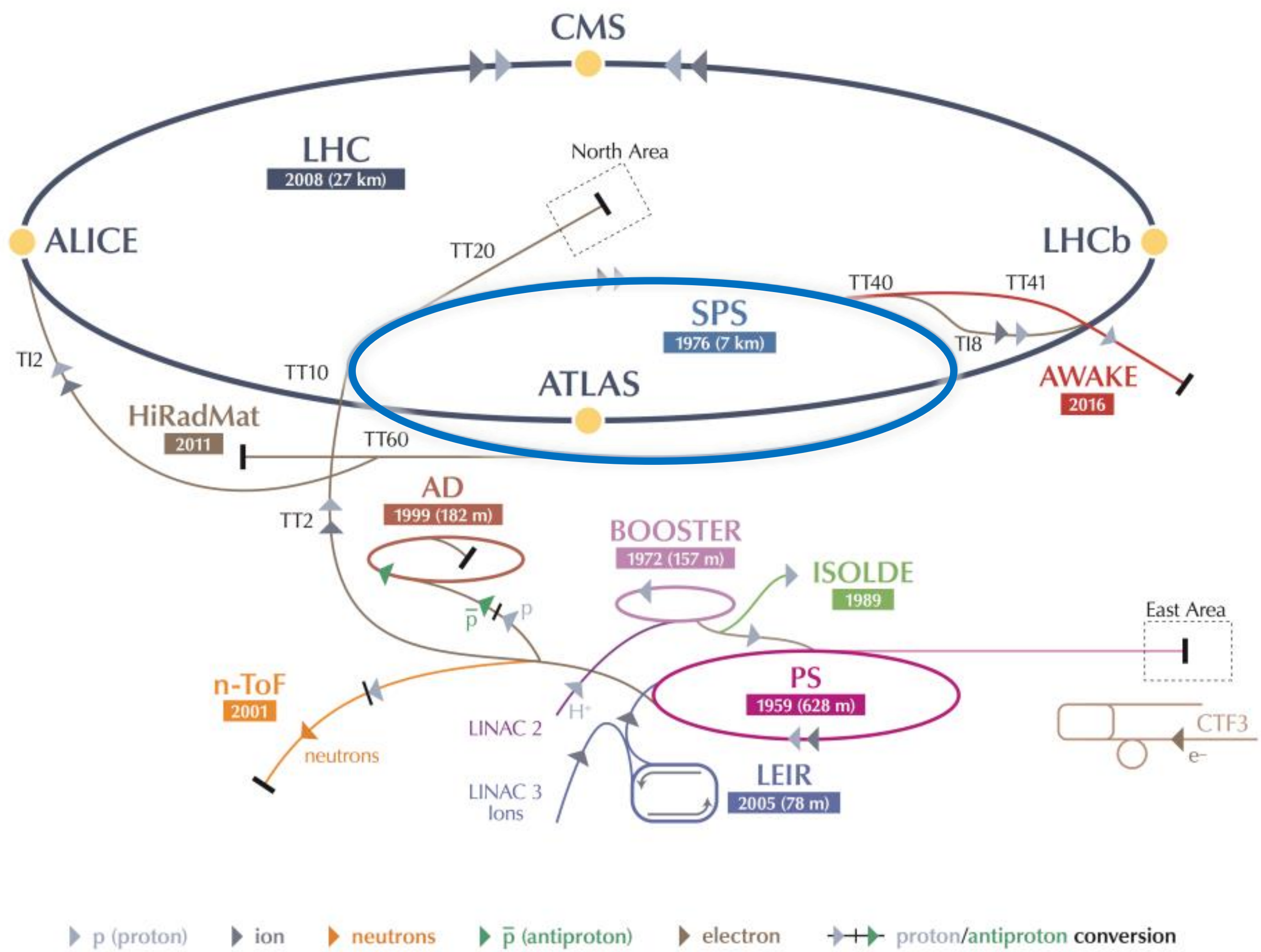


Fig1 - CERN Accelerators Complex

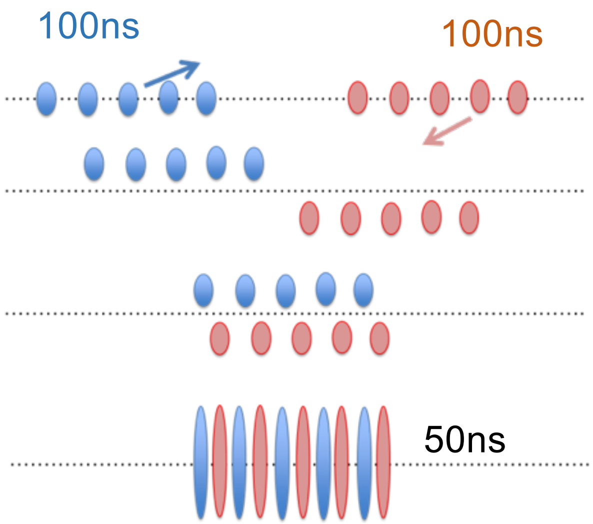
SPS RF Upgrade 2019-2020 (LS2)

High Lumi LHC Beam requirements

- Proton [1]:
  - Doubling intensity → $2.5 \cdot 10^{11}$ p+/bunch
- Ions [2]:
  - 50ns bunch spacing → slip stacking
  - long injection plateau (~40s) → low noise

Main limitations

- Beam-loading
  - V_{RF}=1MV, ~2MV beam induced
- Longitudinal instabilities (impedance)



Courtesy T. Argyropoulos

Fig2 – Ions Slip-stacking [3]

SPS RF Upgrade 2019-2020 (LS2)

RF systems :

- 4x 200MHz cavity → 6 cavities
- 2x 800MHz cavity

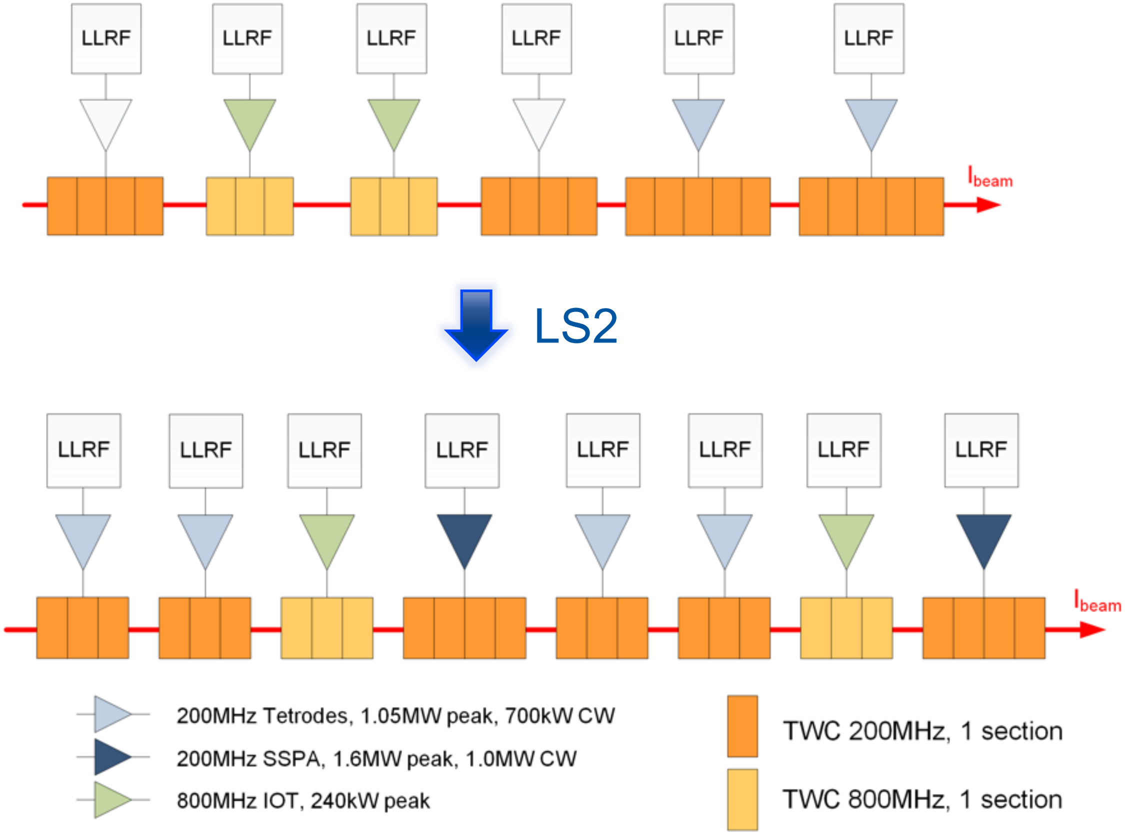


Fig3 – SPS Power upgrade

SPS 200MHz Cavities

4 Travelling wave cavities (TWC200)

→ Splitted into 6 cavities after LS2

(Better compromise with beam loading & Cavity Voltage)

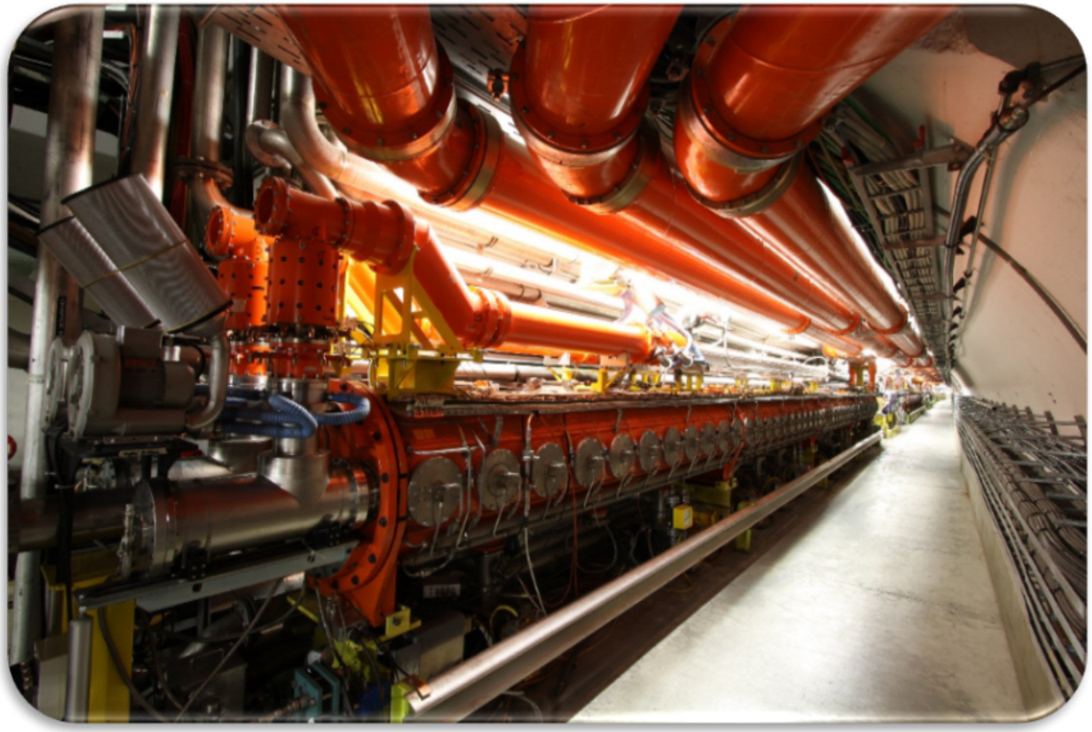
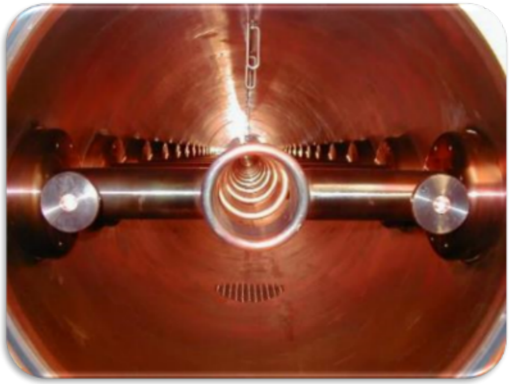


Fig4 – SPS TWC200



Drift tubes structure

SPS 800MHz Cavities

2x 800 MHz Travelling wave cavities (Tunnel)

4x 60kW IOT amplifiers per cavity (Surface)

Center freq	**800.888MHz**
Phase advance per cell	$\pi/2$
Group velocity v_g/c	+0.035
Cell length	93.5 mm
Total length L (37 cells)	3.460 m
Series impedance R_2	0.647 $M\Omega/m^2$

Disc-loaded structure

$$V_{800} \cong \frac{V_{200}}{10}$$

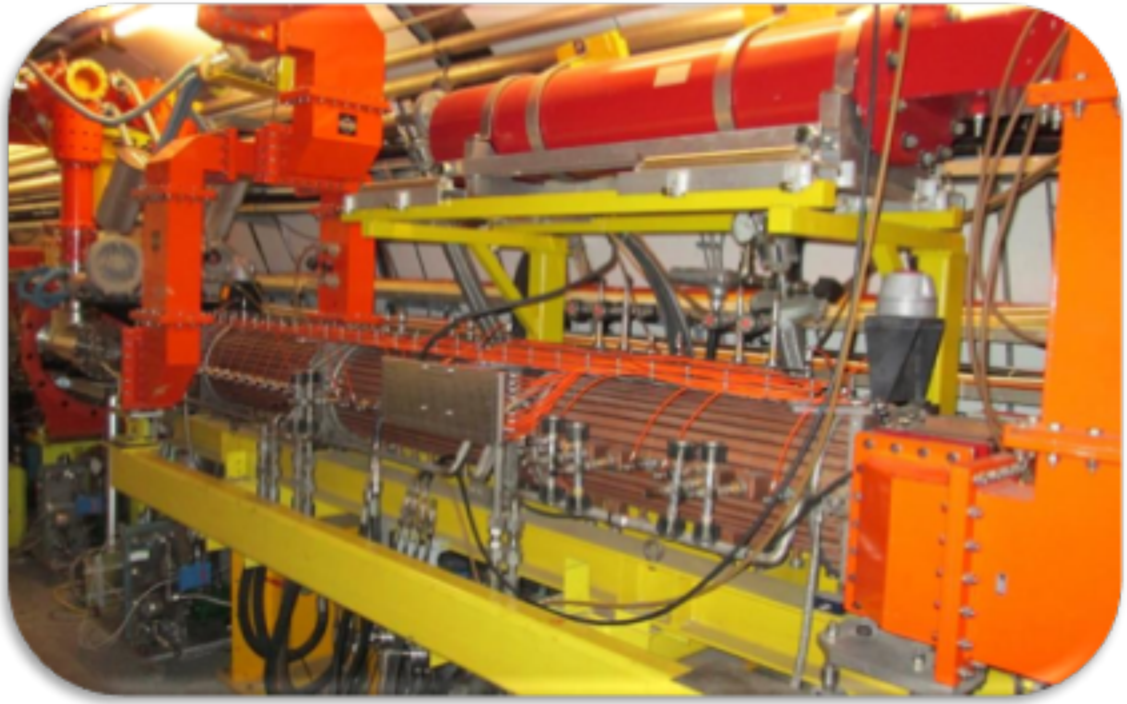
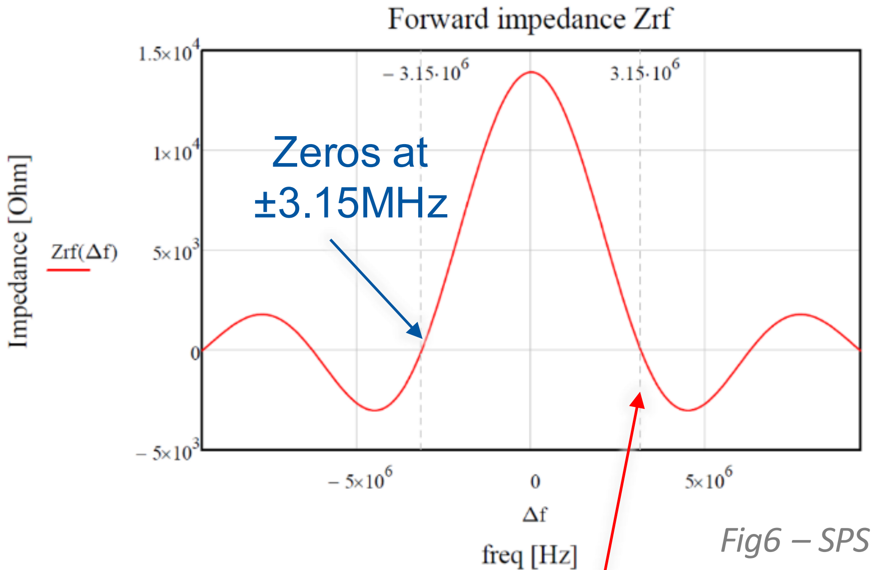


Fig5 – SPS TWC800

LHC proton beam (2-3·10^{10} protons/bunch) unstable without 800MHz system

SPS 800MHz Cavity Voltage

Voltage created by the generator



Voltage created by the beam

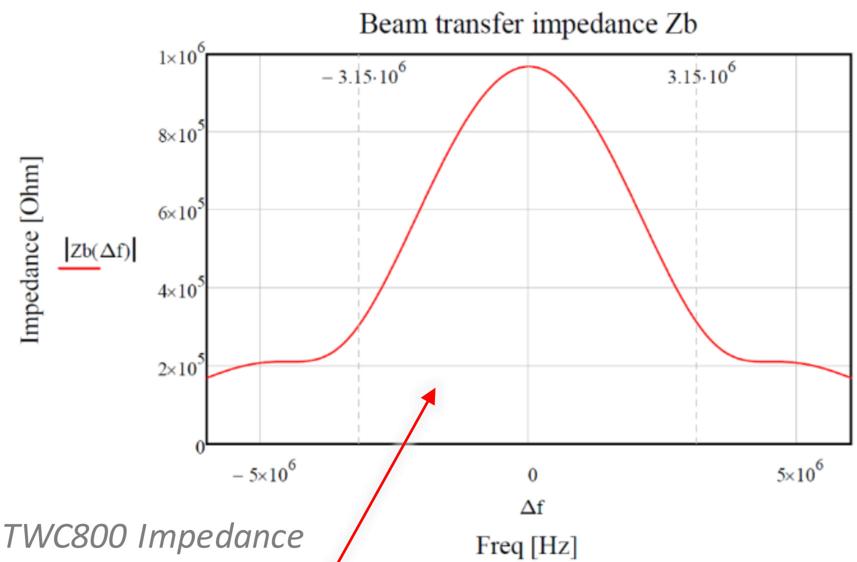


Fig6 – SPS TWC800 Impedance

$$V = L\sqrt{\frac{Z_0 R_2}{2}}\left(\frac{\sin\frac{\tau}{2}}{\frac{\tau}{2}}\right) I_{RF} - \frac{L^2 R_2}{8}\left[\left(\frac{\sin\frac{\tau}{2}}{\frac{\tau}{2}}\right)^2 - 2j\frac{\tau - \sin\tau}{\tau^2}\right] I_b$$

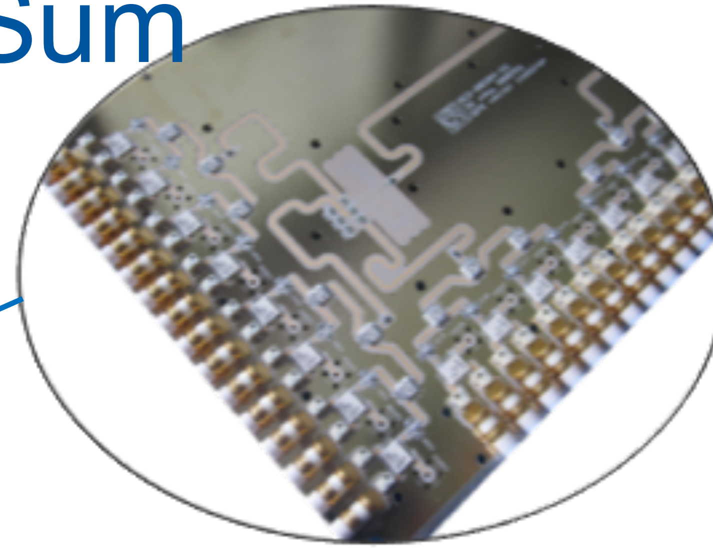
V : Cavity voltage

$$\tau = \frac{L}{v_g}\left(1 - \frac{v_g}{v}\right)\Delta\omega$$

τ : Total phase slip for ultra relativistic p+

SPS 800MHz Vector Sum

Fig7 – RF Combiner



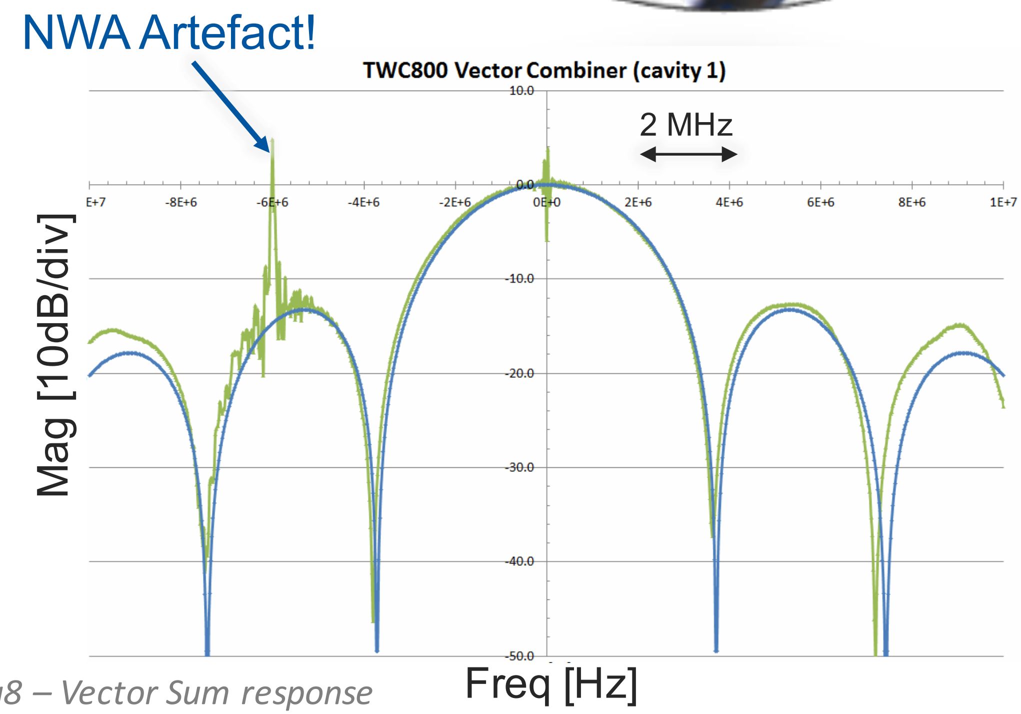


Fig8 – Vector Sum response

SPS LLRF Upgrade

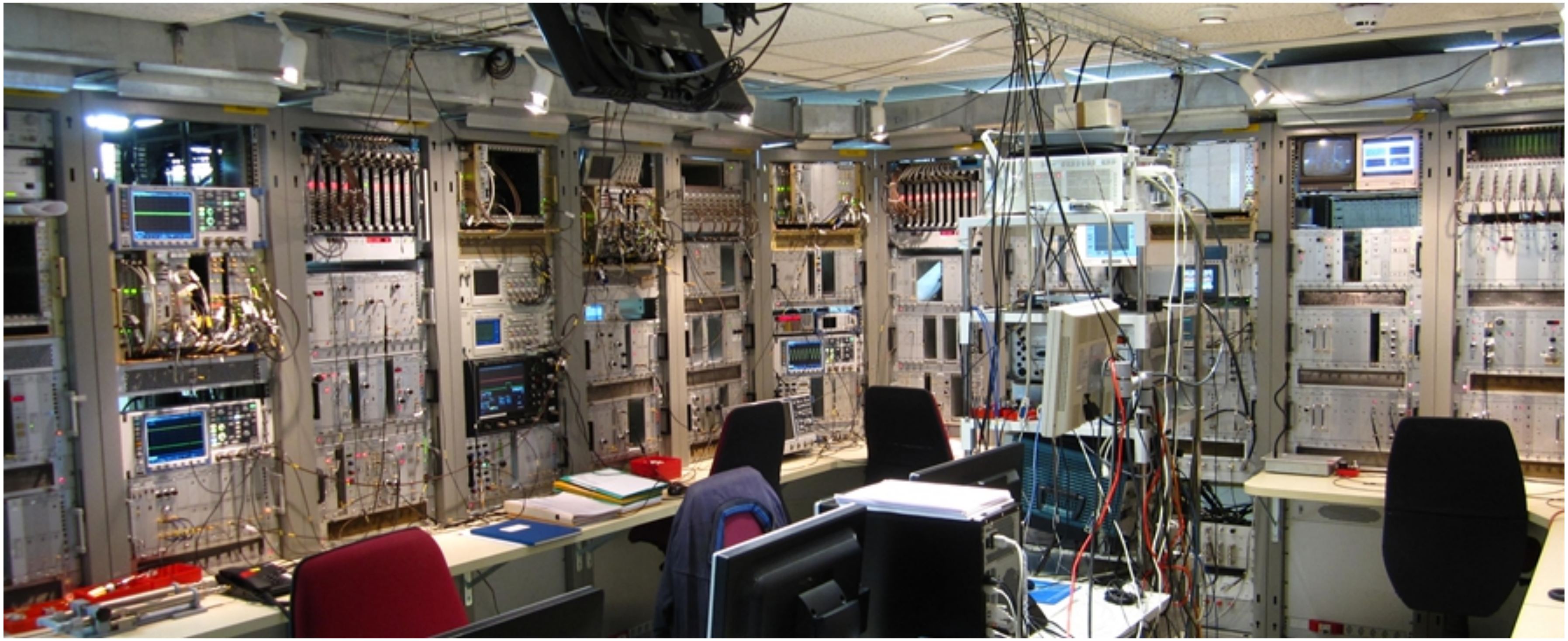


Fig9 - Current SPS Beam Control Systems

SPS LLRF Upgrade

Current system :

- NIM, Custom 6U Europa crate, VME
- Mostly analog
- Some designs from 1970s
- Only electronics for 4 cavities at 200MHz
  - (6 cavities installed after LS2)
- Lack of control
  - No cycle-cycle settings (PPM)
  - No remote control, no built-in diagnostic
  - Very time-consuming setting-up

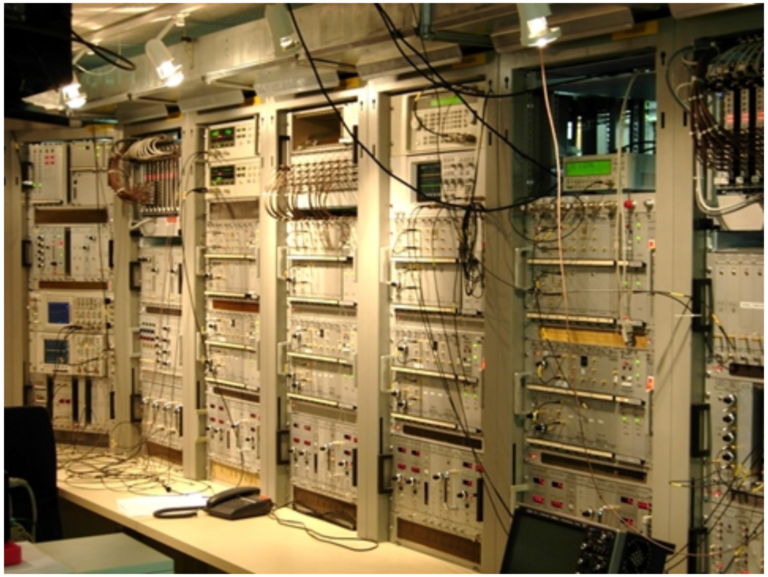


Fig10 - Current SPS 200MHz RF feedbacks

Upgrade foreseen in LS2 (2019-2020)

- Beam loading compensation MUST be improved to cope with 2x I_{BEAM} (HiLumi LHC)
- Bunch per Bunch Beam Phase & Radial position measurement → **5-10GSPS**
- Fixed-frequency acceleration (FFA) for ion acceleration → **FPGA**
- Fixed-frequency sampling clock (lower noise) → **COTS**
- Deterministic serial link for RF frequency distribution → **White-Rabbit**
- Momentum slip-stacking for 50ns ion bunch spacing, → **SoC (FPGA+ARM, eg: ZYNQ)**

SPS LLRF Architecture

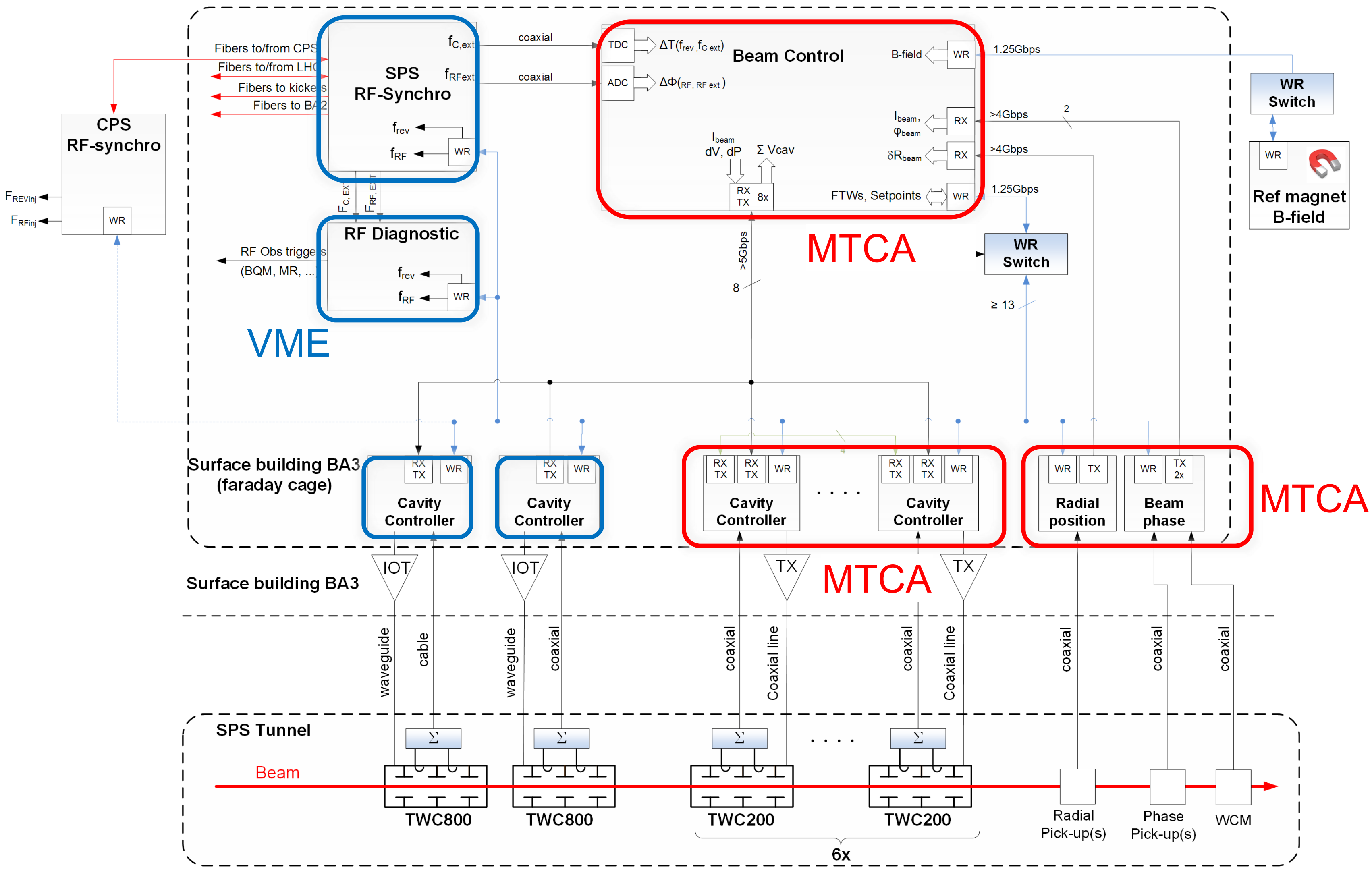
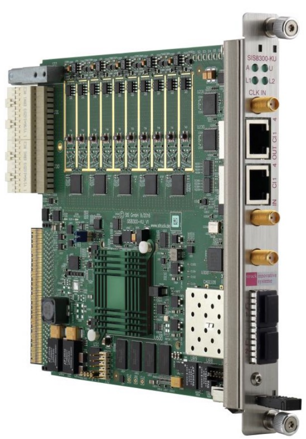


Fig11 – SPS LLRF Architecture

SPS LLRF 200MHz cavity Controller

DS8VM1 (Desy/Struck)



SIS8300-KU (Desy/Struck)

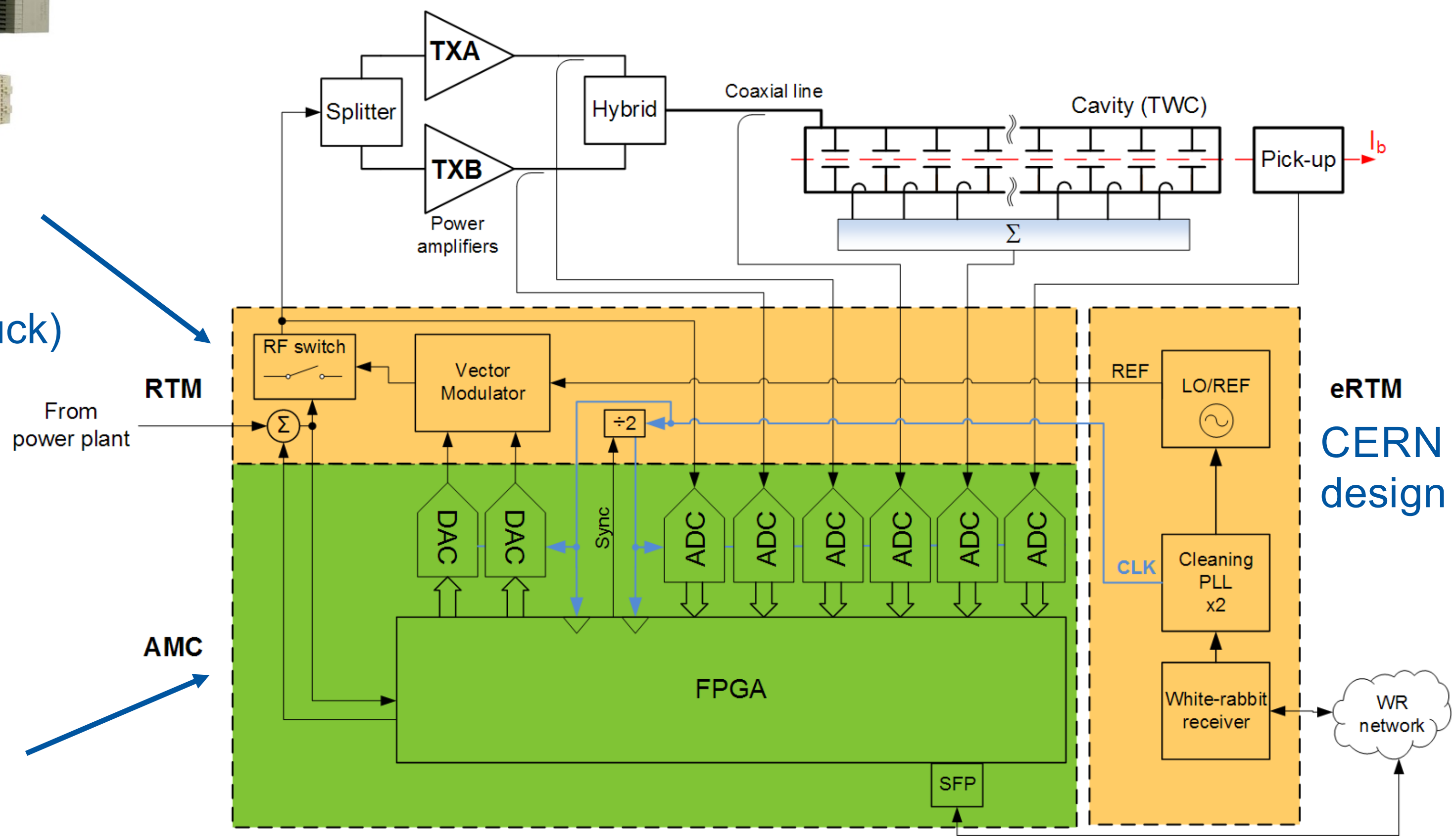
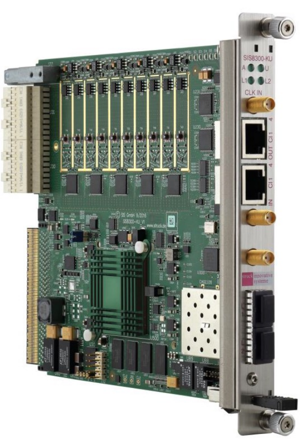


Fig12 – SPS 200MHz Cavity Controller (Direct sampling)

SPS LLRF 200MHz cavity Controller

DS8VM1
(Desy/Struck)



SIS8300-KU
(Desy/Struck)

Polar loop:
- TX noise
- Open loop phase
- Gain linearity

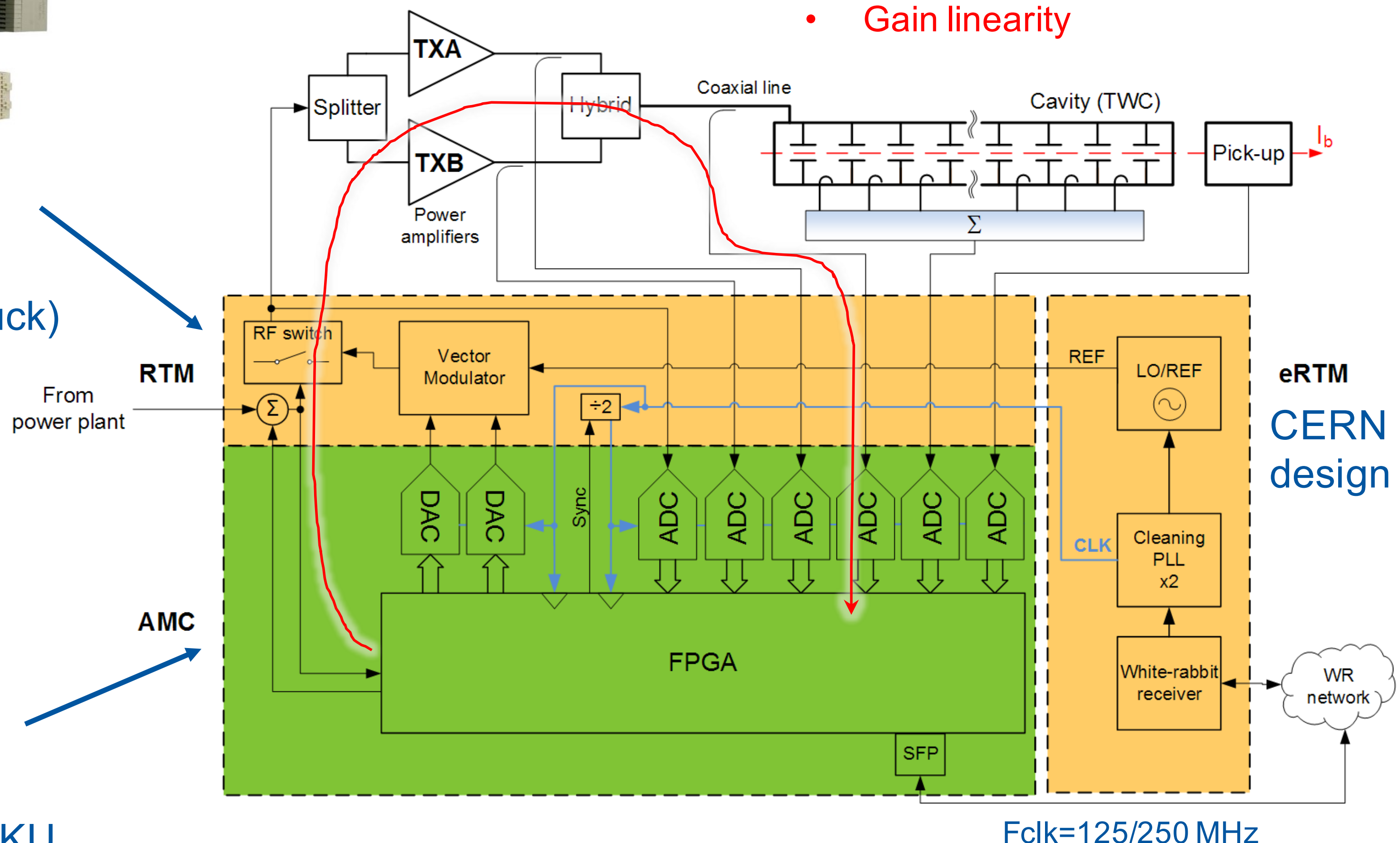


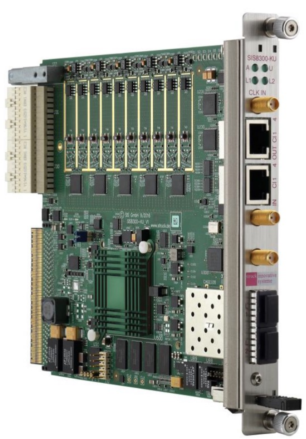
Fig13 – SPS 200MHz Cavity Controller (Direct sampling)

SPS LLRF 200MHz cavity Controller

RF Feedback

- IQ feedback
- Transient beam loading (Frev)
- Impedance reduction at synchrotron sidebands (fs, 2·fs)

DS8VM1 (Desy/Struck)



SIS8300-KU (Desy/Struck)

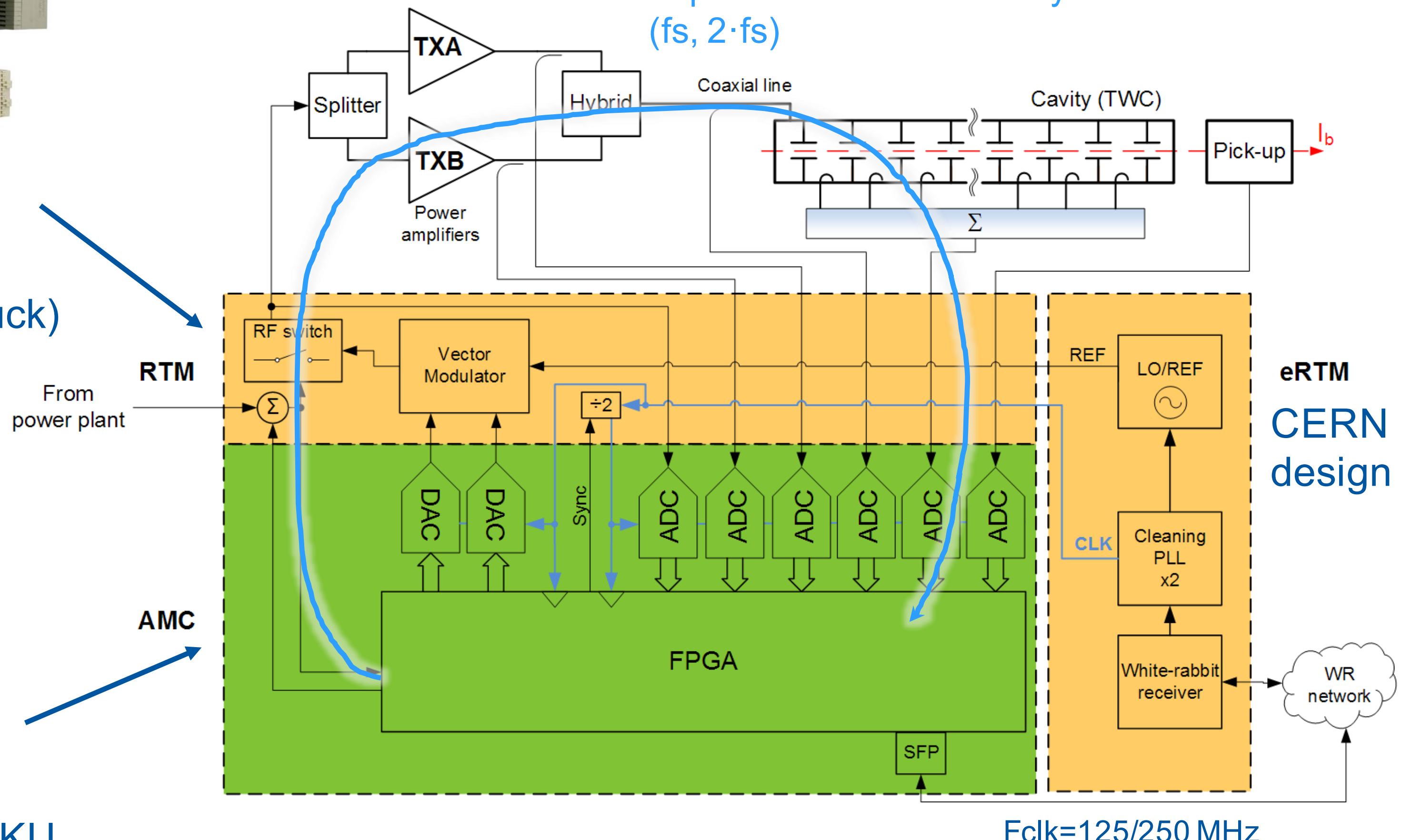


Fig14 – SPS 200MHz Cavity Controller (Direct sampling)

SPS LLRF Clock Generation/Distribution

Fixed-frequency sampling

- Big paradigm change for CERN synchrotrons
- Simplify clocking scheme
- Better noise performance (clock)
- Higher complexity in signal processing for bunch synchronous processing

White-rabbit support

- Reconstruction of sampling clock from White-Rabbit
- Aim for <130dBc/Hz (from 100Hz offset range)
- Scalable system

LLRF Backplane (Desy) compatible

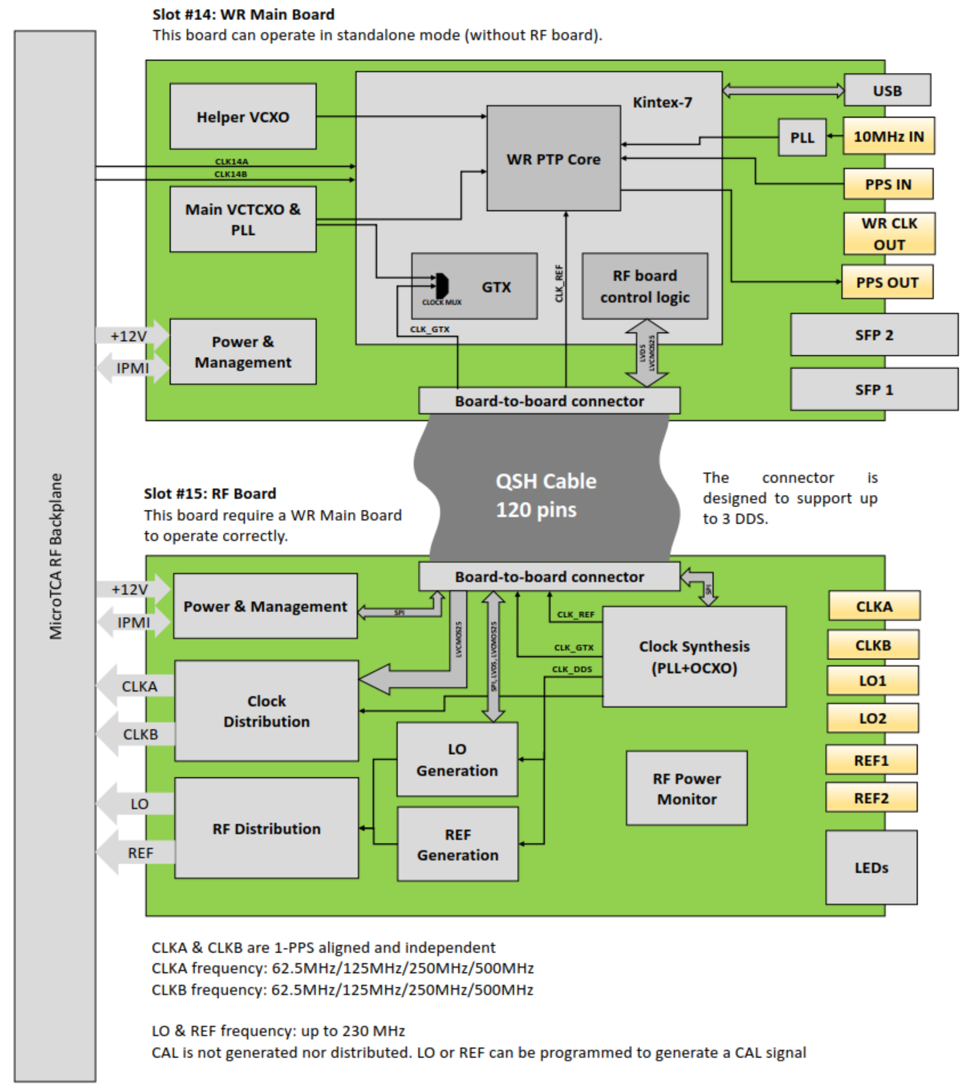


Fig15: eRTM for SPS LLRF (Courtesy Mattia Rizzi)

SPS LLRF Beam control

Beam based loops

- B-field reception (White-rabbit)
- RF freq calculation (FPU)
- RF freq distribution (White-rabbit)
- Synchro Loop
- Phase loop
- Radial loop
- Cogging /Rephasing (extr. to LHC)
- Slip stacking (Ions 50ns)

AMC:

- FMC Carrier, 2x FMC (HPC)
- SoC (FPGA+ARM)
- White-Rabbit (2x)
- MTCA.4

RTM :

- 4x SFP+, 3xQSFP+
- MTCA.4.1 (optional)

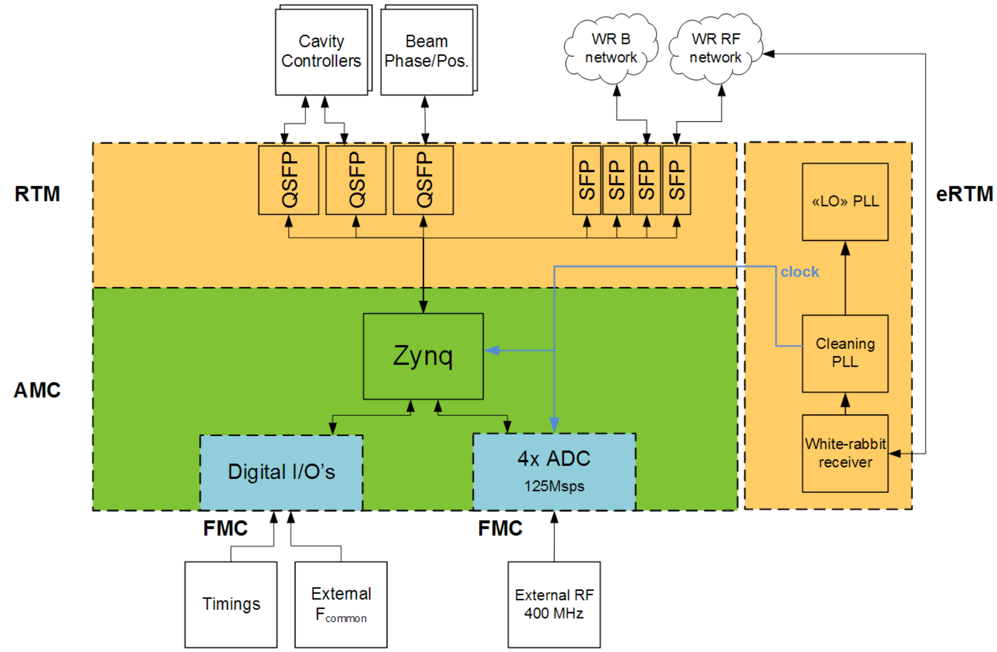


Fig16: Beam control in MTCA.4 (Courtesy A. Spierer)

SPS LLRF Beam Phase, Radial Position, Intensity

- Signals received from beam position monitors typically cover several GHz
- SPS RF frequency: 200 MHz → bunch spacing 5 ns
- Direct sampling of beam signals with fixed sampling clock at >> GSPS
- Beam synchronous feature extraction in digital
- Beam instantaneous frequencies received via WR link
- System clocks are deterministic for every cycle ("absolute time", based on WR)

Hardware Parameters:

- Input channels ≥2
- Sampling rate ≥ 5 GSPS
- Analog BW ≥ 1 GHz
- Vertical Res. ≥ 8 bits
- Data output 200 MSPS
- Clocks derived from WR (125 MHz)

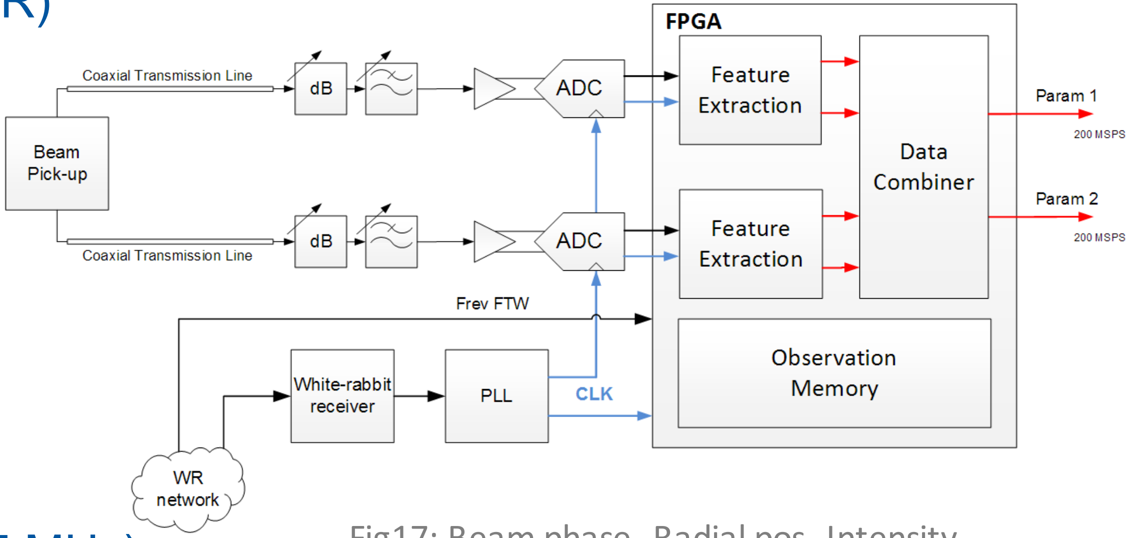


Fig17: Beam phase, Radial pos, Intensity (Courtesy G. Kotzian)

SPS LLRF MTCA.4.1 Equipment

MTCA 9U Crate

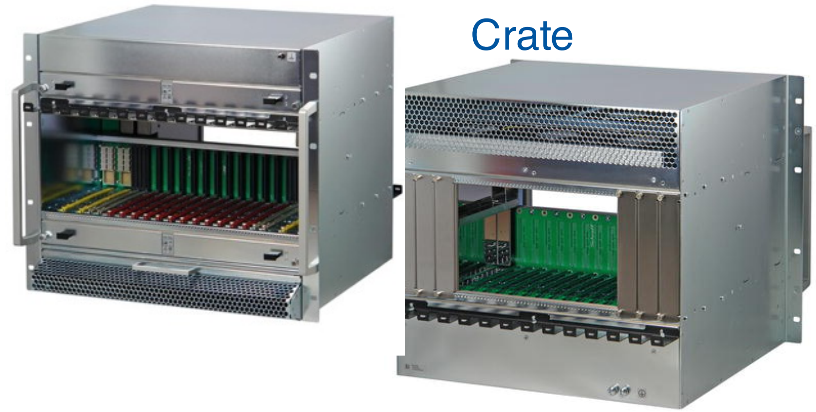


Fig18: MCTA.4.1, 19'', 9U (Pentair GmbH, N.A.T. GmbH)

MCH (crate controller)

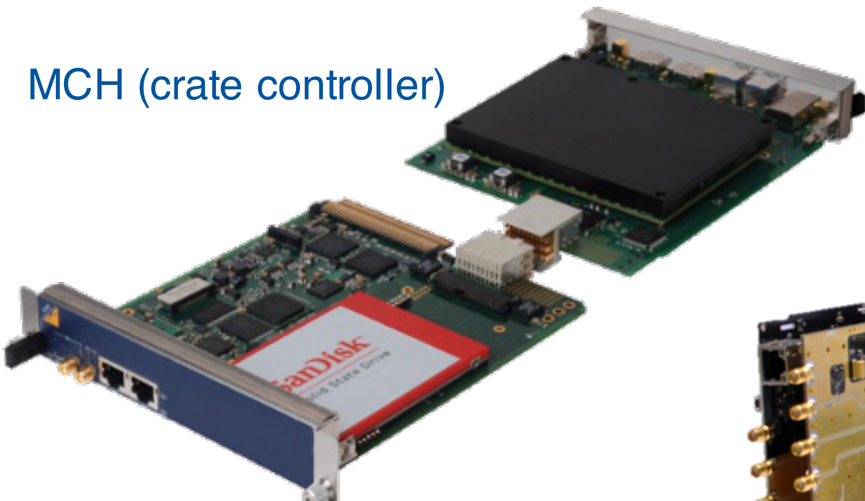


Fig19: MCH (N.A.T. GmbH)

RF backplane

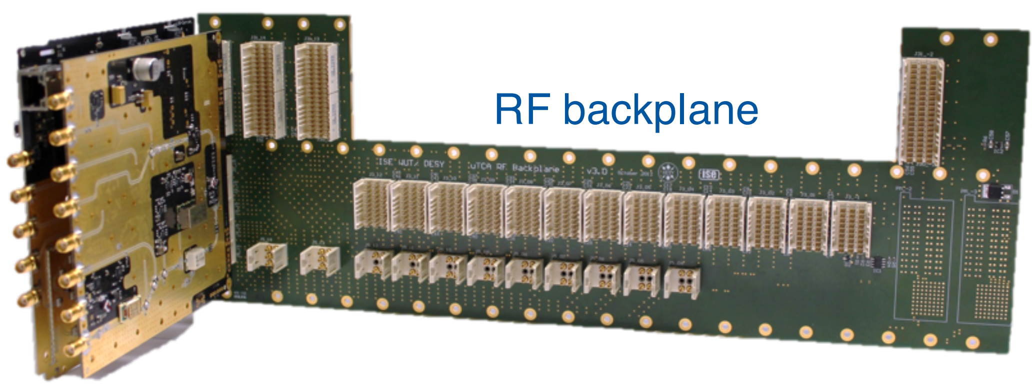


Fig20: NAT-LLRF-Backplane (DESY, N.A.T. GmbH)

CERN SPS-LIU Schedule

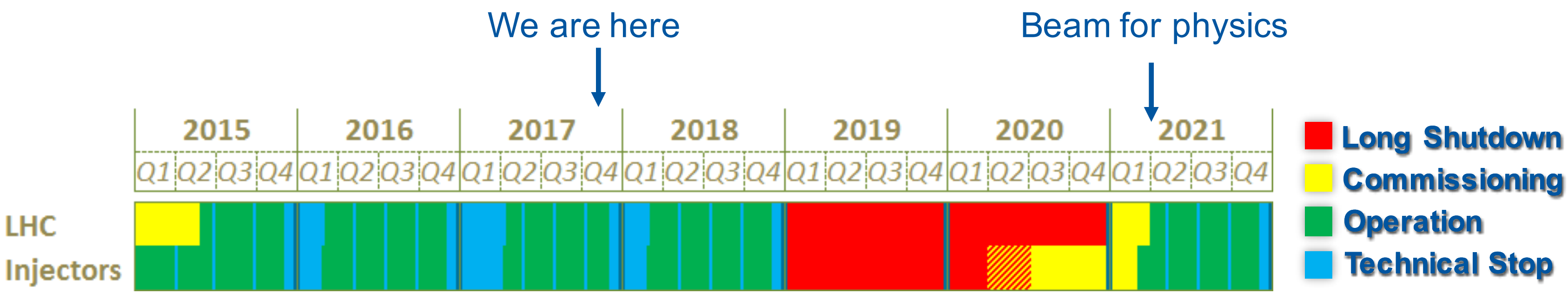
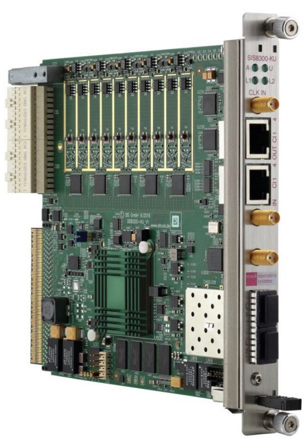


Fig21: SPS-LIU Master plan

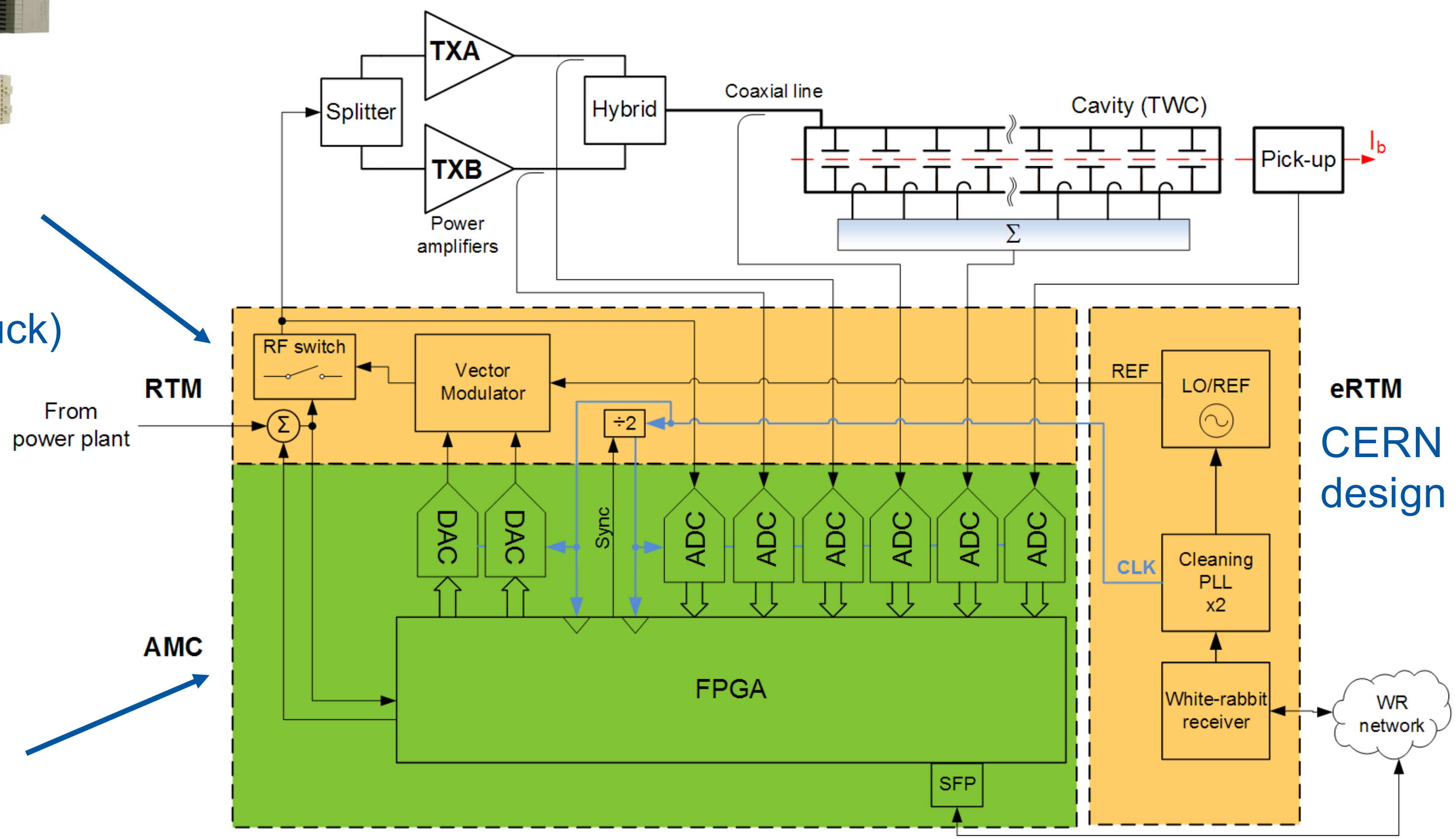
- Q1 2018: MTCA Cavity controller tests on 200MHz cavity
- Q2/Q3 2018: Prototype HW for Beam control (FMC carrier)
  MTCA HW for Beam phase/Intensity measurement
- End 2018: CERN Accelerator complex stop → Long Shutdown 2
- 2019-2020 : LLRF Upgrade
- Q4 2020 : LLRF commissioning
- Q1/Q2 2021: Beam commissioning & Run 3
  0.55A DC → 1.1A DC (HiLumi LHC)

SPS LLRF 200MHz cavity Controller

DS8VM1
(Desy/Struck)



SIS8300-KU
(Desy/Struck)



CERN design

Fclk=125/250 MHz

Fig22 – SPS 200MHz Cavity Controller (Direct sampling)

SPS LLRF 200MHz cavity Controller

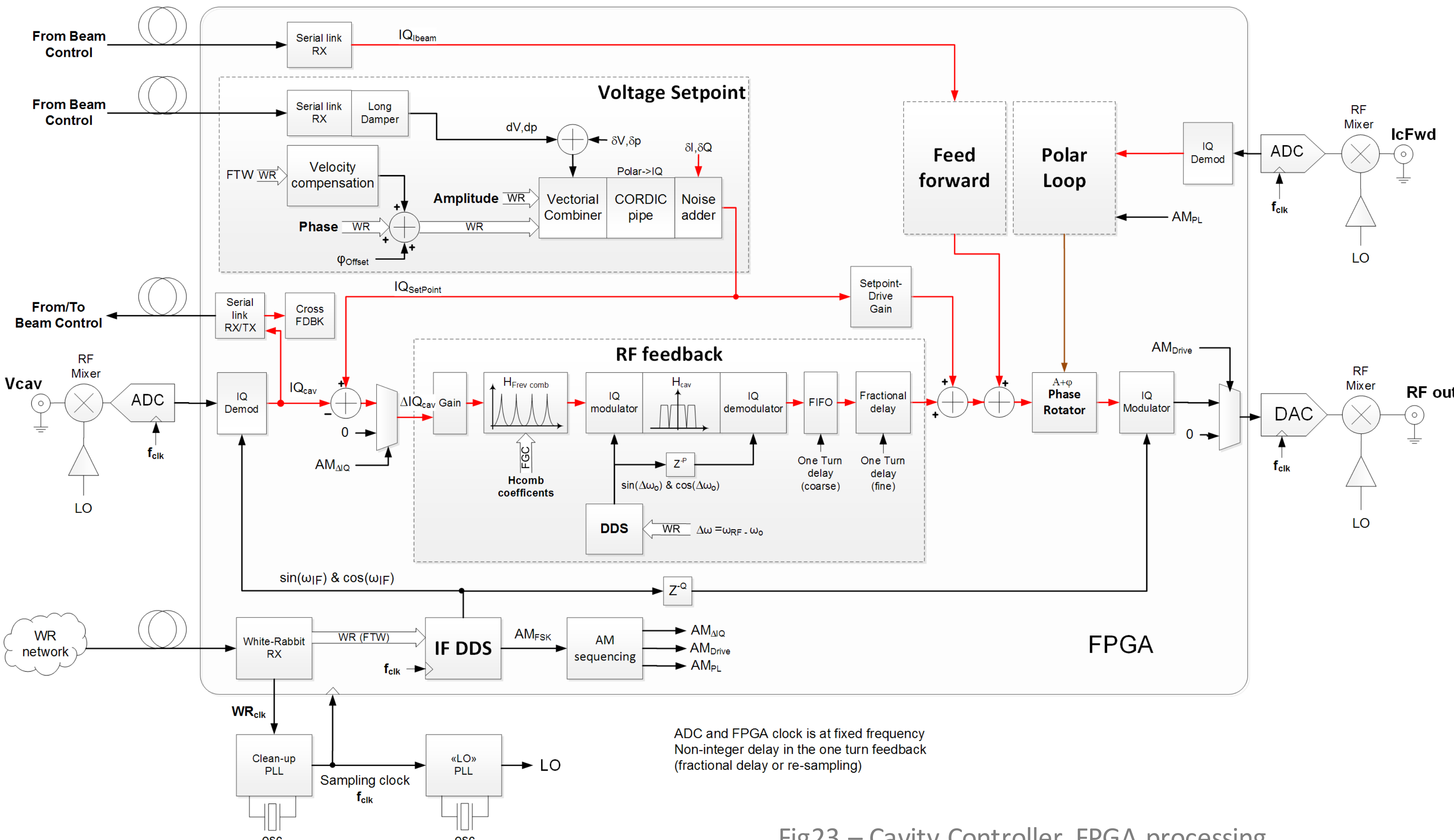


Fig23 – Cavity Controller, FPGA processing

SPS LLRF 200MHz cavity Controller

One Turn delay feedback

$$H_{comb} = G\frac{b_0 + b_1 \cdot Z^{-N}}{1 + a_0 \cdot Z^{-N} + a_1 \cdot Z^{-2N}}$$

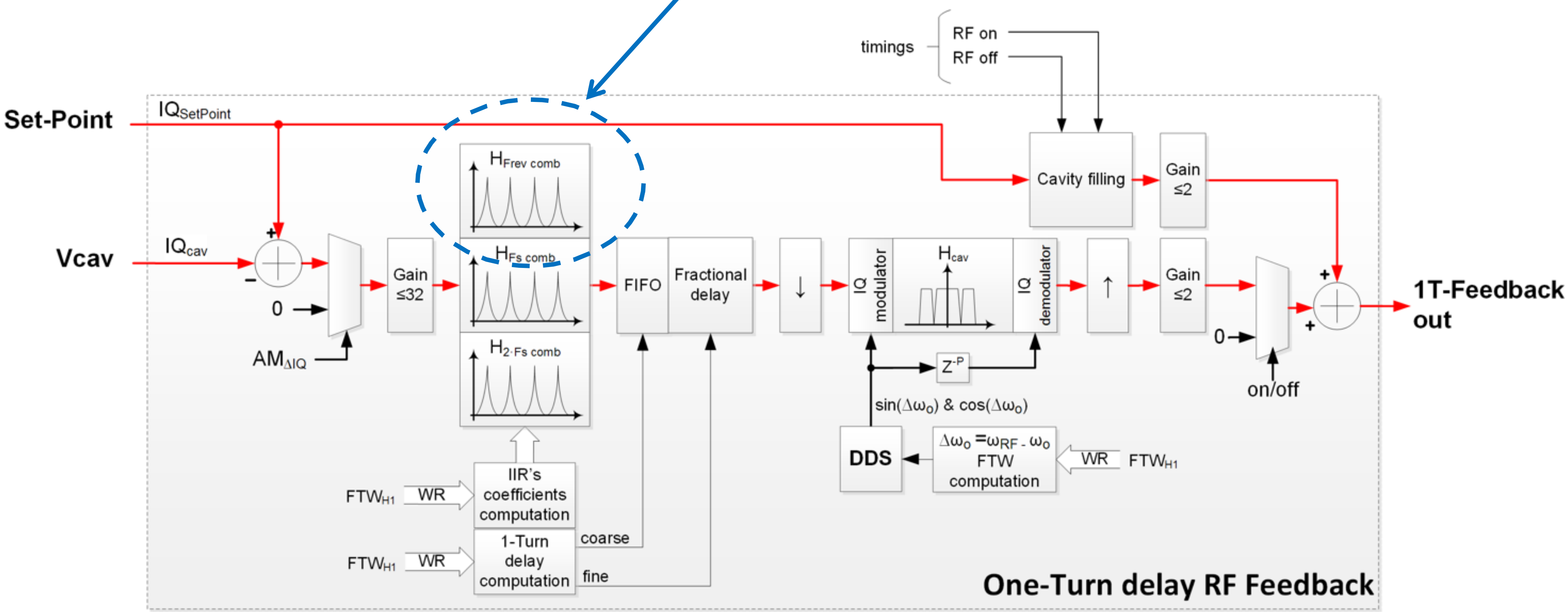


Fig24 – One Turn Delay feedback with triple comb

SPS LLRF 200MHz cavity Controller

MIMO feedback

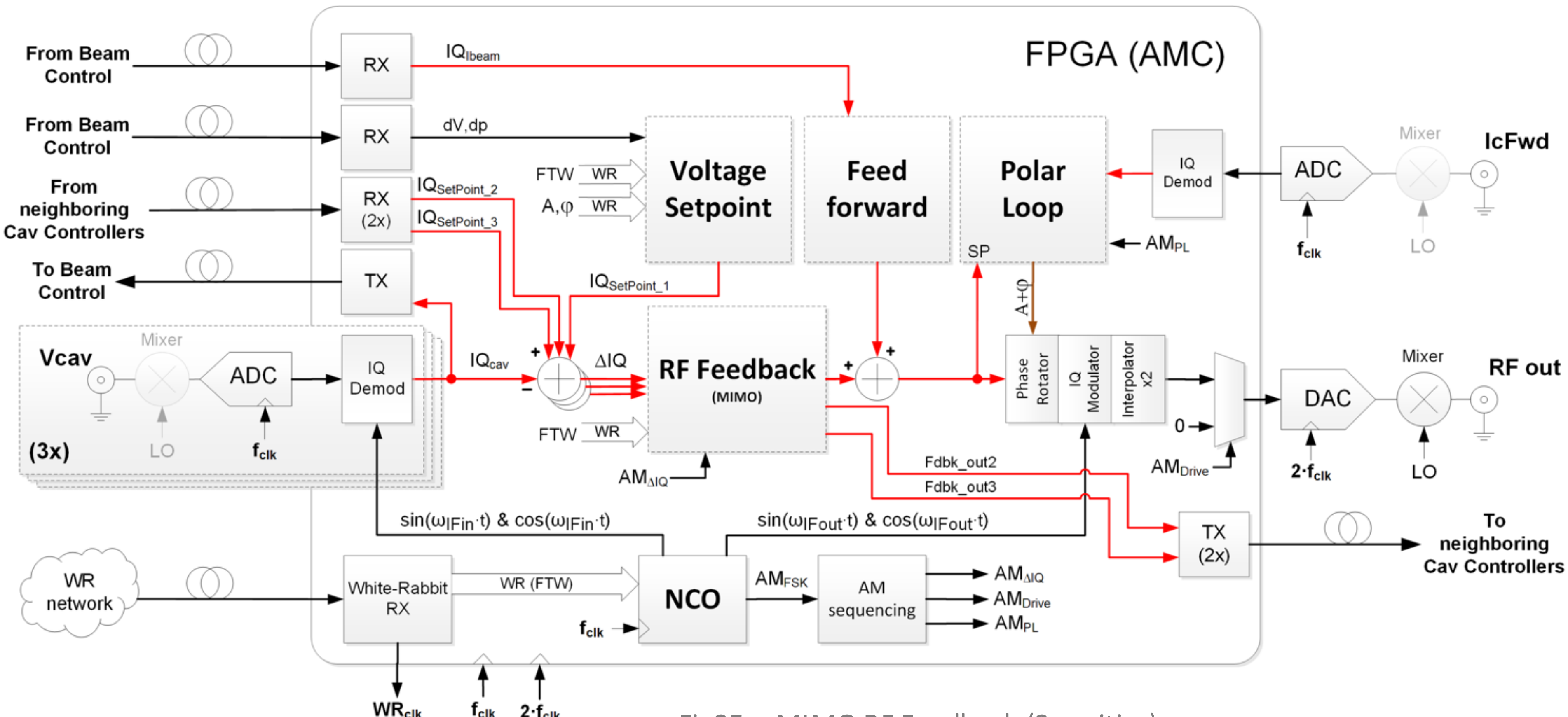


Fig25 – MIMO RF Feedback (3 cavities)

SPS LLRF 200MHz cavity Controller

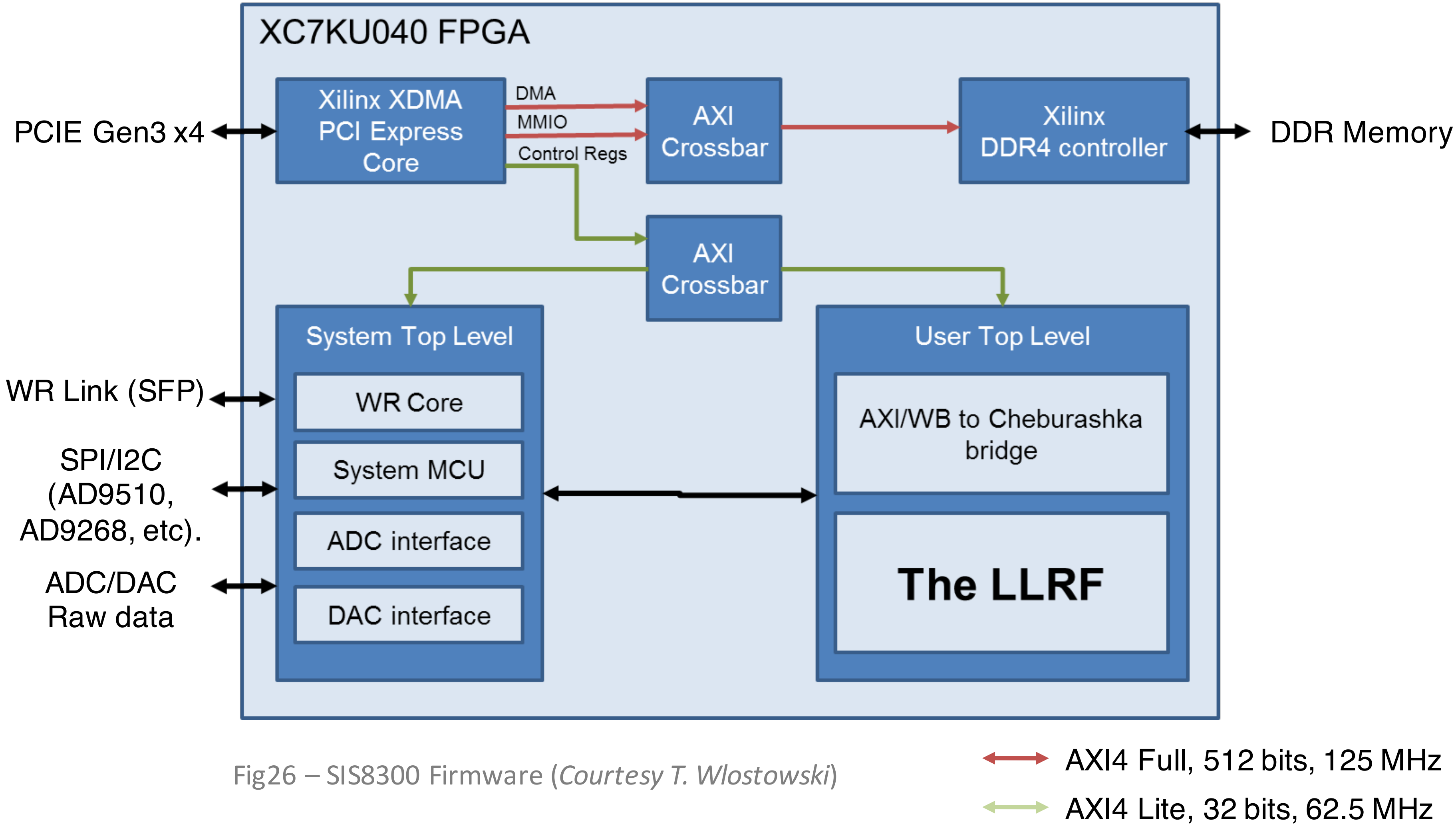
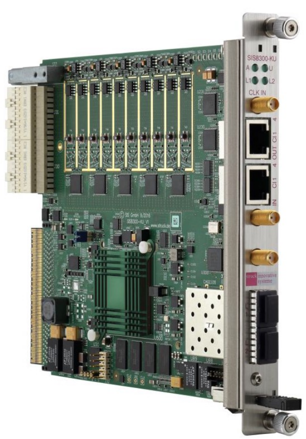


Fig26 – SIS8300 Firmware (*Courtesy T. Wlostowski*)

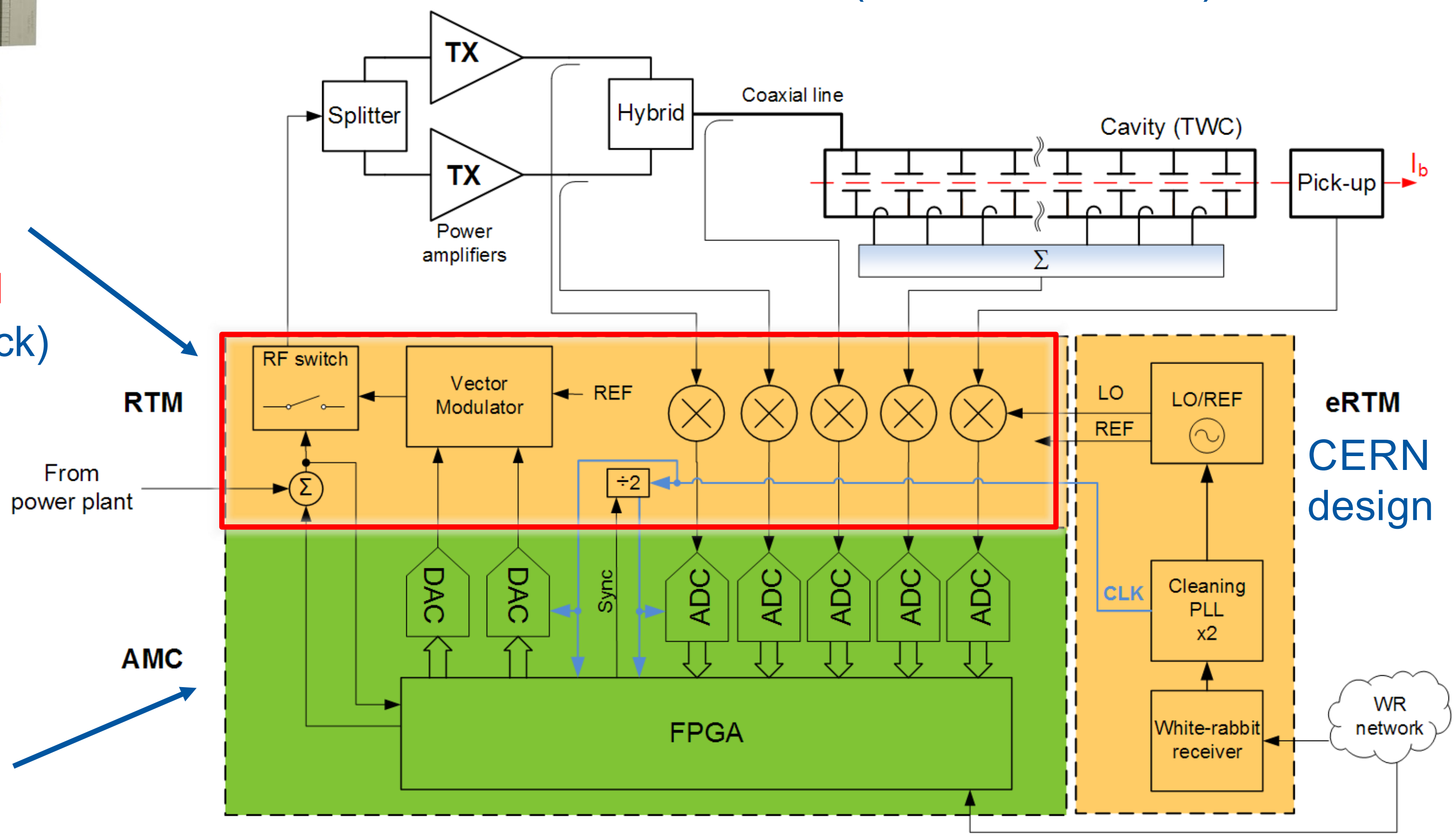
SPS LLRF 200MHz cavity Controller

IF processing to be studied (Down-converter)

DWC8VM1 (Desy/Struck)



SIS8300-KU (Desy/Struck)



Fclk=125/250 MHz

Fig27 – SPS 200MHz Cavity Controller (Down converter)

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[1] J. Coupard & al. LHC INJECTOR UPGRADE – Technical Design Report – Volume I: Protons, CERN-ACC-2014-0337, 15.12.2017

[2] J. Coupard & al. LHC INJECTOR UPGRADE – Technical Design Report – Volume II: Ions, CERN-ACC-2016-0041, 01.04.2016

[3] T. Argyropoulos, MOMENTUM SLIP-STACKING OF THE I-LHC BEAM IN THE SPS, talk at LIU-SPS BD WG, CERN, 27.02.2014

[4] G. Hagmann & al., SPS LLRF Upgrade project, LLRF Workshop 2017, Barcelona, Spain, Poster P-9