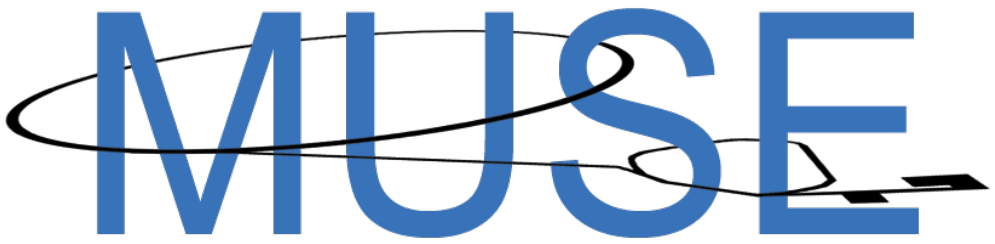


Mu2e Calorimeter electronics

E. Pedreschi

INFN Pisa

MUSE Network General Meeting
October 22th 2018

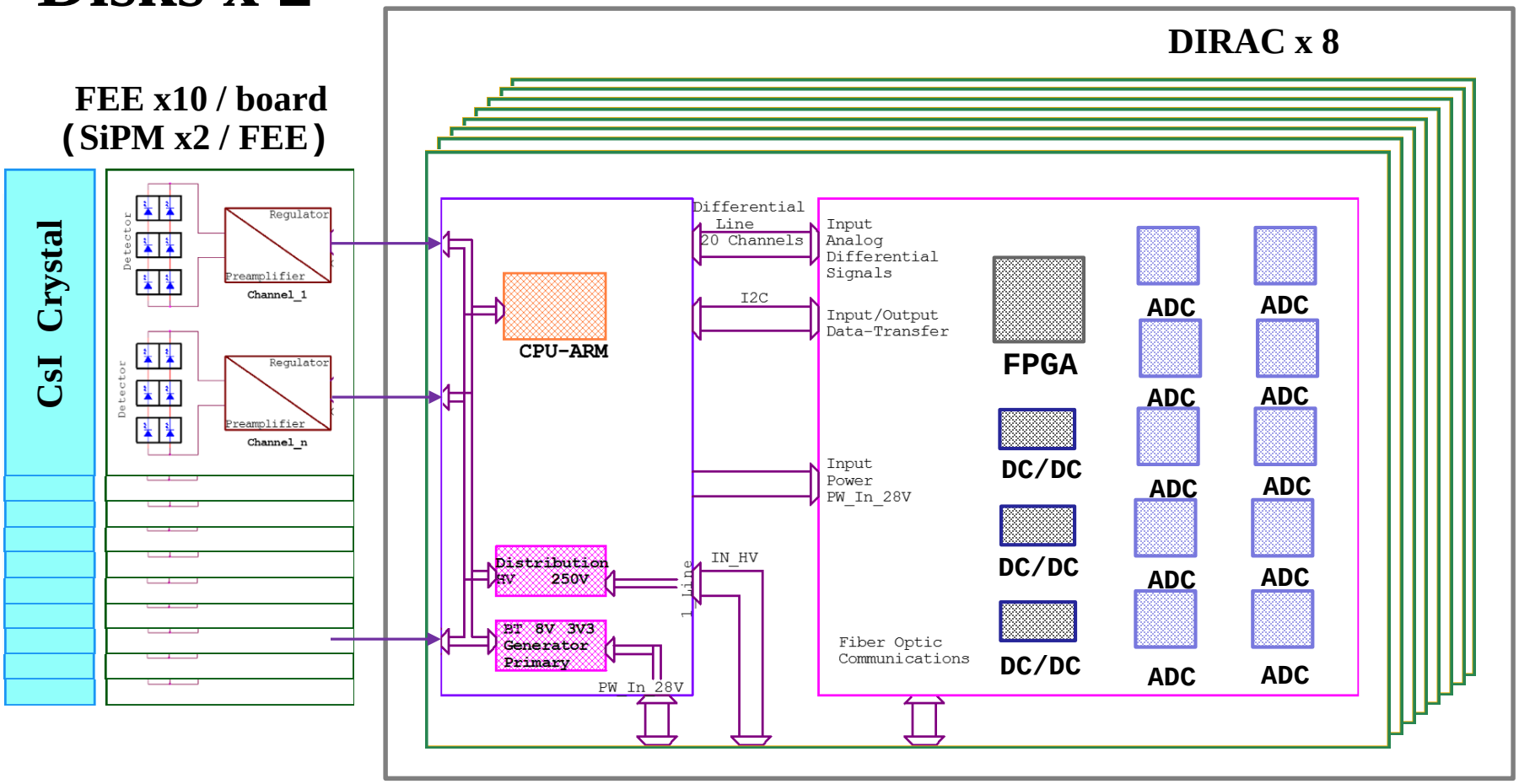
Outline

- Mu2e Calorimeter Electronics
- Front End Electronics - FEE
- DIgitizer ReAdout Controller - DIRAC
- Proto-Slice Test
- DIRAC radiation test.

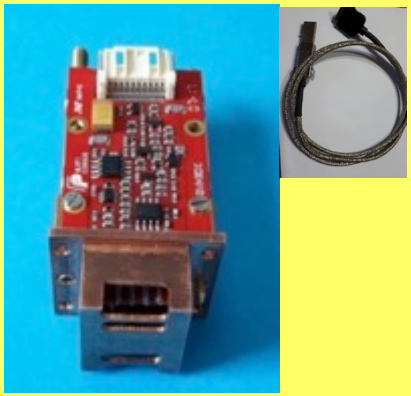
Mu2e Calorimeter Electronics

Disks x 2

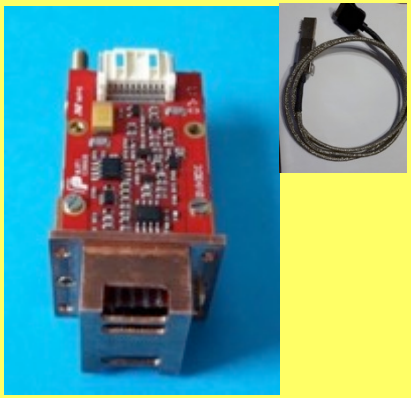
Crate x 10



Mu2e Calorimeter Elecronics



X20



X8

X20 (10 + 10)

Some numbers

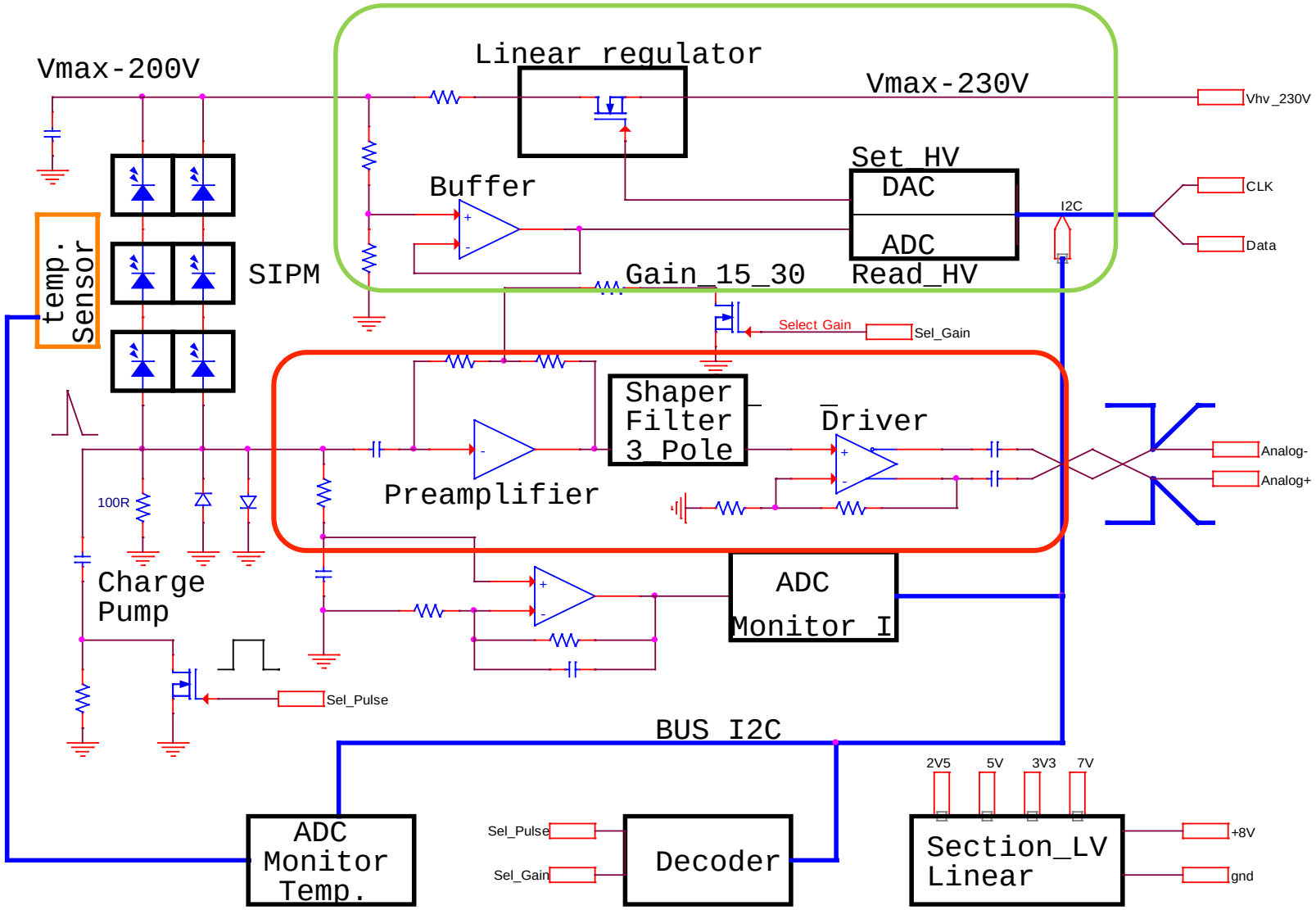
- 2 disks
- 680 crystals/disk
- 2 SiPM/crystal
- 2 x 2 x 680 = 2720 electronic channels
- 20 channels/ digitizer board (DIRAC)
- 2720/20 = 136
- Each crate hosts 8 DIRAC.

We have to produce:

- 2720 FEE chip cards
- 2720 custom cables
- 136 digitizers & readout boards (DIRAC) + mezzanines
- 20 crates

Front End Electronics - FEE

FEE block diagram



EQUIVALENT CIRCUIT

Regulator specification

Vin max DC	200V
Current limit	2mA
Dynamic regulation	5V÷200V
Setting time	100us
Ramp-up programmable	1ms÷100ms
Ripple (measured)	3 mV (Vpp)
Power dissipation (min, no load)	50 mW
Power dissipation (Max, with load)	350 mW
Operating temperature	- 40ºC÷+50 ºC
Monitor current detector	50uA÷2mA
Remote control via Dirac interface	I2C
GND insulated from earth	Ceq max 3pf

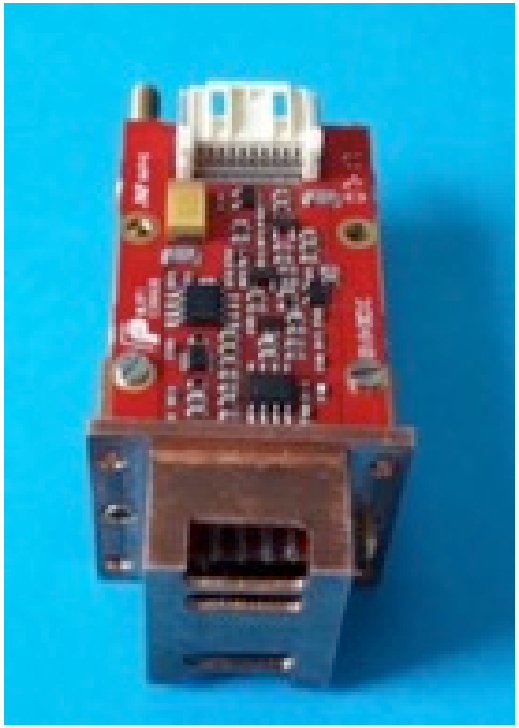
Amplifier specification

- Gain Vout/Vin 2 steps remote control 15V÷30V
- Dynamic differential output +/-1V
- Preamplifier bandwidth 40Mhz
- Preamplifier Rise tim 10ns
- Output impedance 100 Ω
- Coupling output end source AC
- Noise, with source capacity 1pf 1nV√Hz
- Power dissipation 45mW
- Power supply +8V
- Semi-gaussian shaping filter 3 pole
- Rise Time after shaper 25ns
- Injection test pulse charging, fixed amplitude 400mV
- Input protection 10mJ

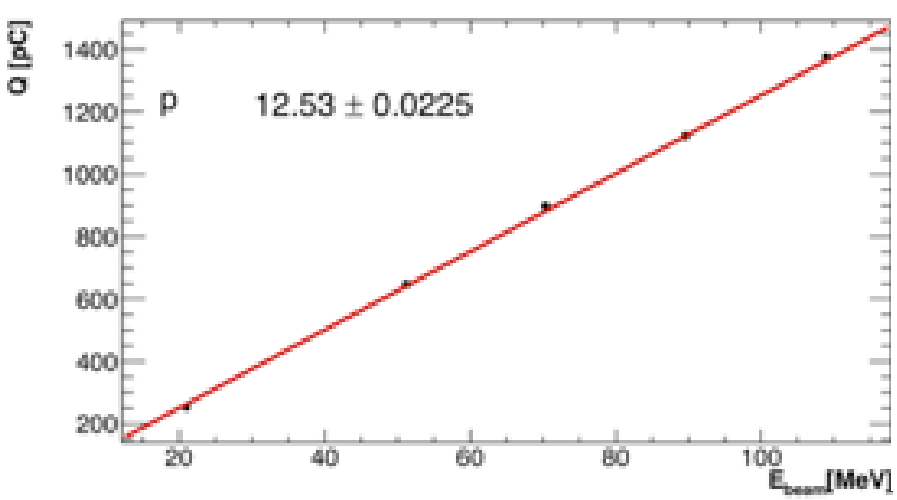
FEE (AMP-HV)

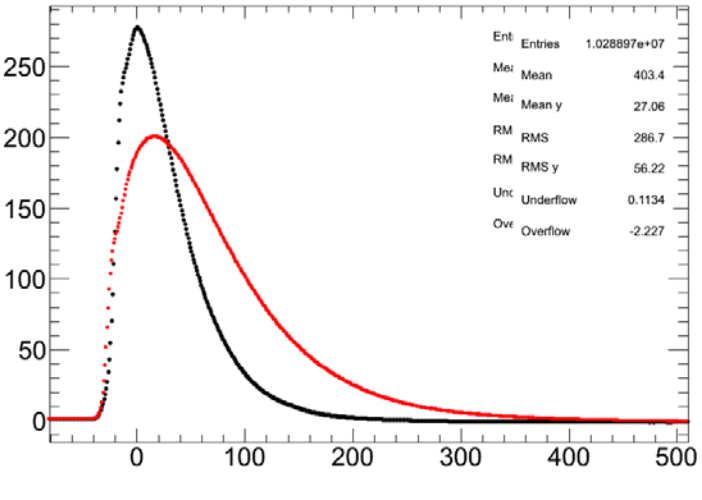
- AMP-HV is a custom 2-sides board
- Amplifier on A side, Local HV regulator on B-side
- It has a temperature sensor
- It provides Idark measurement, two gains' setting

➔ Differential signals are sent to Mezzanine Board (MB) and then to the DIRAC board



2 versions up to now … V1 had some linearity problems solved in V2
Modified shaping time in V2 to increase the leading edge time.
V3 is foreseen to strenghten radiation hardness of the board





DIgitizer ReAdout Controller
DIRAC

DIRAC requirements and specifications

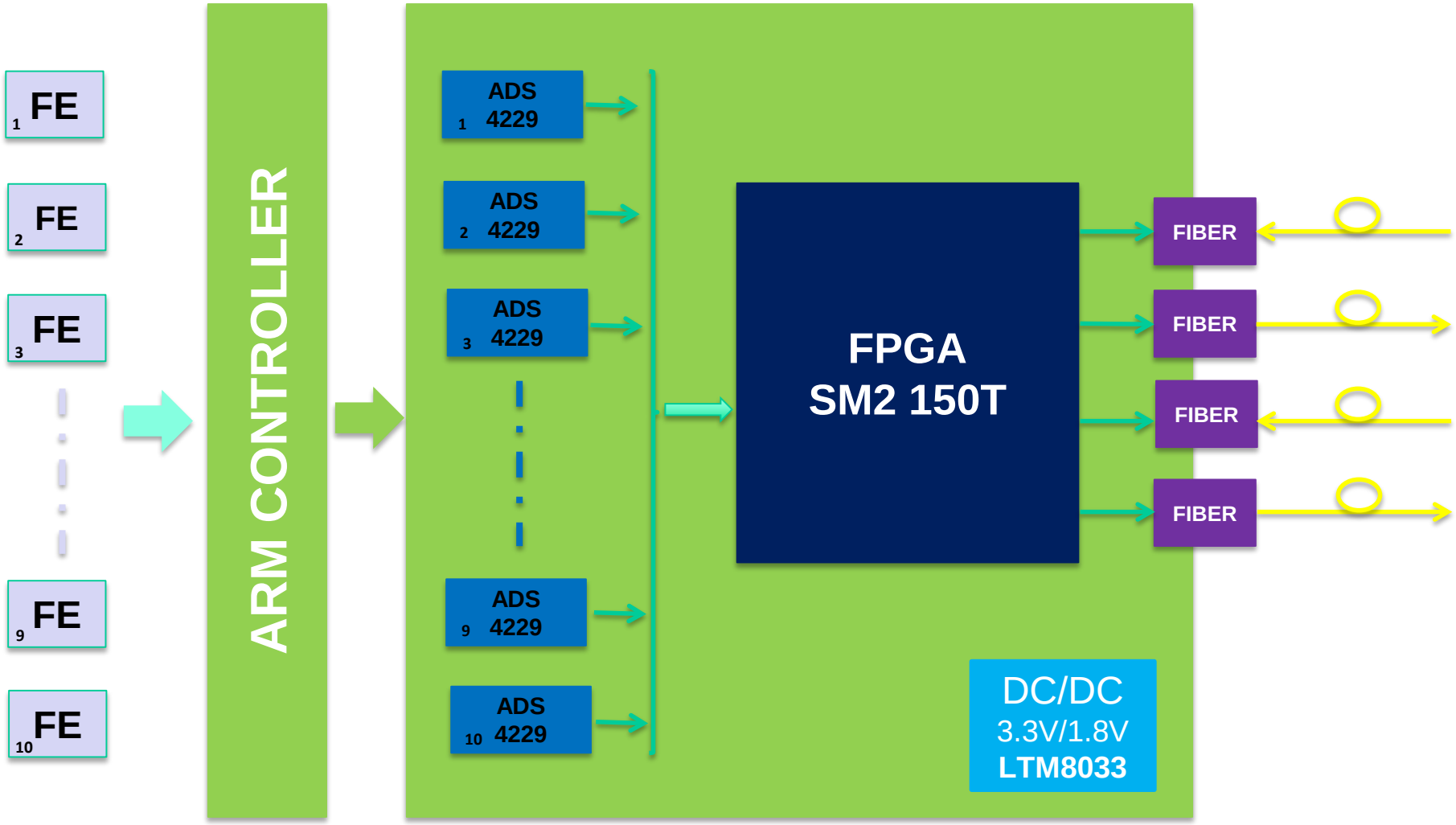
Requirements:

- Sample the SiPM signal (after FEE) to achieve a good energy resolution O (7-10%) and an optimal time resolution O(200 ps)
- Each crystal is readout through 2 SiPM → we need to digitize ~ 2700 channels
- Limit the number of pass through connectors

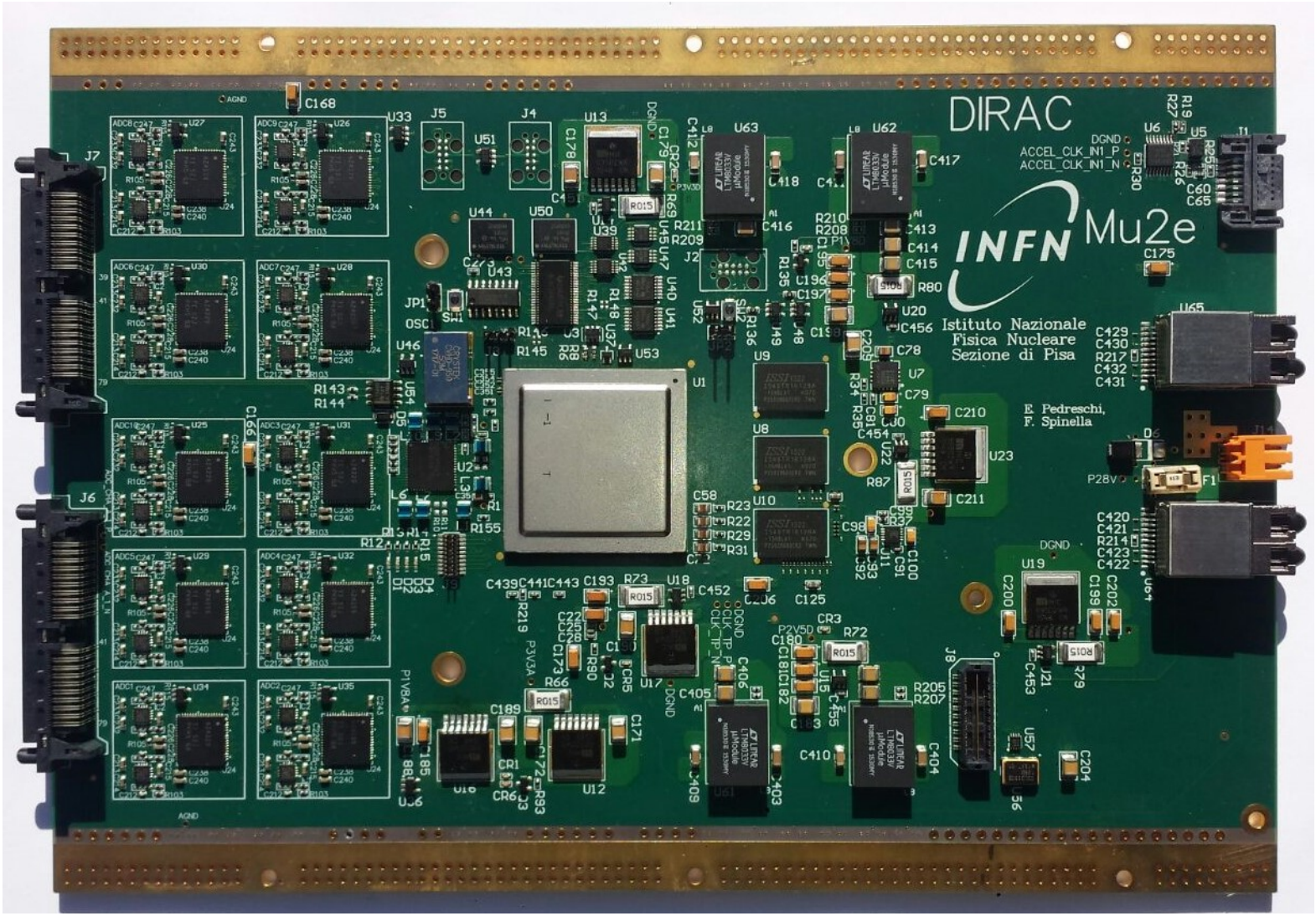
This translates to the following specifications:

1. Sample the signal with an ADC (200 Msamples @ 12 bits)
2. DIRAC is located inside the cryostat:
   - ✓ Stand a radiation environment of 0.2 krad/y of TID (Total Ionizing Dose).
   - ✓ Work in presence of high magnetic field (1T)
   - ✓ Low power
3. Host at least 20 channels/board (mechanical constrains & BW limit)
4. Have large reliability to allow to operate for 1 year w.o. interruption

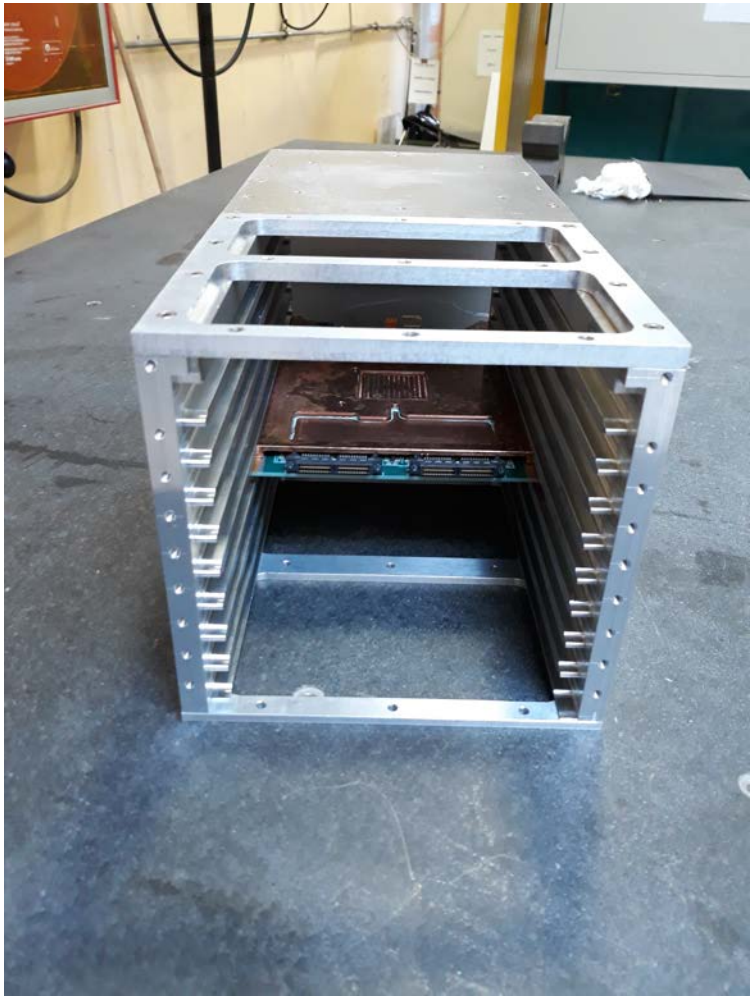
DIRAC Block Diagram

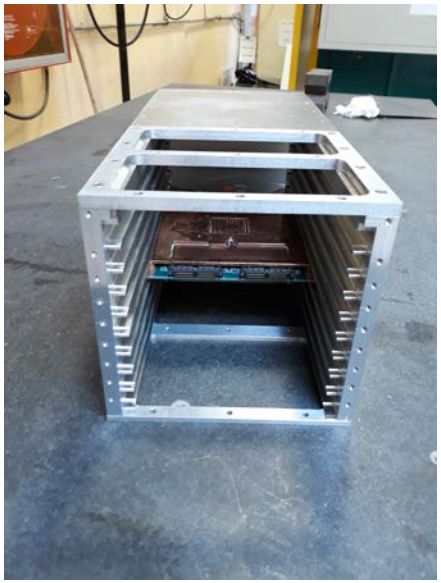


DIRAC V1

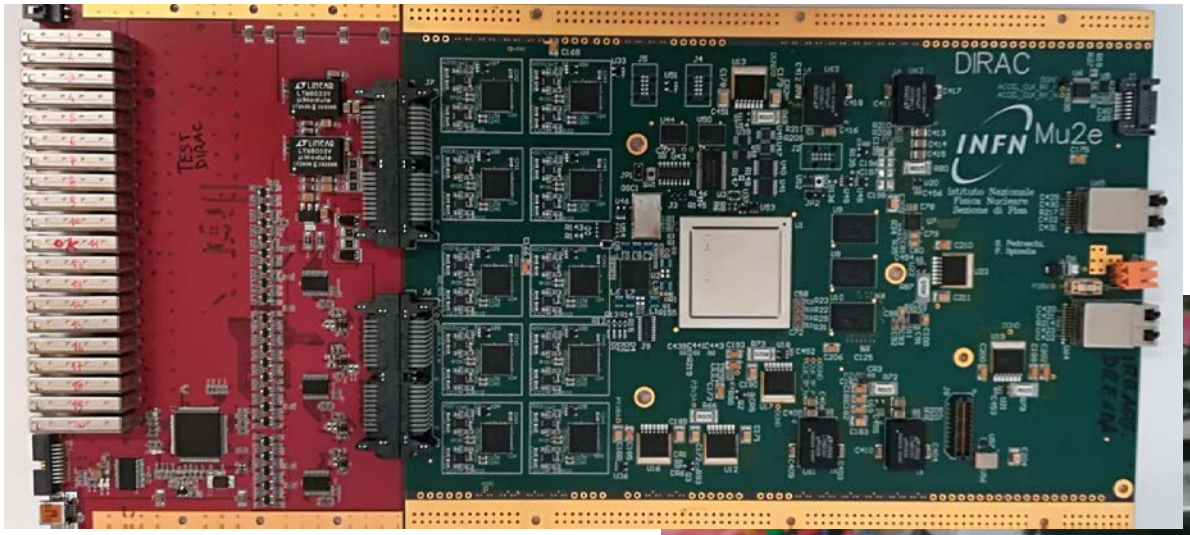

DIRAC
INFN Mu2e
Istituto Nazionale
Fisica Nucleare
Sezione di Pisa
E. Pedreschi,
F. Spinella
ACCEL_CLK_IN1_P
ACCEL_CLK_IN1_N
DGND
AGND
P28V
P3V3A
P2V5D

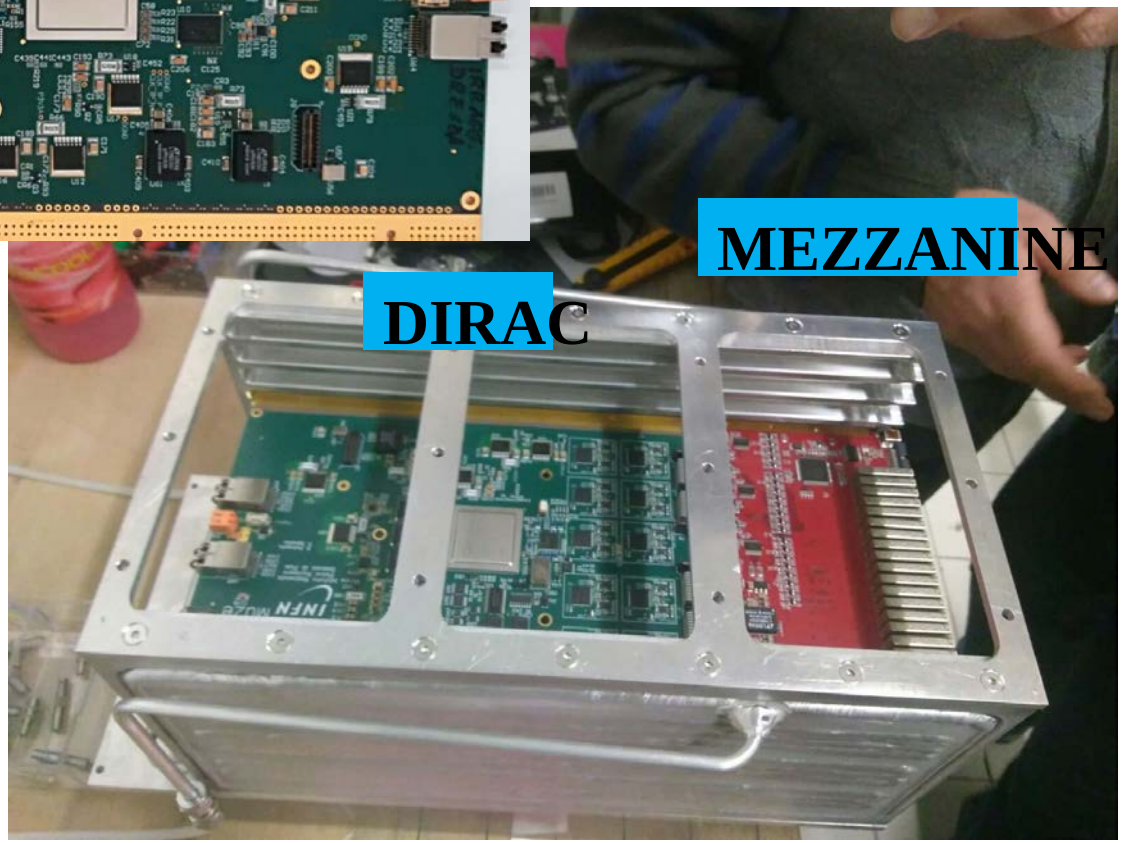
DIRAC V1 + Crate



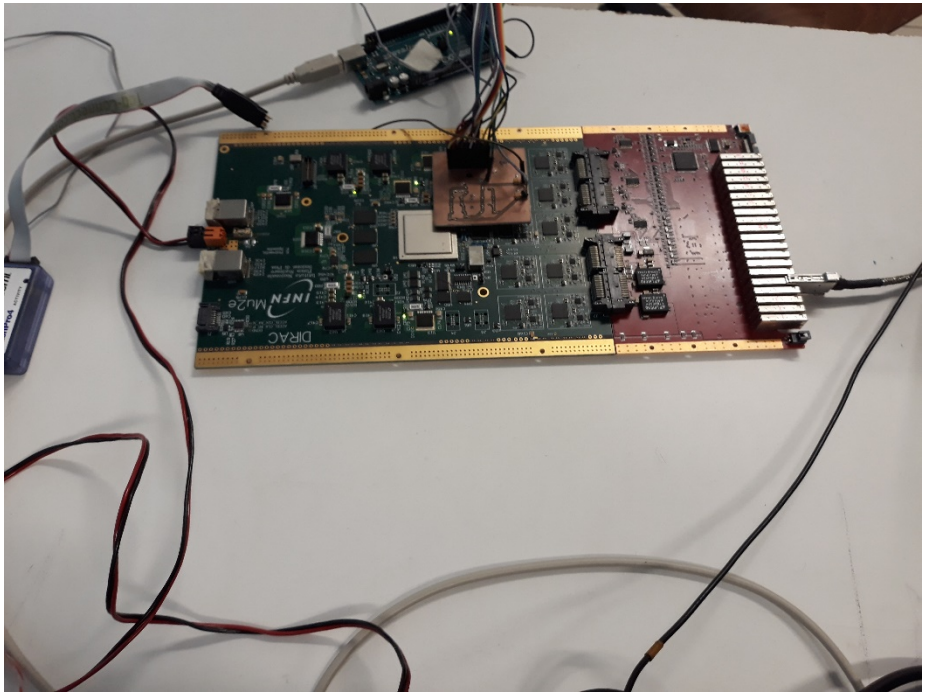


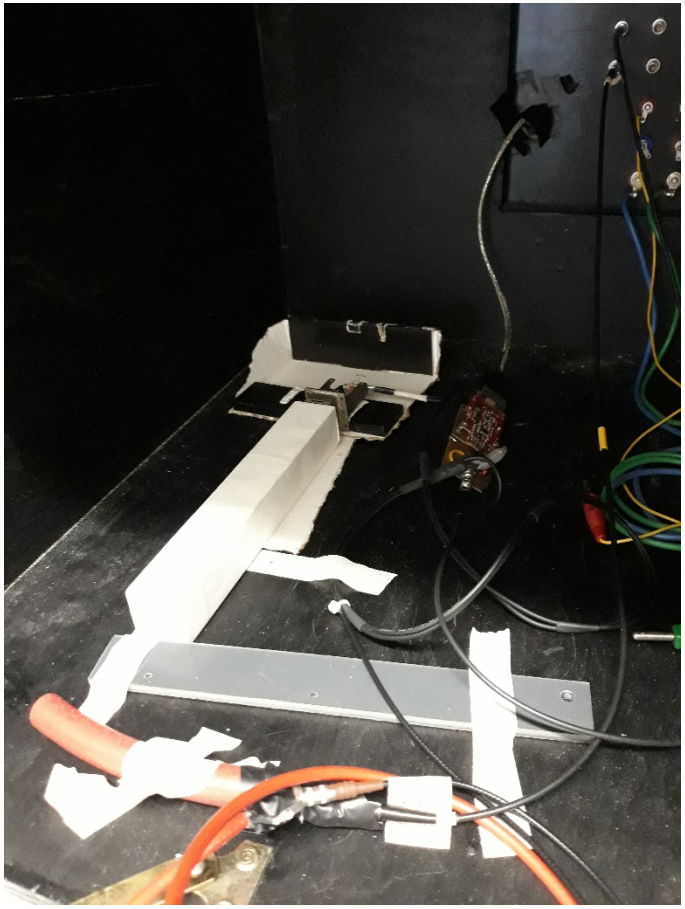
DIRAC V1 + Mezzanine + Crate



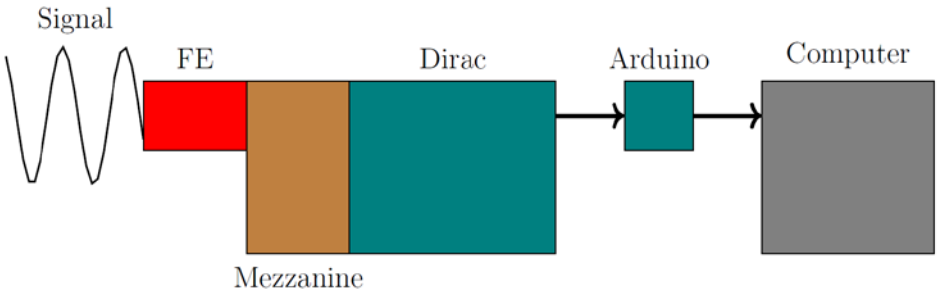


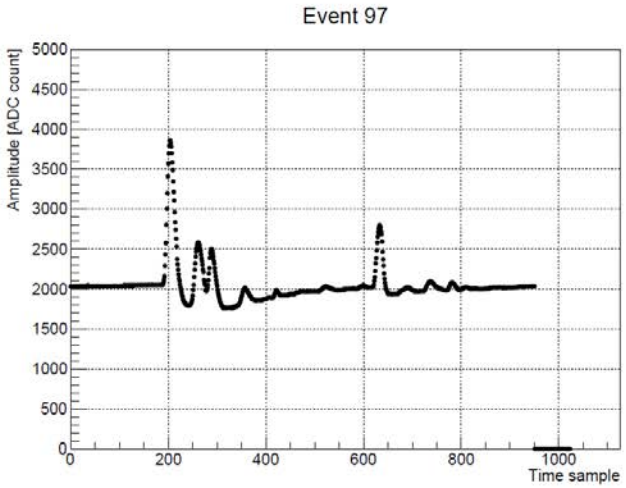
Proto Slice test: full chain, 1 channel





Proto Slice test: injected signal on FEE

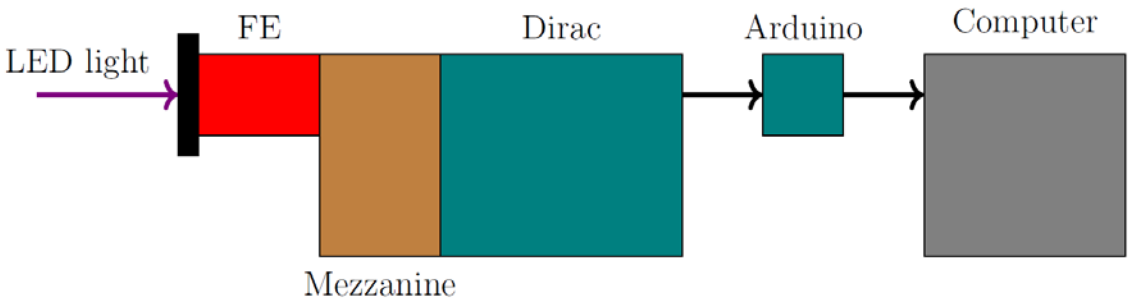


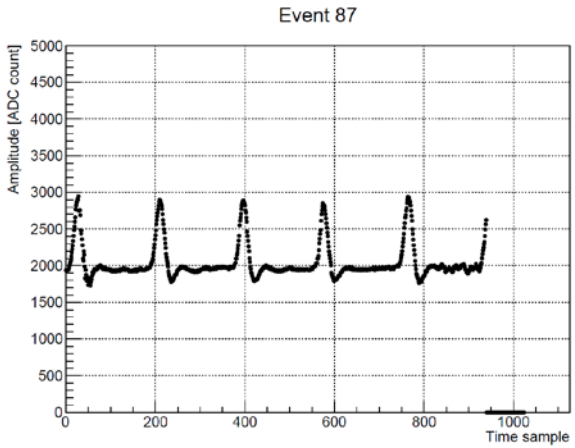


Electrical signal from Arbitrary Function Generator

Readout signal 200 MHz 12 bit

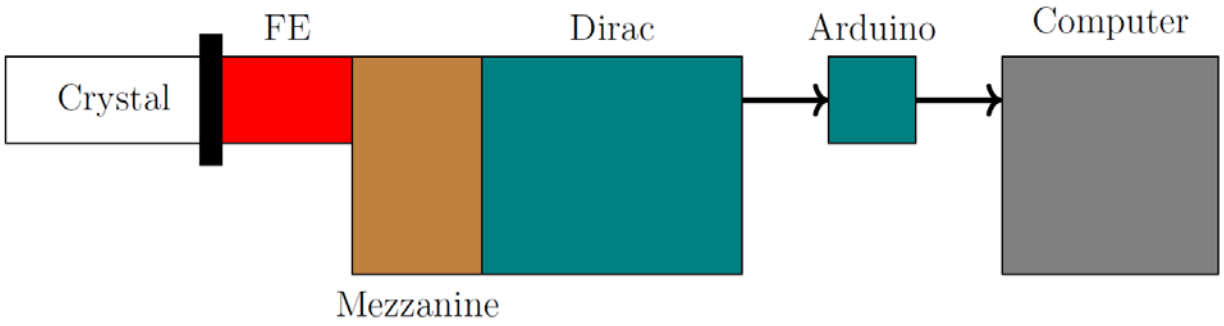
Proto Slice test: LED + SiPM

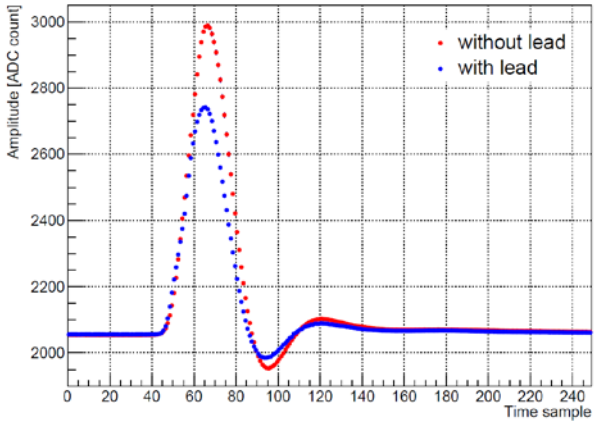




Readout signal
200 MHz 12 bit

Proto-Slice test: CsI + SiPM + Cosmic





Readout signal
200 MHz 12 bit

DIRAC V1 status

- Full chain test for 1 channel
- 20 channels firmware already in place. Currently we are optimizing clock constraints to reach 200 MHz an all channels
- NO design issues up to now

Towards V2 …

- A version V2 is currently under design.
- We will replace some components (FPGA, fiber optics transceiver, DCDC converter) to increase radiation strenghten
- Most of components (e.g. ADCs) will not be changed in V2 release.

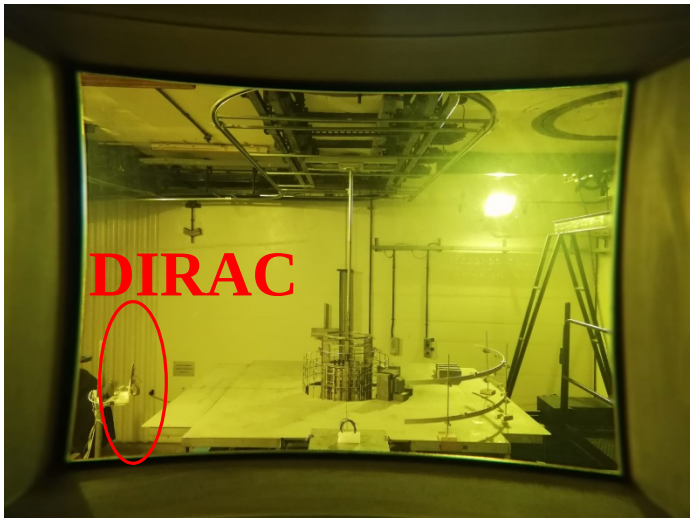
DIRAC radiation test

- DIRAC board must be qualified to be used in a radiation environment
- Several tests are required:
  1. Total Ionizing Dose (TID)
  2. Displacement Damage (DD) Neutrons
  3. Single Event Effects (SEEs)

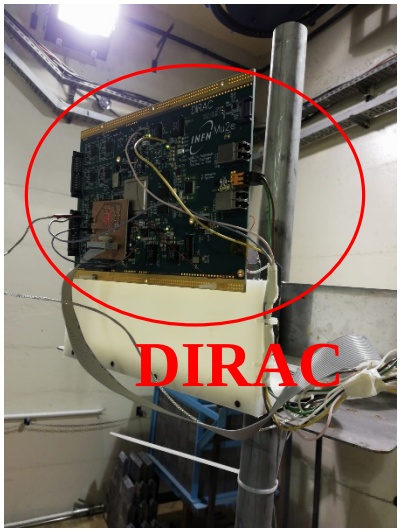
TID tests on V1 done few months ago, DD done only on few components, SEEs foreseen next year on V2

Expected TID ≈ 0.2 Krad/y → 1 Krad in 5 years. Collaboration requires an accectance test with a safety factor 12 → we have to qualify DIRAC for TID up to 12 Krad dose

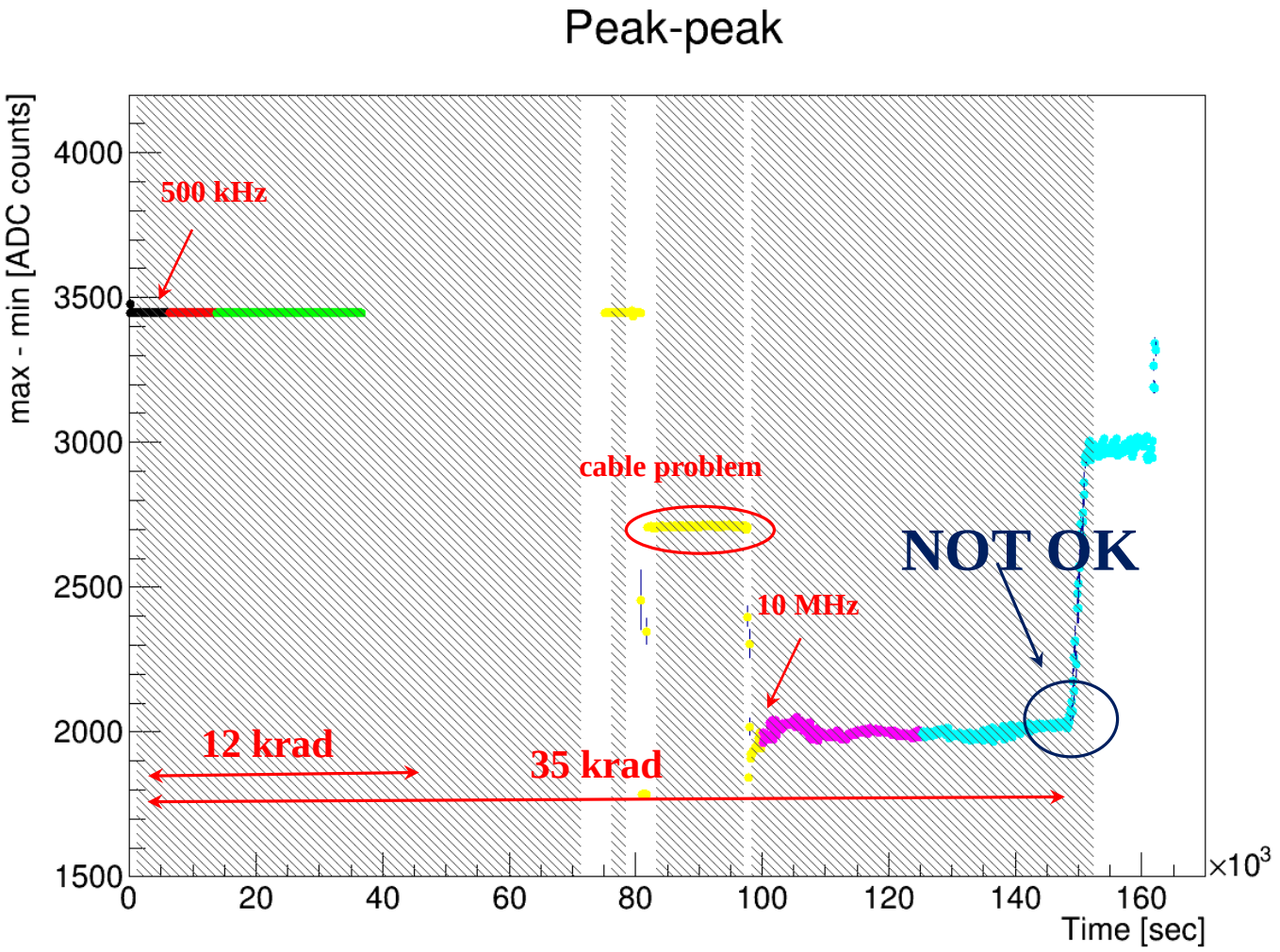
TID test @ ENEA Casaccia (1)



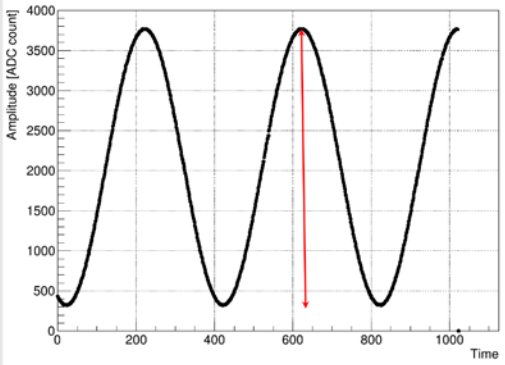
- Co60 source
- Full board test
- Dose is function of distance -> max 2 krad/h
  - ✓ Tested at 1 Krad/h
- Start: June 13 @ 1.30 PM
- Stop: June 15 @ 9.20 AM
- Dose requested: 1Krad/ h
- Total dose: ≈ 41 krad



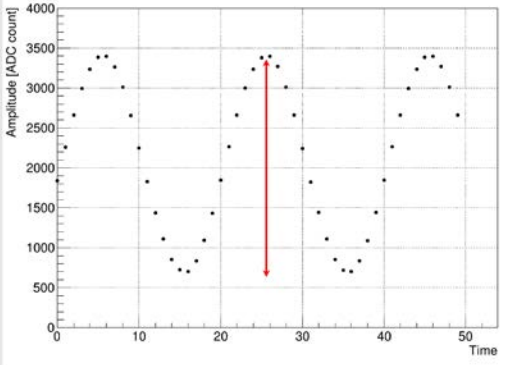
TID test @ ENEA Casaccia (2)



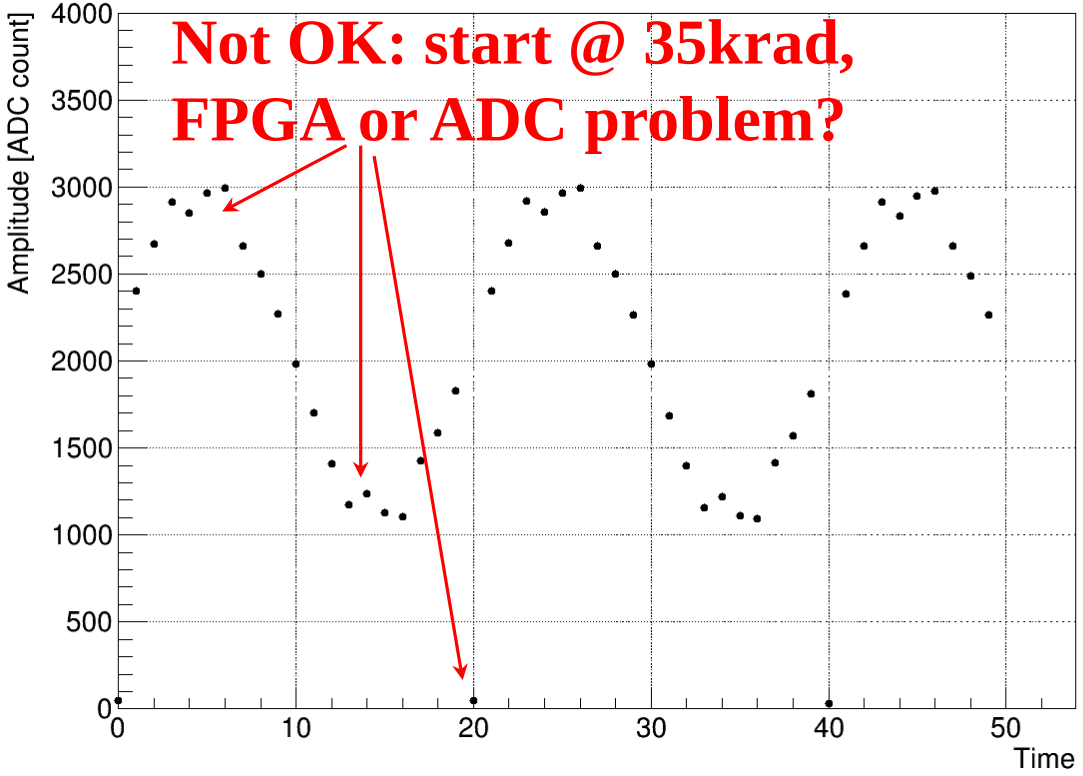
TID test @ ENEA Casaccia (3)



- Input waveform →sin 3V@ 500 KHz



- Input waveform:
- 3 V @ 500 KHz → 4.5V@ 10MHz



- Input waveform →sin 4.5V@ 10 MHz

TID test @ ENEA Casaccia: results

- 41 h beam time
- Nominal Dose Rate (NDR) ≈ 1krad/h
- Total dose ≈ 41krad
- No evidence of broken components up to 30 krad
  - ✓ Could be ADC or FPGA
- After 41 krad SM2 ARM does not restart after power cycle
- DCDC converters voltage increase: ≈ 20% @ 41 krad

Thank you!