PIP2 MEBT Kicker Review

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Chopper Review Meeting
2 August 2018

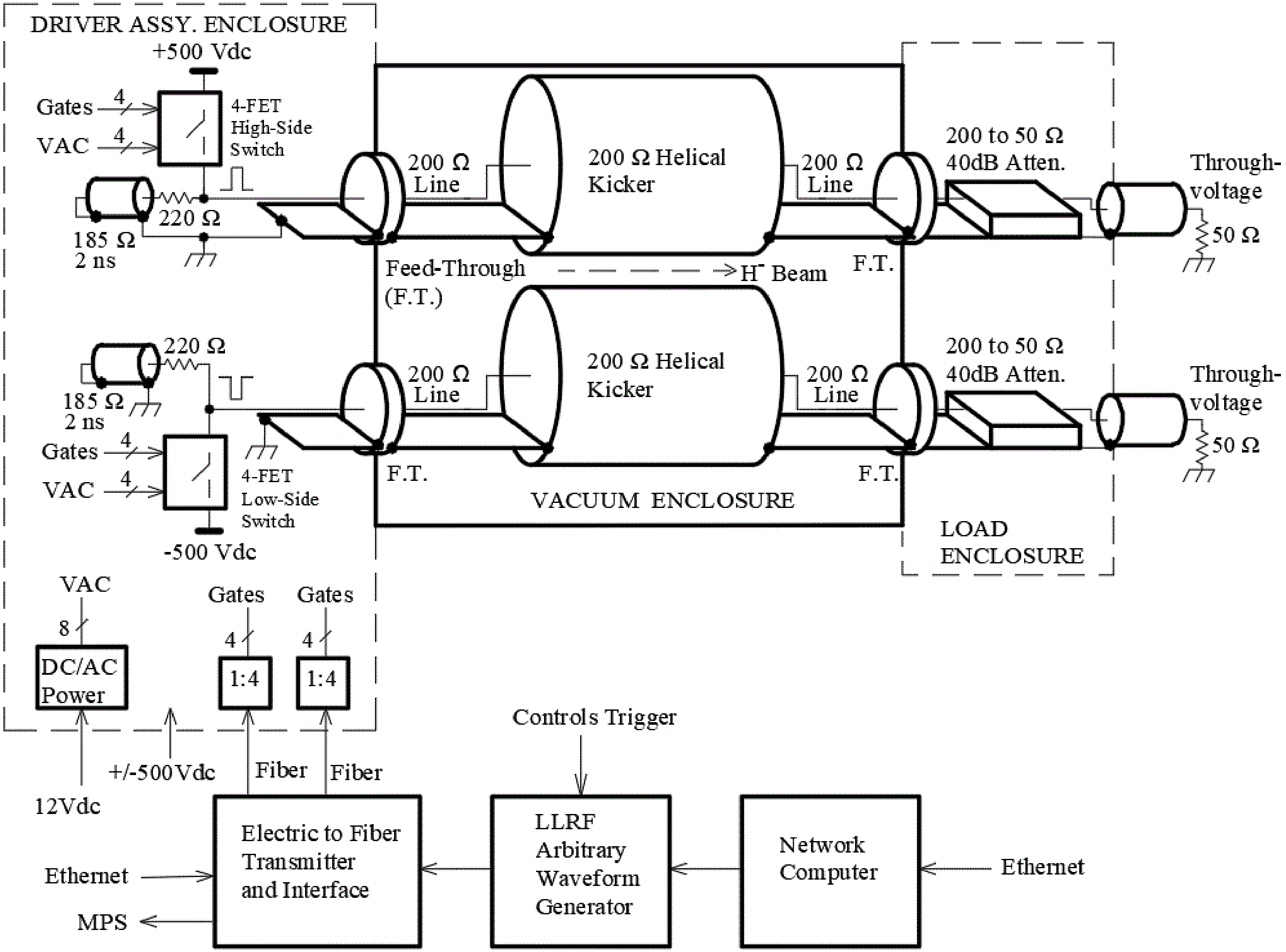
Outline

- Requirements overview & system design approach
- Challenges
- Design details
- Electrical performance results
- Issues to be addressed

Kicker Requirements

- Kick individual bunches (bunch-by-bunch)
- Rise/fall time 4.0 ns (5-95%) maximum between bunches
  - This leaves 2.15 ns flattop to both kick and pass
- Kicking scheme
  - +/- 500 V to kick beam out, 0 V to pass
- Kick an arbitrary pattern for Booster delivery (at 20 Hz)
  - 45 MHz average switching rate during 550 μs macro-pulse
  - 0.5 MHz overall average switching rate
- Beam test modes
  - 81.25 MHz switching rate for 10's of μs, at 20 Hz
  - Any arbitrary pattern having switching rates <81 MHz and <0.5 MHz average

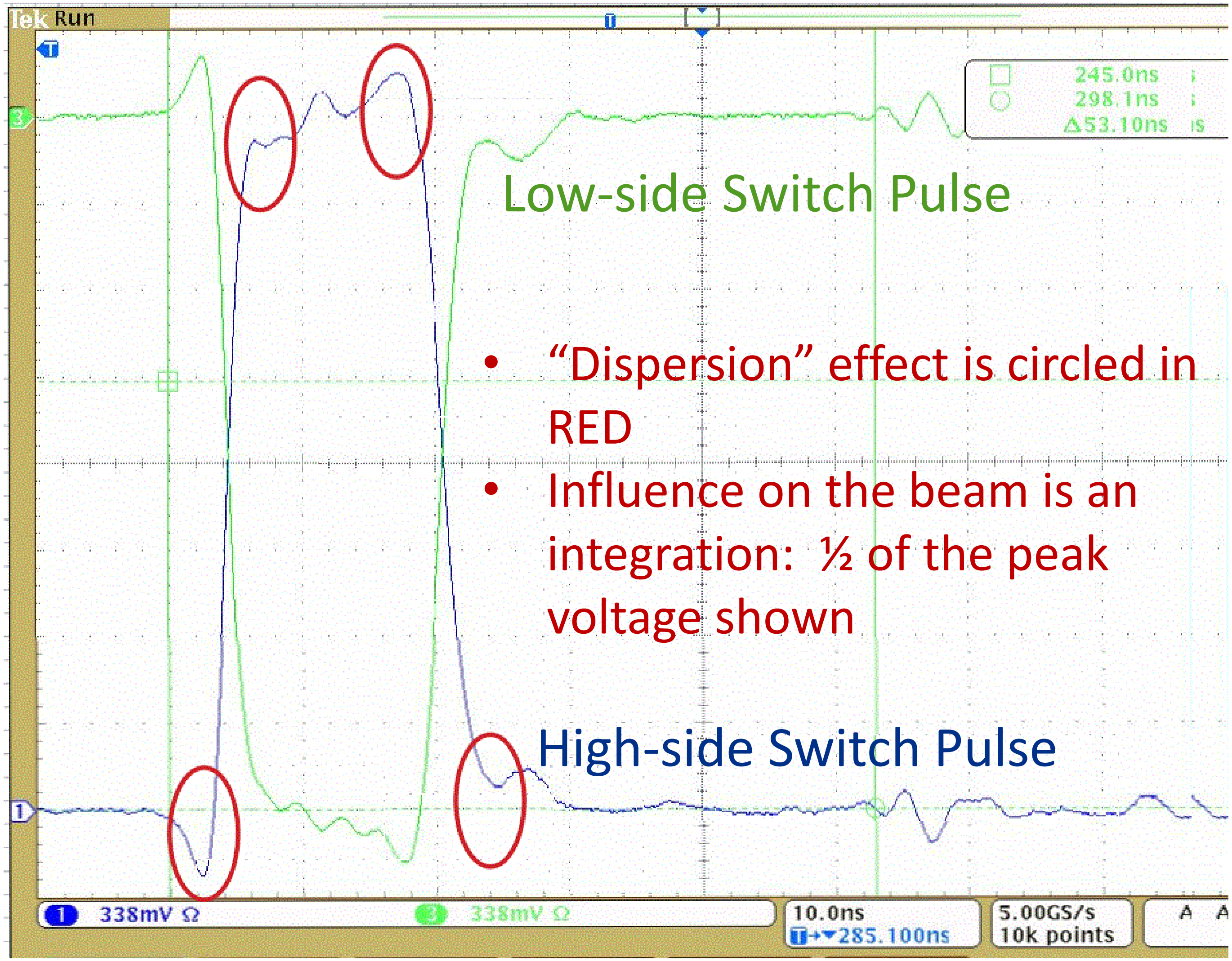
Kicker System



Overview – the Helix

- Dual 200 Ohm helical, traveling wave structure
  - 200 Ω (as opposed to typical 50) lowers drive current and power making fast switching conceivable
    - <<10 Watts RF skin effect losses in the vacuum
  - Symmetric and broadband structure
    - Potentially low internal reflections
- Thermal design
  - ~0.1 gpm water-cooled ground tube for 40 W beam loss
- Includes protection electrodes
- Challenges
  - Match propagation to beam velocity
  - Reflections
    - Discontinuities between helix, 200 Ω strip lines and load
  - Frequency dependent effect (referred to as “dispersion”)
    - Cause: inter-winding coupling and winding capacitance to ground

“Dispersion” Effect



Low-side Switch Pulse

- “Dispersion” effect is circled in RED
- Influence on the beam is an integration: ½ of the peak voltage shown

High-side Switch Pulse

Addressing the Helix Design Challenges

- Propagation time is matched to beam beta by a tuning procedure
  - Both prototype helices were tuned to -0.5% of ideal
- Reflection issues
  - Microstrip lines in and out are designed for 200 Ohms
    - Feed-through to strip line to helix reflections are low
  - Helix low impedance end-effects cause reflections
    - Coupling between windings raises strip line impedance from ~140 to 200 Ω … but the turn at each end lacks the coupling
    - Modeling used to find suitable compensation scheme
    - Ground tube stepped 1-turn, both ends, raises impedance
    - Reflection reduced about 30%
  - Load reflection can be compensated with small series inductance
  - Switch-driver close to feed-through (and no coax) reduces reflections
- Dispersion effect reduction
  - Helices are located away from ground surfaces by 1.75”
  - Helix dimensions were chosen to be slightly faster than beam beta
  - Adding inter-winding capacitive plates provides compensation
  - Compensation decreases dispersion and increases propagation time
    - Integrated value of dispersion voltage peaking reduced to <5%

Overview – Helix Drivers

- Kicker drivers are fast switches
  - One single-switch driver per helix, opposite voltage polarity
- Apply ±500 V to kick beam out, 0 V to pass
- Switches are series-connected FETs to share switching losses
  - Total switch switching loss from Cds, 3 FETs in series:

$$3 * \frac{1}{2} Cds\left(\frac{v}{3}\right)^2 f = \frac{1}{3} * \frac{1}{2} CdsV^2 f \quad (Watts)$$

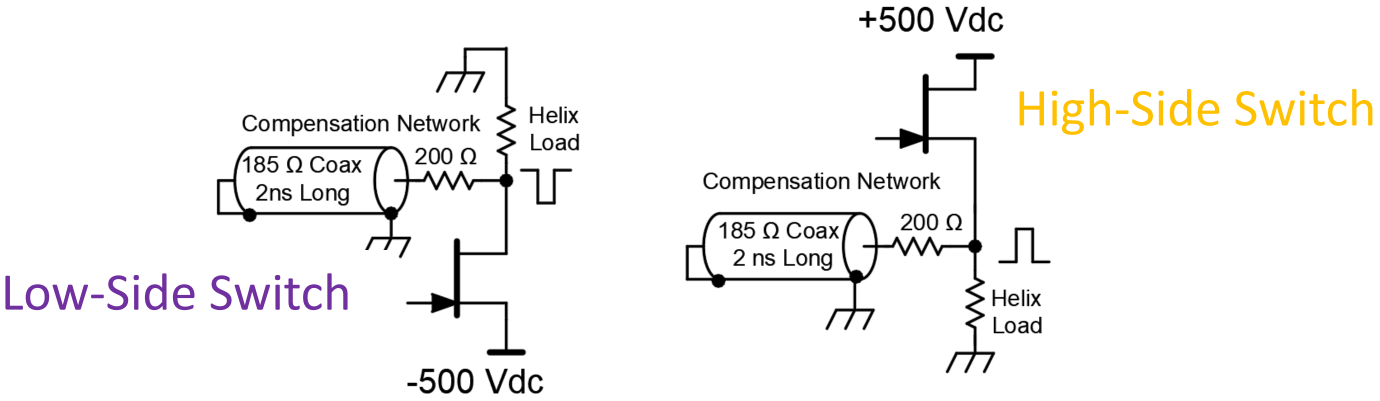
- Switch construction
  - Each switch fully isolated
  - Each FET is individually gated simultaneously
- Driver design challenges
  - Switch on and off fast enough
  - Custom FET gate driver required for this switching speed
  - Determine FETs reliability to handle thermal cycling
  - Handling switching losses for Booster requirement
    - 1 μJ switching loss per cycle – capacitive switching loss
    - 45 Watts are dissipated per FET at 45 MHz rep rate

Addressing the Driver Design Challenges

- Photonics laser and transmitter provides precision triggering
  - The generator signal gates laser
  - Splitters deliver triggering to all FETs simultaneously to photo detectors on each GaNFET driver board
- Switching speed is obtained using GaN FETs (GaN Systems, Inc.)
  - GS66502B: 7 Adc, 15 A pulsed; 650 V; 20 pF d-s, 65 pF g-s
  - GaNFET driver circuit kept as small as conveniently possible minimizing parasitics
- Custom FET gate driver circuit designed with operating margin
  - Turn-on time is settable to <2 ns
  - 3-FET switches operate at 500 V above 90 MHz; and 81.25 MHz at 600 V
  - A Calibration procedure used to match FET timing
    - Both turn-on and -off delay are matched to +/-100 ps
    - Allowance remains for shifts due to time and temperature

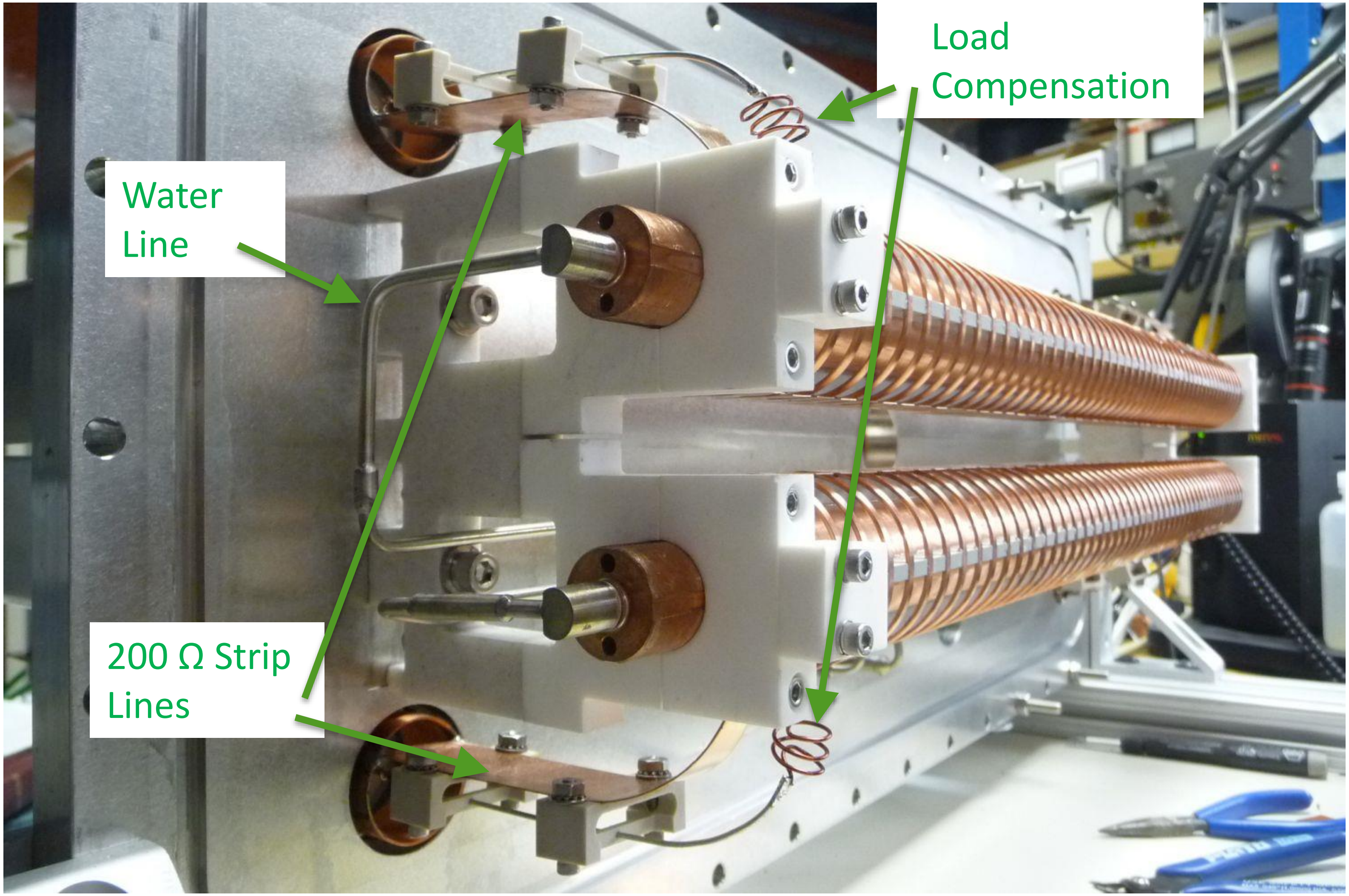
Addressing the Driver Design Challenges (cont.)

- FET reliability test: 3-FET switch was operated for 4 months 24/7
  - 500 V bias, 45 MHz for 550 µs at 20 Hz (Booster ave. switching rates)
  - No evident timing variations
  - Demonstrates GaN FETs are not overly stressed
- Turn-off time reduced to <4 ns with compensation:



- 500 V on the plate assumes 100% efficient kicker
  - Helices are 95-97% efficient
  - 3 V drop in the switch
  - Required bias voltage is ~528 Vdc
  - Our present limit is 500 Vdc bias voltage

Helical kickers

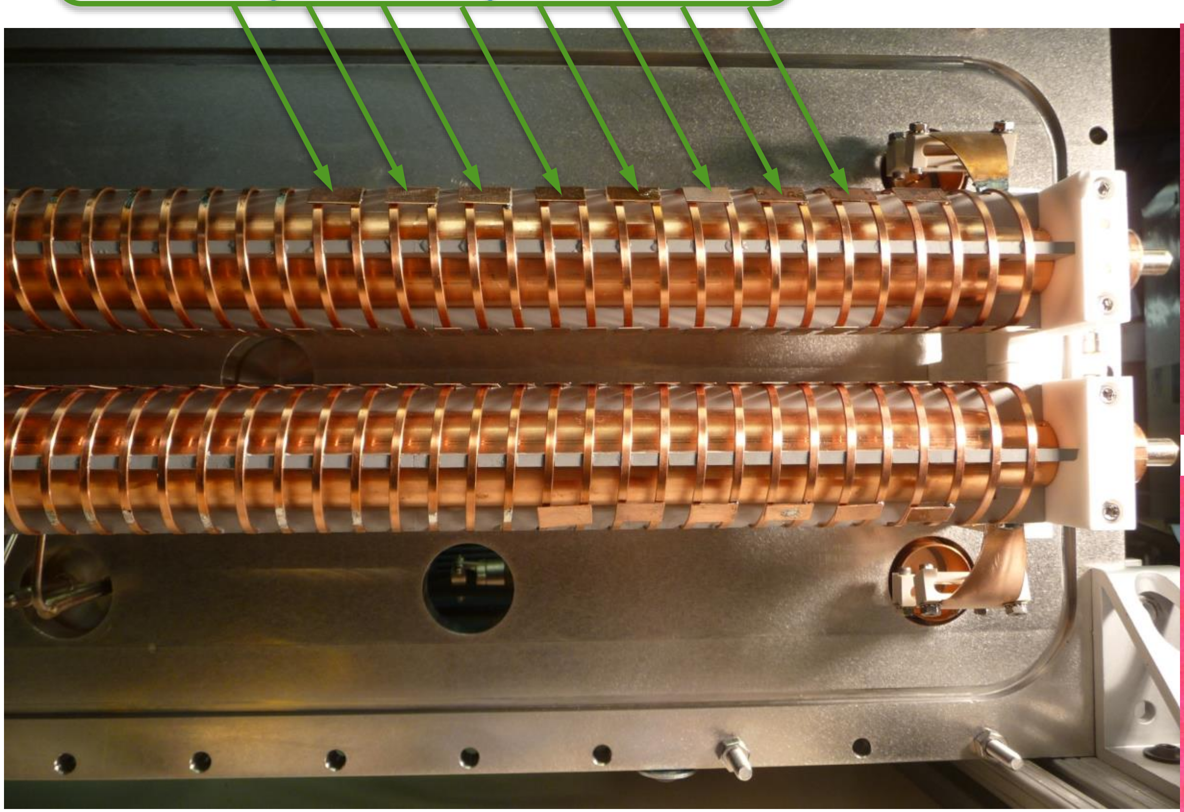


Load Compensation

Water Line

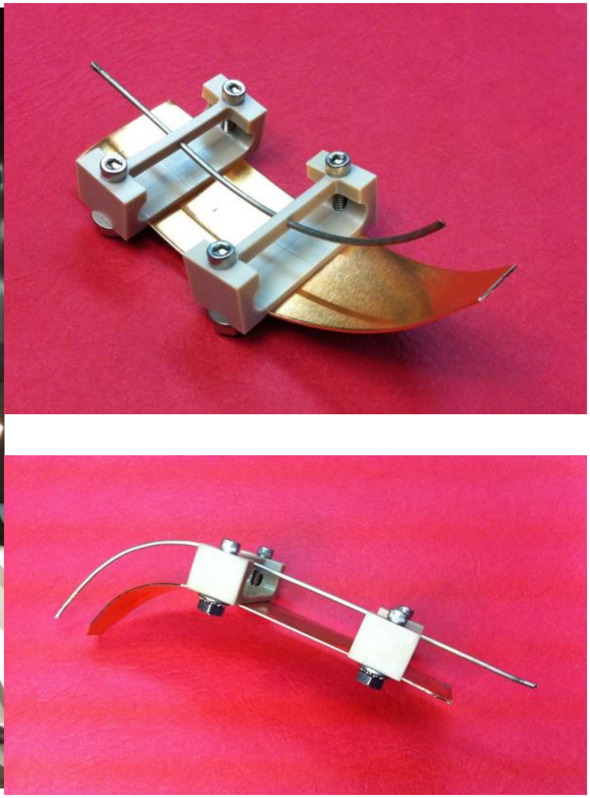
200 Ω Strip Lines

Dual-Helix Assembly



Dispersion compensation:
capacitive plates

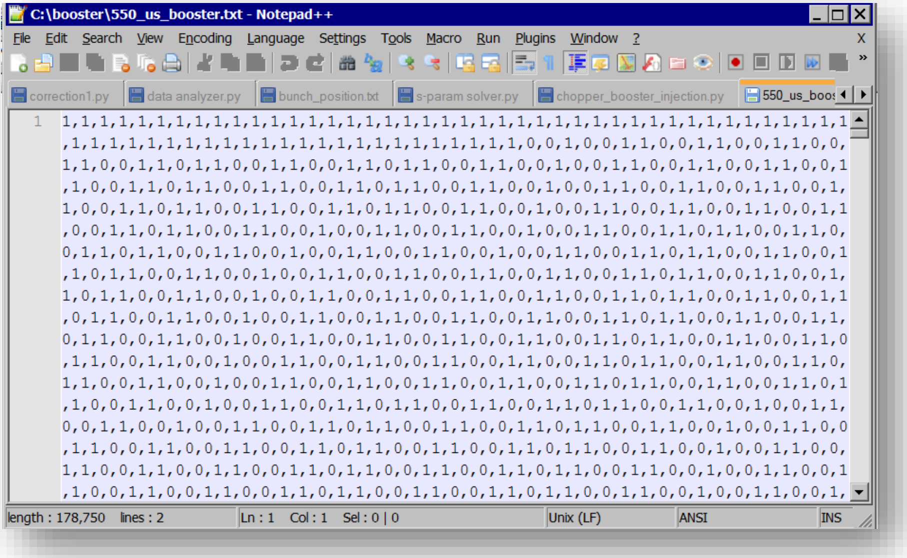
Strip line Construction



LLRF’s Arbitrary Waveform Generator

- 1’s/0’s in a file define kick/pass switching pattern are downloaded to the Generator
- Phasing as well as turn on/off edge adjustments can be set with ~40 ps resolution
- The arbitrary 550 μs Booster pattern was used at PIP2-IT:

The File



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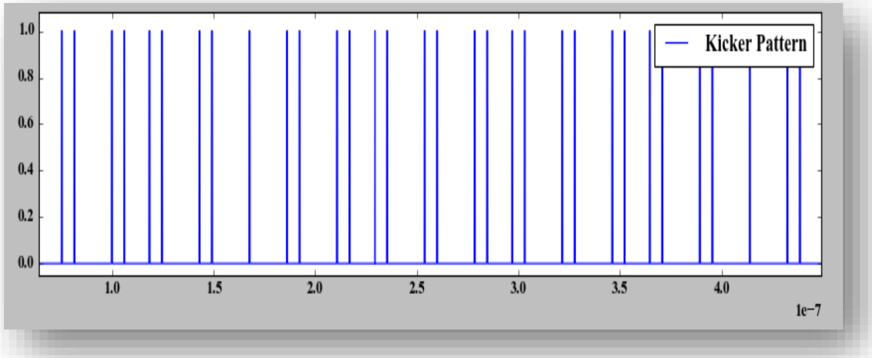
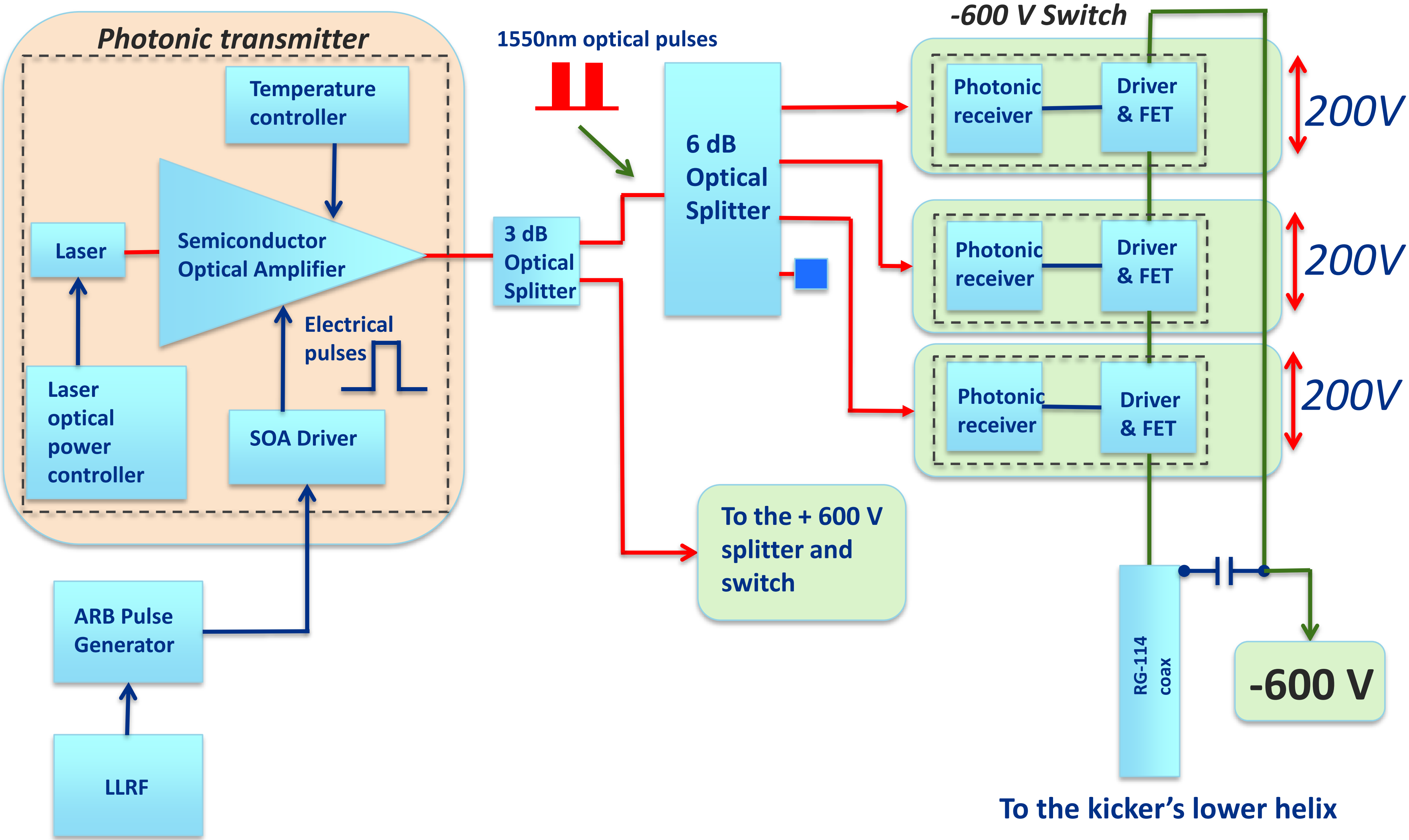
length : 178,750 lines : 2 | Ln : 1 Col : 1 Sel : 0 | 0 | Unix (LF) | ANSI | INS

The Arbitrary Kicking Pattern



Electric to Fiber Transmitter & Switch



Photonic transmitter

Temperature controller

Laser

Semiconductor Optical Amplifier

Electrical pulses

Laser optical power controller

SOA Driver

ARB Pulse Generator

LLRF

1550nm optical pulses

3 dB Optical Splitter

6 dB Optical Splitter

To the + 600 V splitter and switch

-600 V Switch

Photonic receiver

Driver & FET

200V

Photonic receiver

Driver & FET

200V

Photonic receiver

Driver & FET

200V

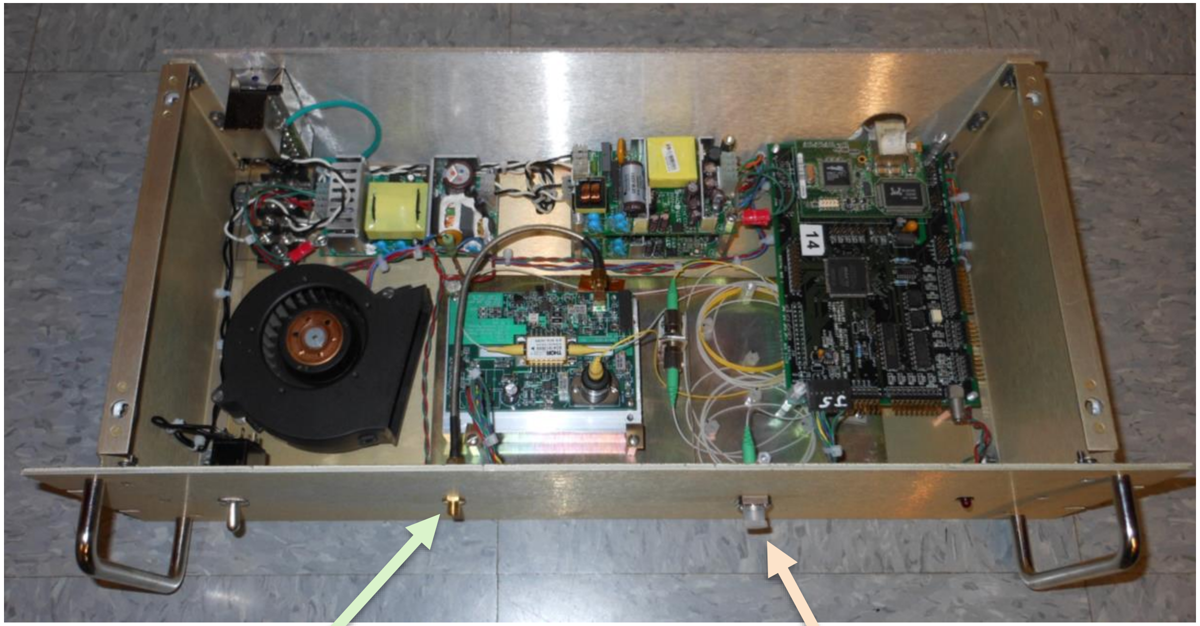
RG-114 coax

-600 V

To the kicker’s lower helix

Photonic Transmitter Chassis

Photonic transmitter:

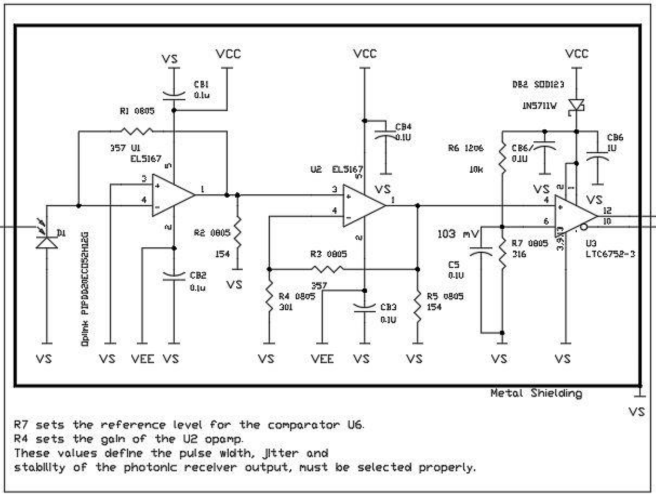


0.6 V TRIGGER INPUT

1550 nm OUTPUT

GaNFET Driver Circuit

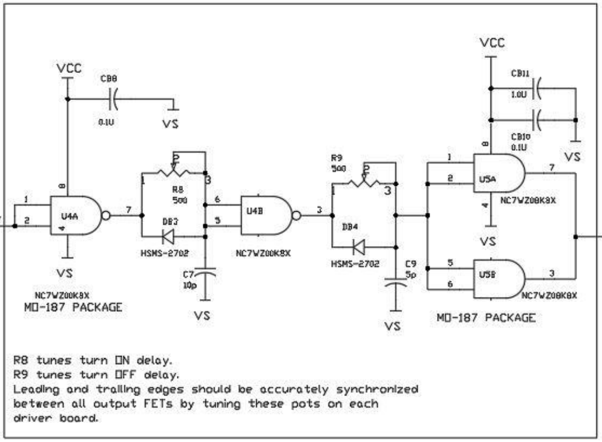
Detector Stage



R7 sets the reference level for the comparator U6.
R4 sets the gain of the U2 opamp.
These values define the pulse width, jitter and stability of the photonic receiver output, must be selected properly.

- Photo detector
- 1 GHz opamps: gain (x2)
- 280 MHz comparator

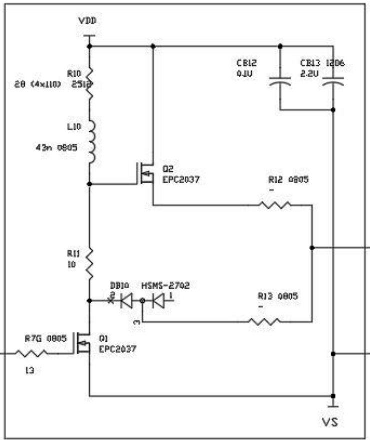
Delay Tuning Stage



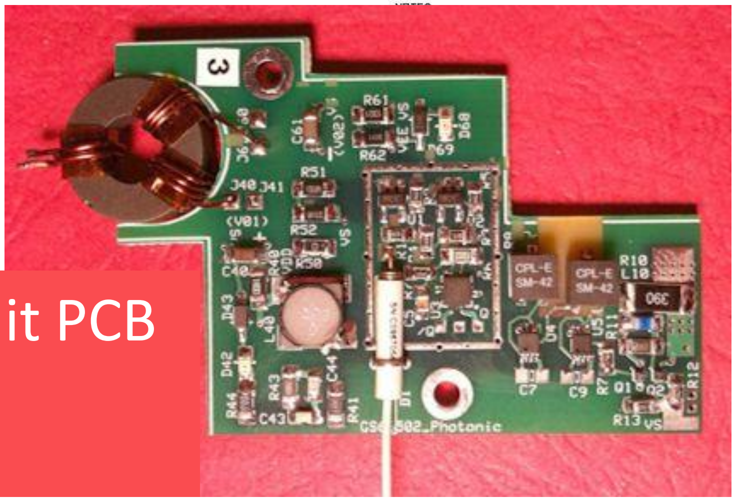
R8 tunes turn ON delay.
R9 tunes turn OFF delay.
Leading and trailing edges should be accurately synchronized between all output FETs by tuning these pots on each driver board.

Turn-on &
Turn-off
delay adjustment

GaNFET Gate Driver



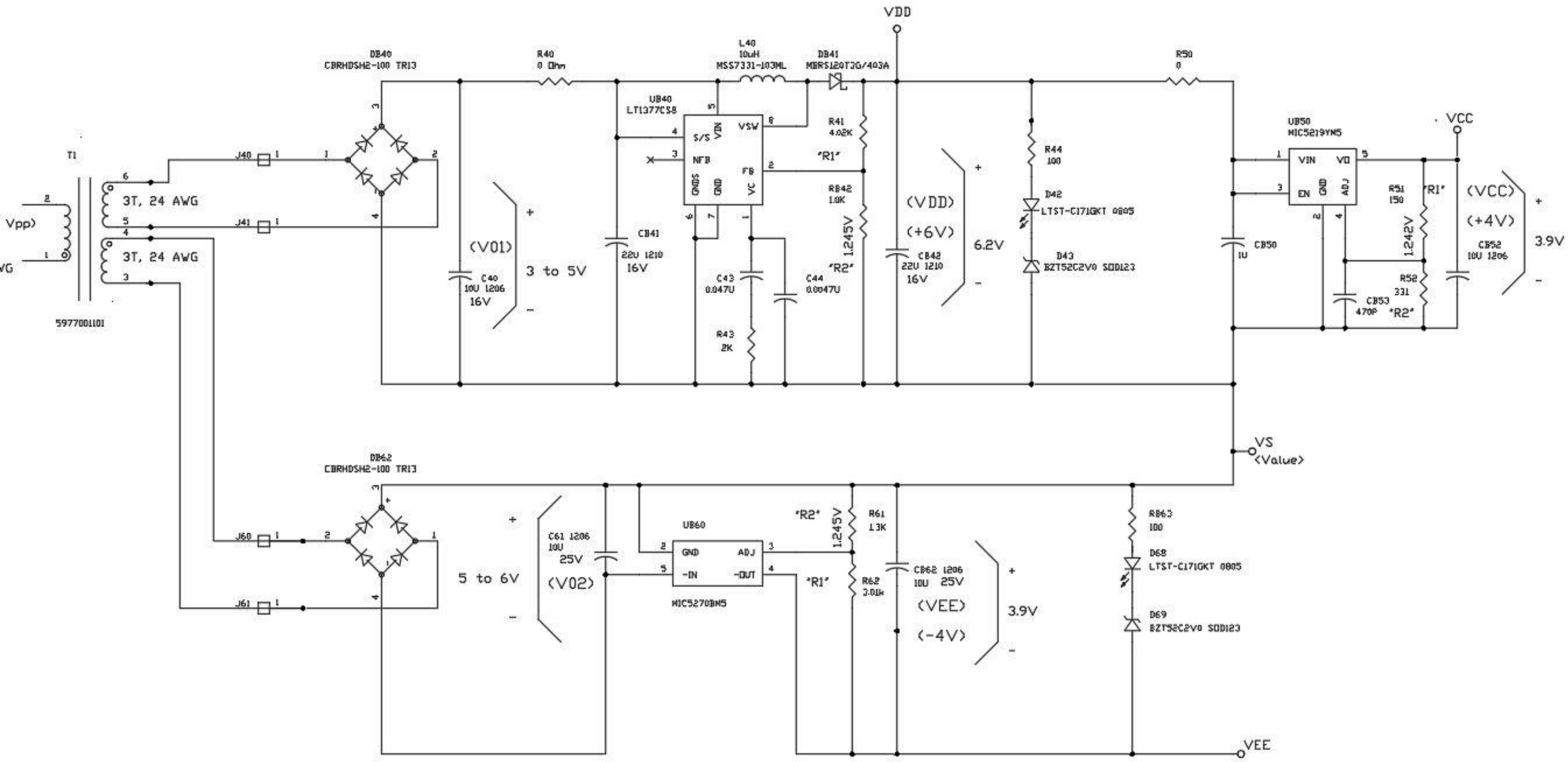
Common source +
source-follower circuit



GaNFET Driver Circuit PCB

- Shields not installed
- size: 2.5” x 1.75”

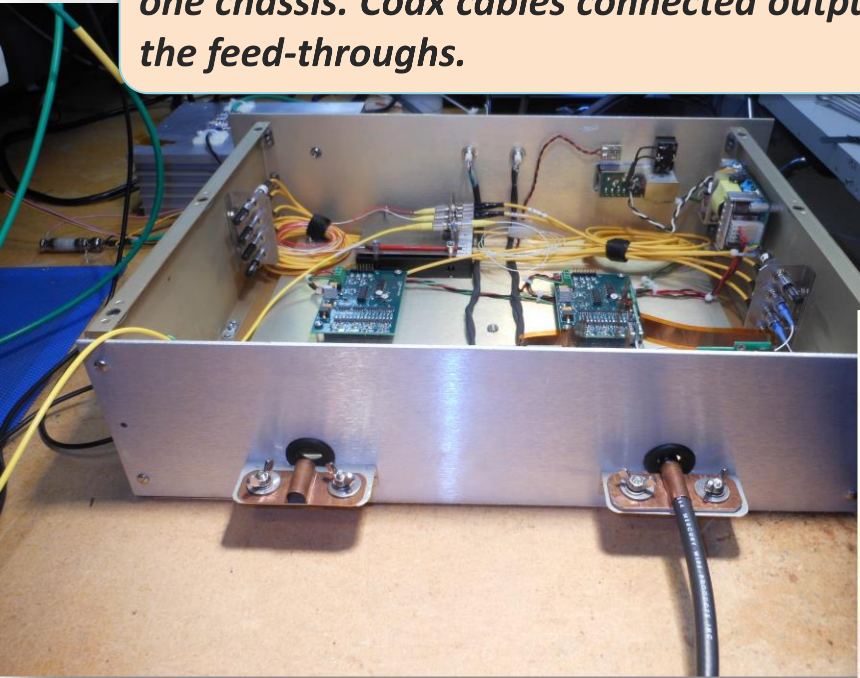
GaNFET Driver Circuit: AC/DC Power

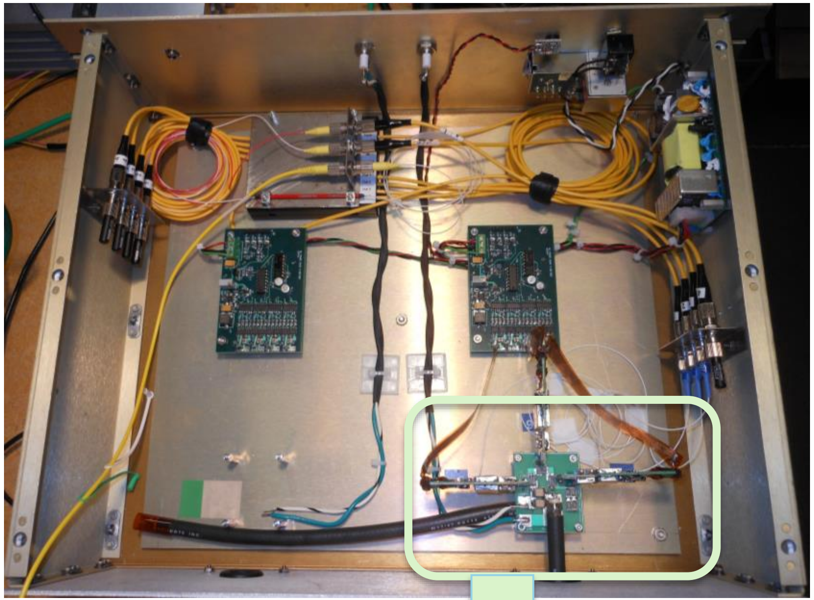


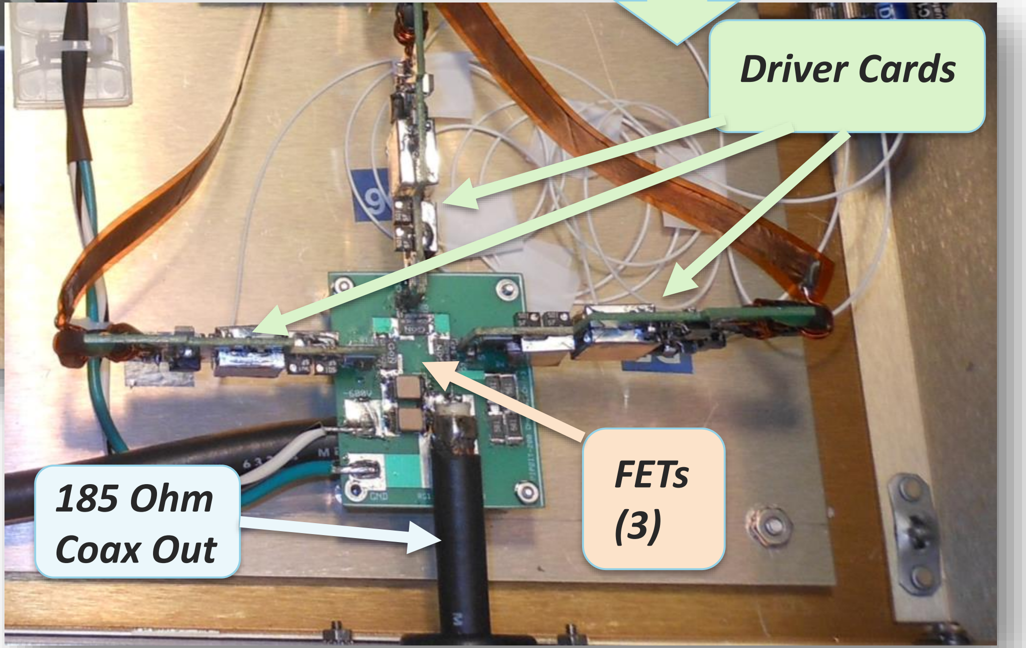
- 3.5 V, 500 kHz AC in
- 3 Well-regulated DC voltages out

The Switch-Driver Chassis
(Photonic Gate Version)

This Version has two switches +/- 600 Volts, in one chassis. Coax cables connected outputs to the feed-throughs.





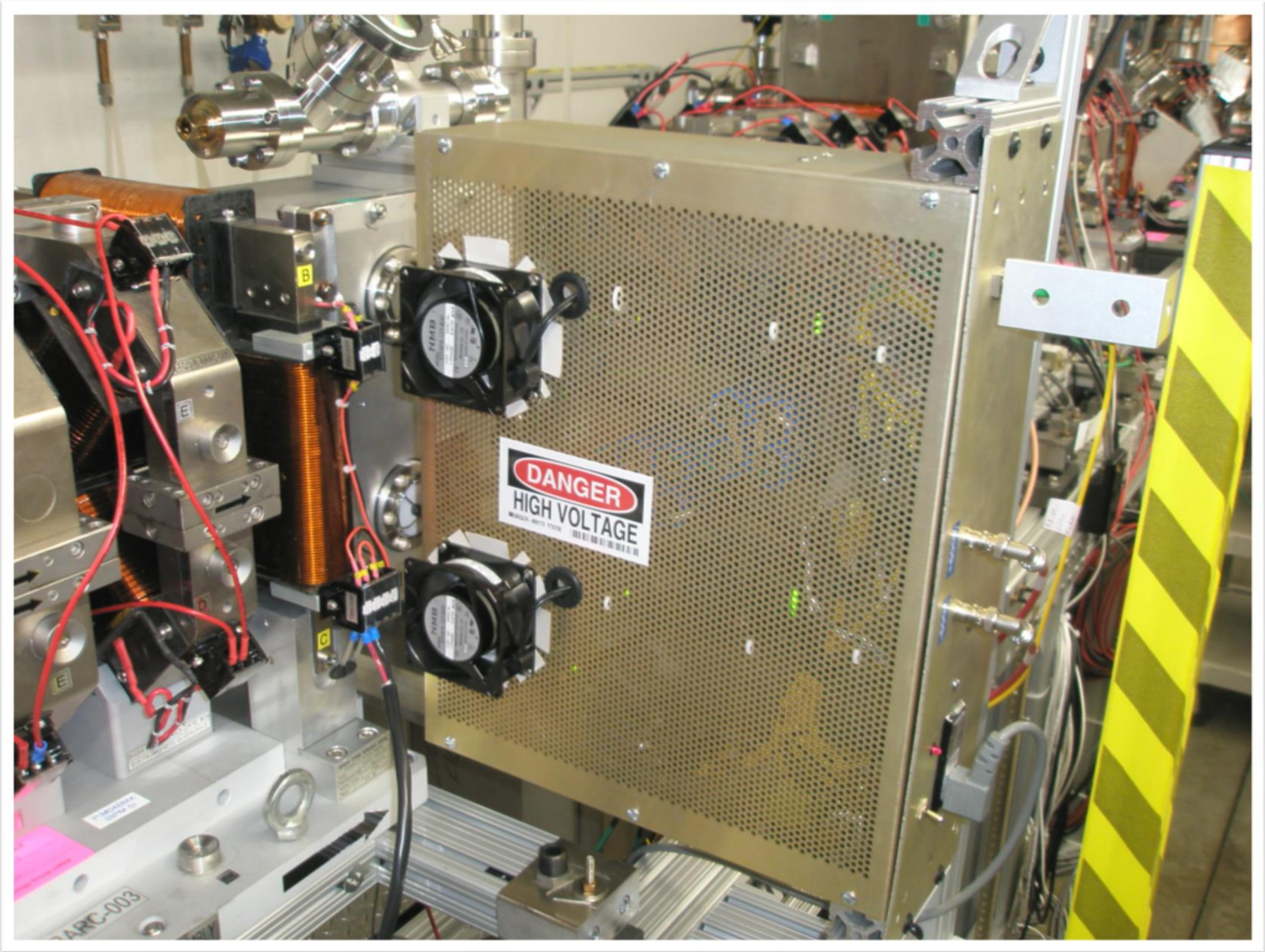


Driver Cards

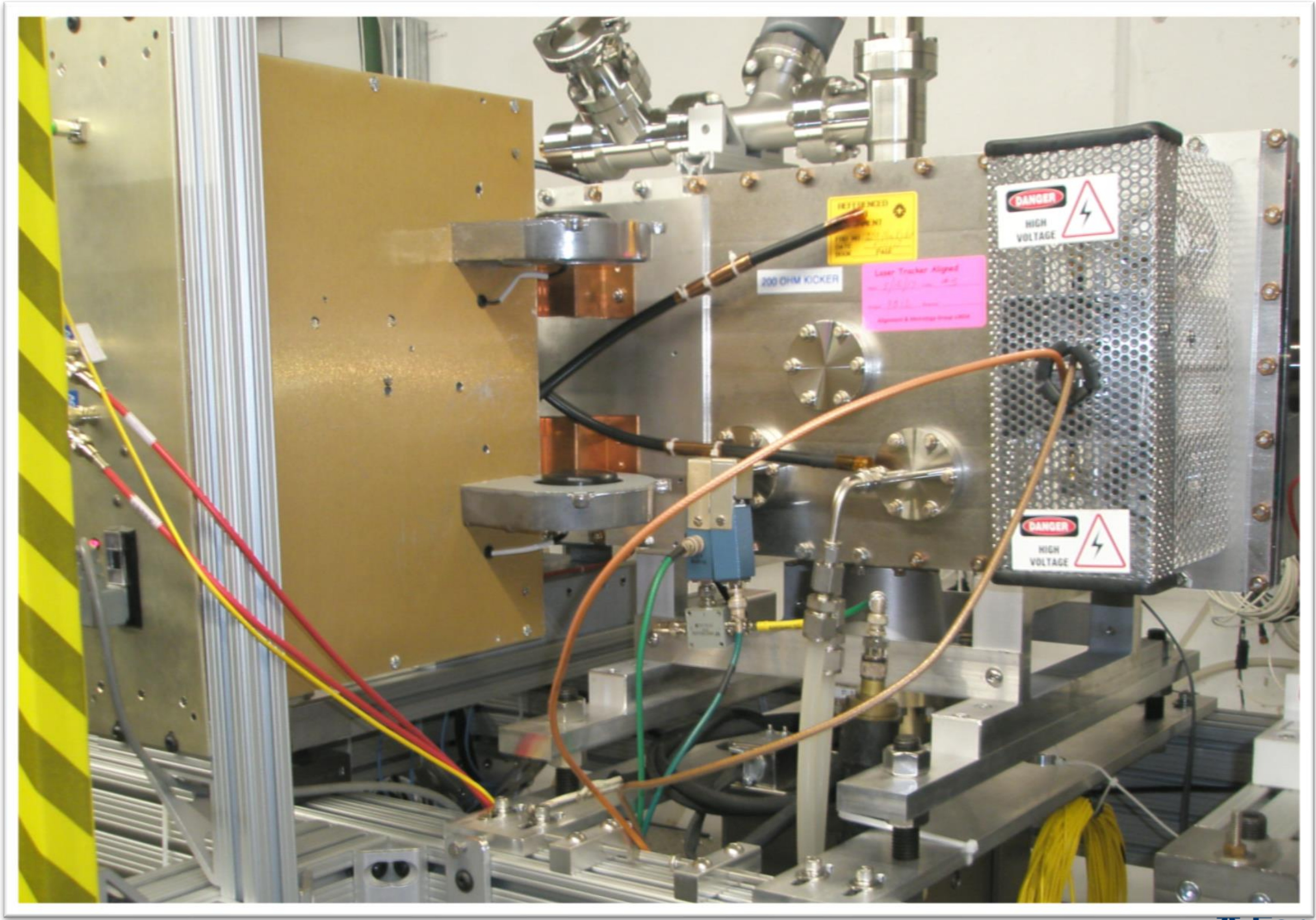
FETs (3)

185 Ohm Coax Out

Driver as installed now in the MEBT



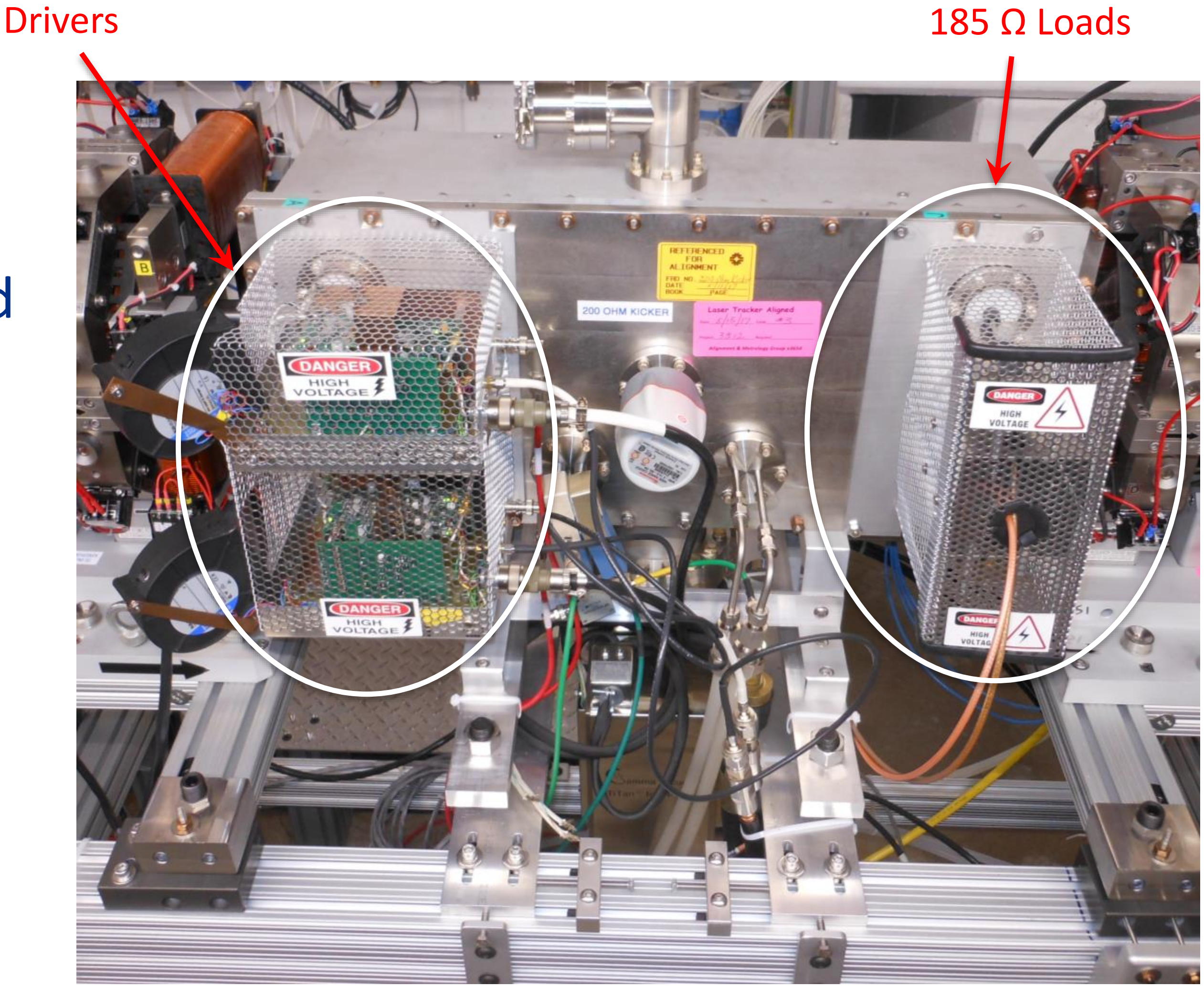
Driver as installed now in the MEBT



First 200 Ohm Chopper Installed at PIP2-IT
(Transformer Gate Version)

Assembly shown similar to intended final version

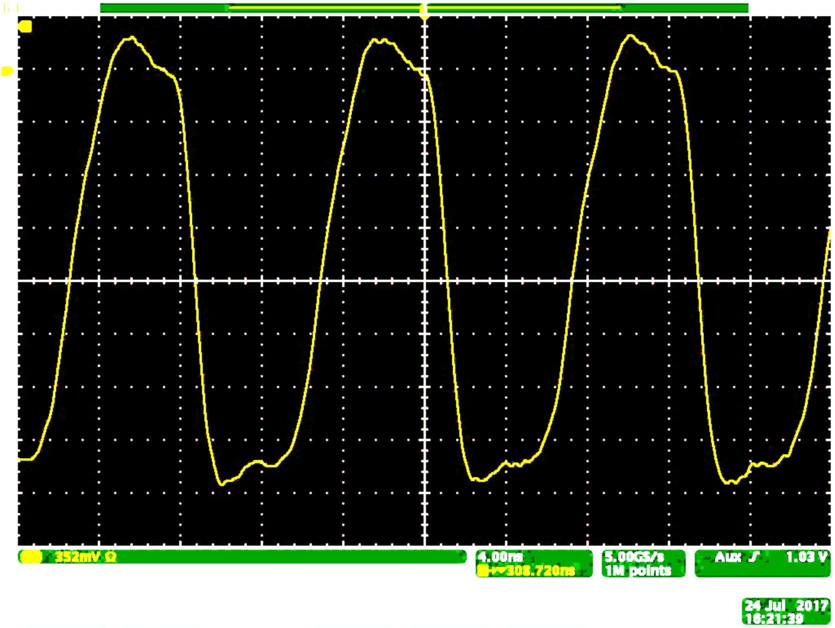
- Switch Driver assembly bolted to the helix plate

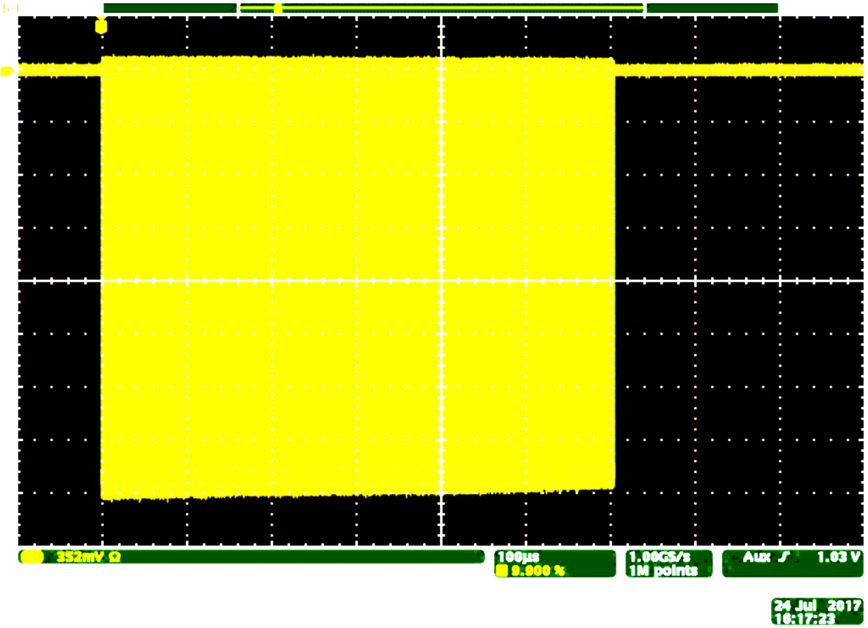


Switch performance

Switching at 81 MHz, 10 us bursts:
600 Vp-p, 4 ns / div

Switching at 45 MHz average rate for 600 us:
600 Vp-p, 100 us / div

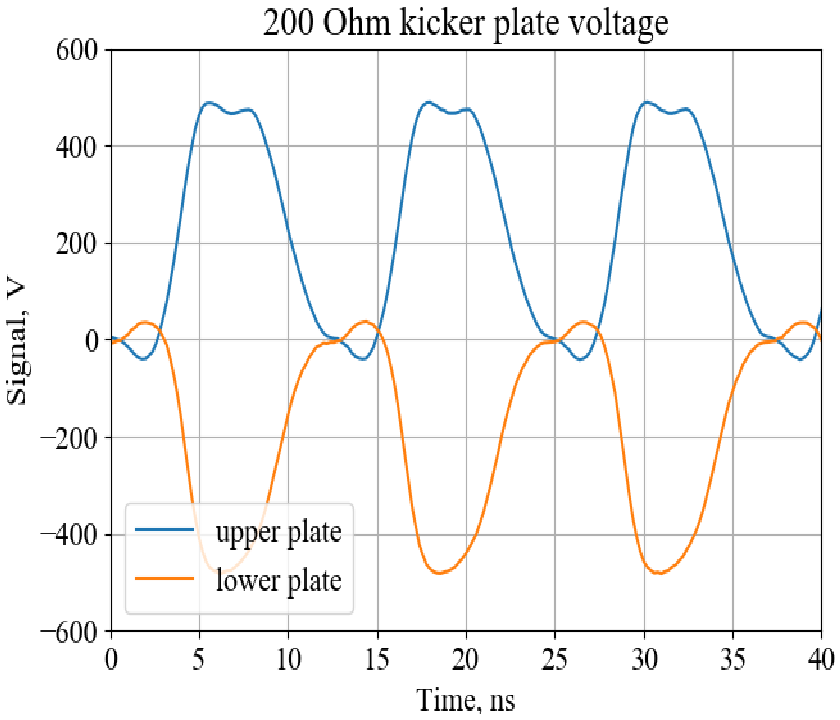




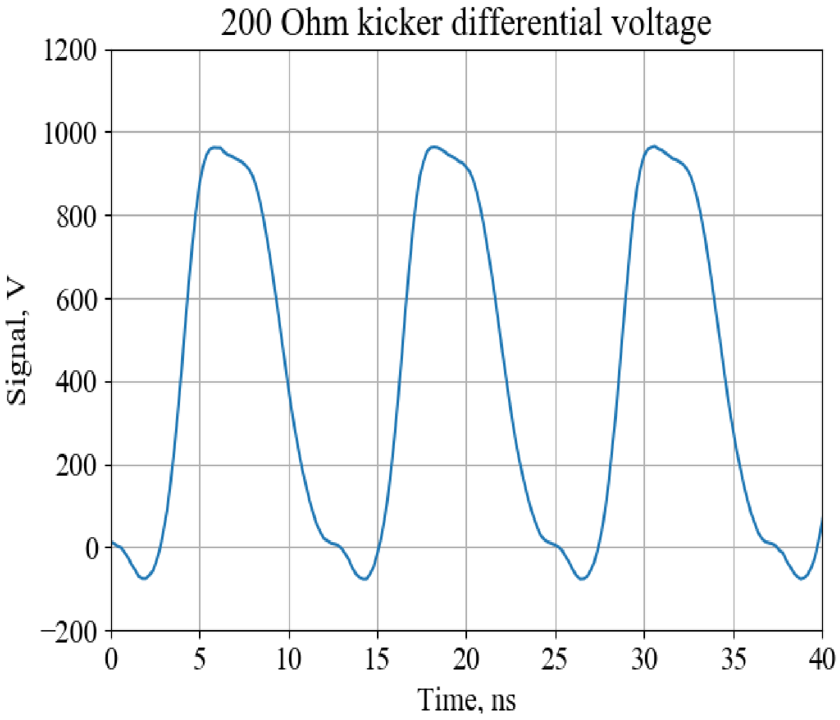
±500V Bias at 81.25 MHz, 20 Hz Repetition Rate

Photonics triggered driver version as operated at PIP2-IT

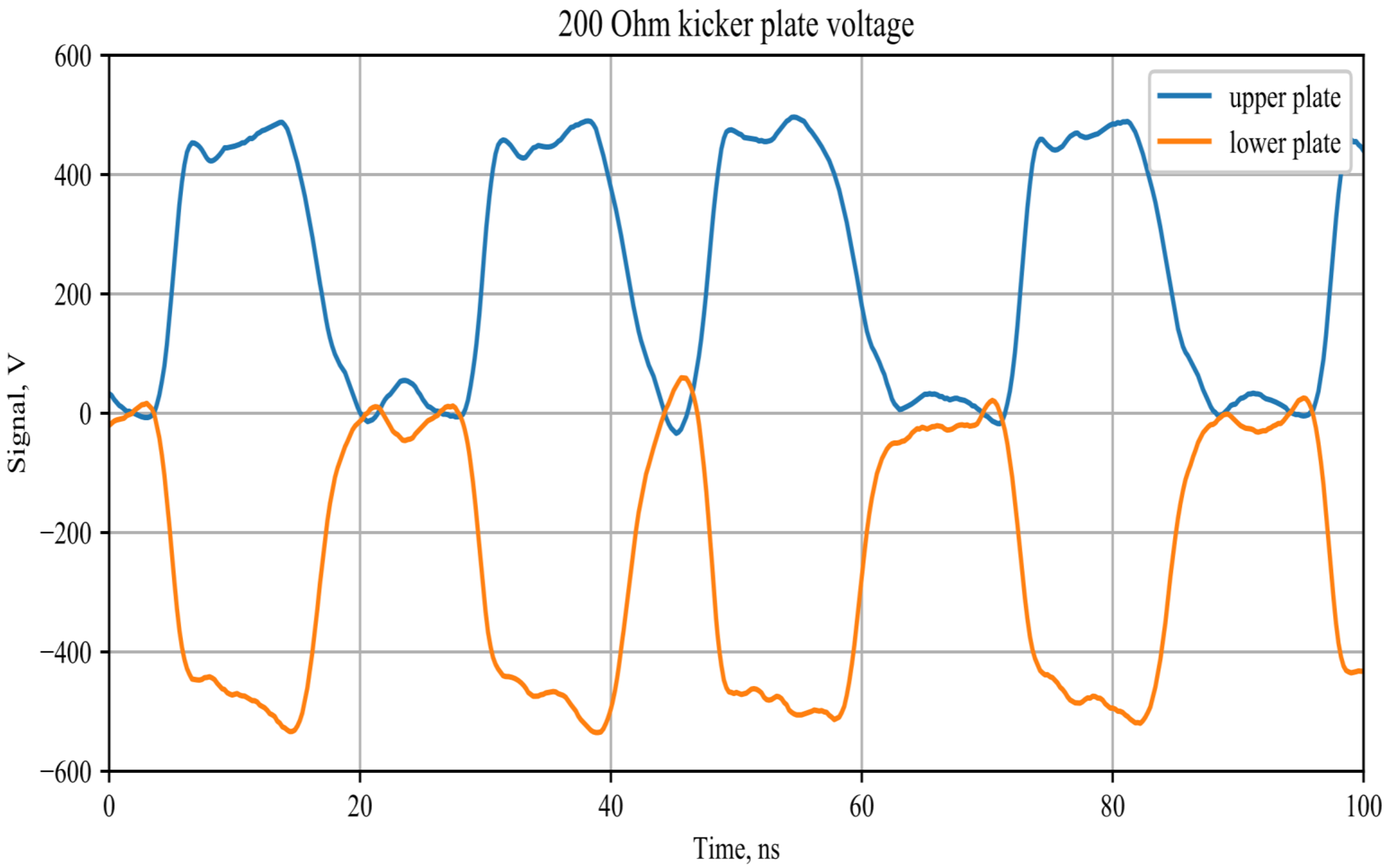
Individual Helix Waveforms



Differential voltage

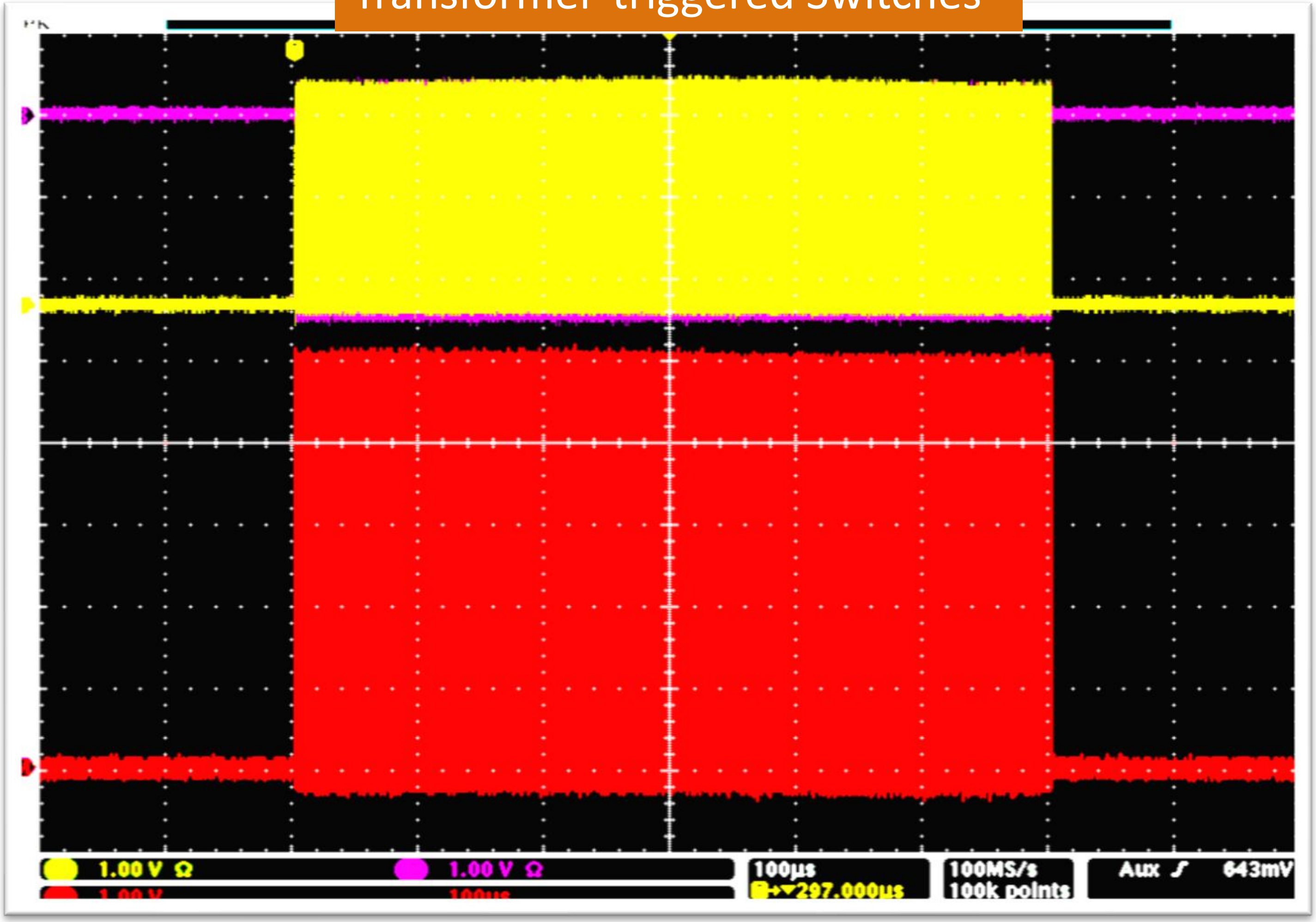


±500V Bias, Arbitrary Pattern



Switching 1100 V, 45 MHz for 600 μs at 20 Hz

Transformer-triggered Switches



Upper Helix

Lower Helix

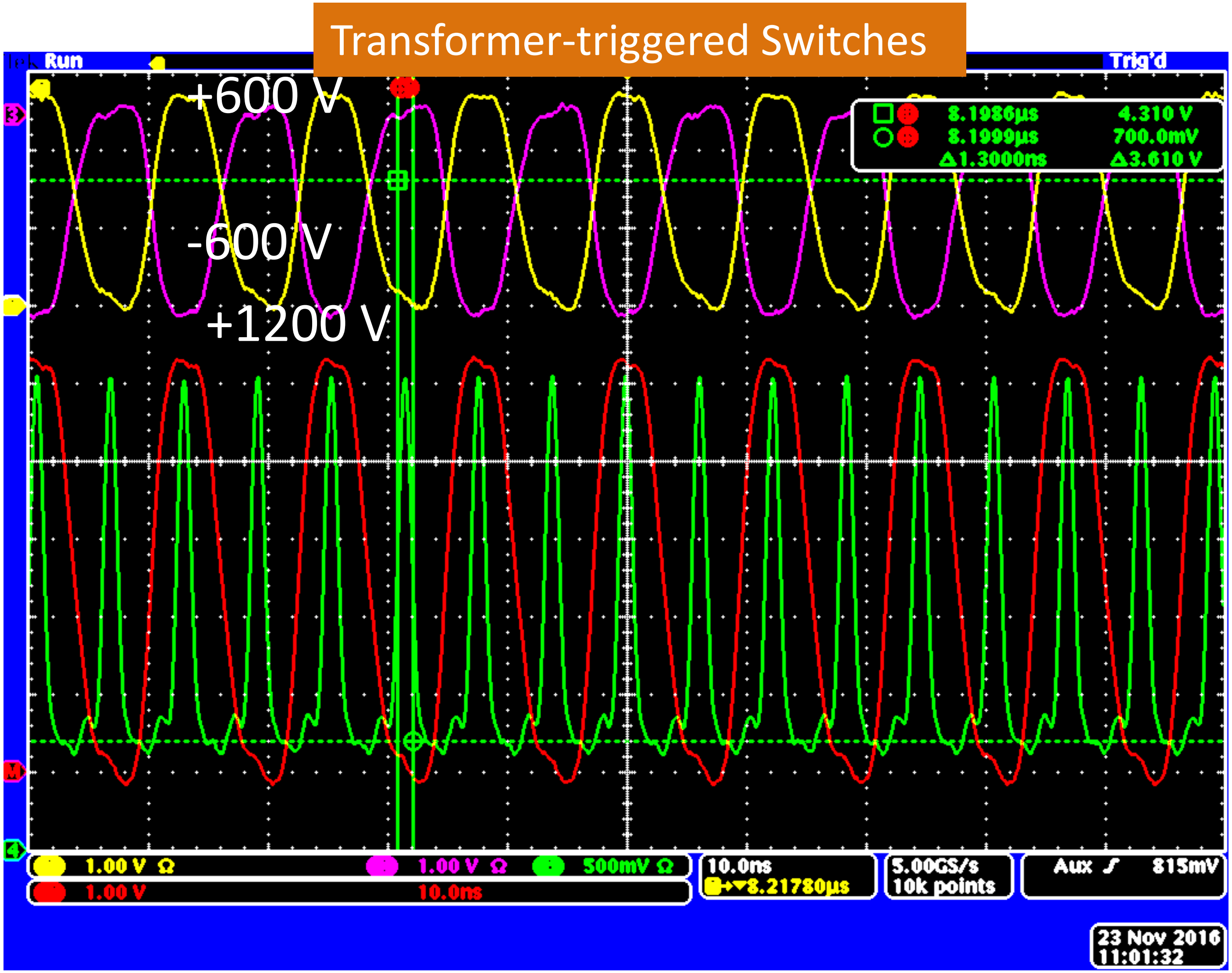
Difference Voltage

Simulated beam bunches

Vertical
≈ 220 V /div

Horizontal:
100 μs /div

Switching at 81.25 MHz, ±600 V; kick every other bunch


Transformer-triggered Switches

+600 V

-600 V

+1200 V

Through-voltages

Upper Helix

Lower Helix

Difference Voltage

Simulated beam bunches

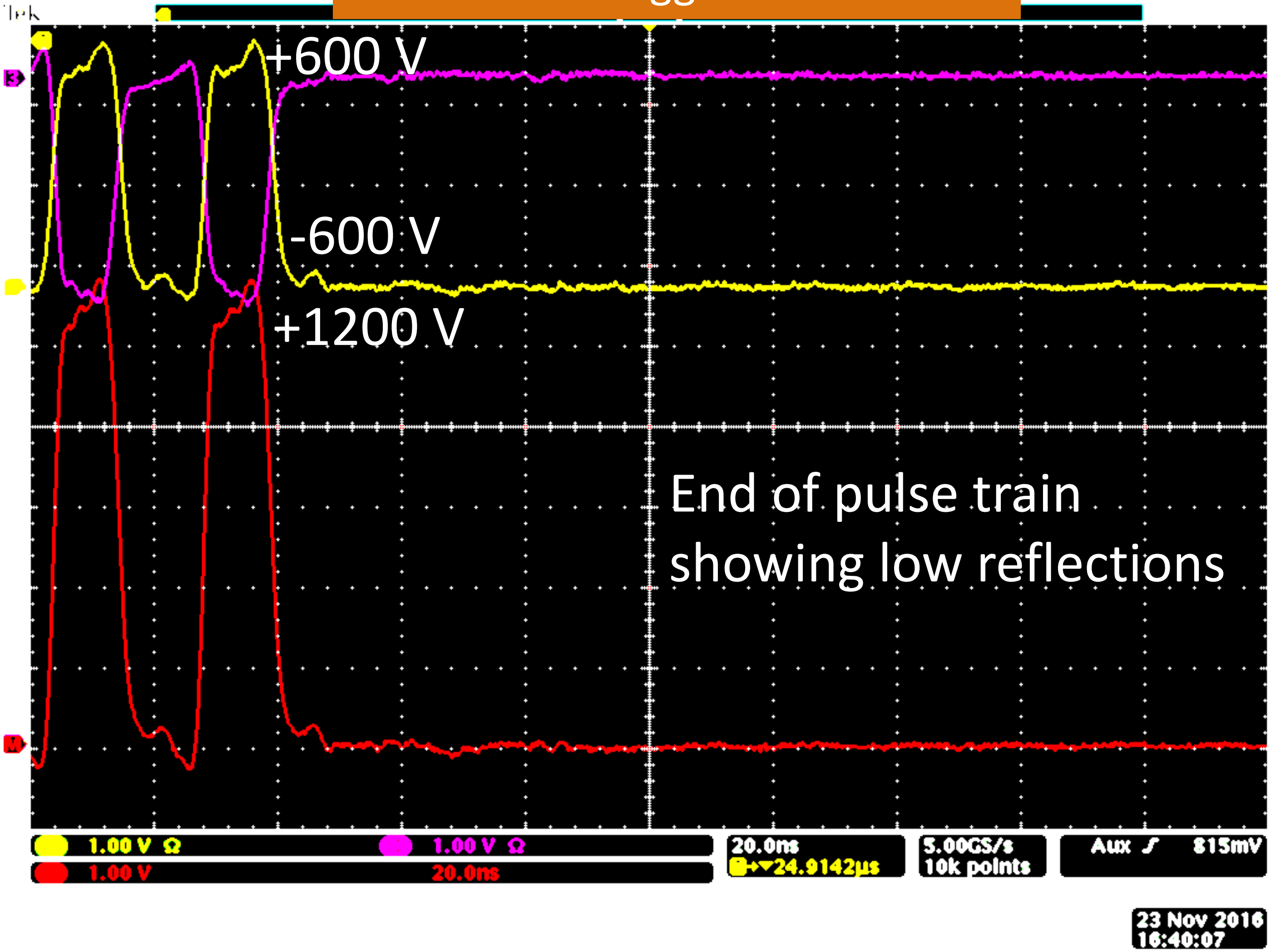
Vertical
≈ 220 V /div

Horizontal:
10 ns /div

Amplitudes are consistent up to 40 µs bursts at 81.25 MHz

Switching at 40.625 MHz, ±600 V; kick 2 pass 2

Transformer-triggered switches



+600 V

-600 V

+1200 V

End of pulse train showing low reflections

Through-voltages

Upper Helix

Lower Helix

Difference Voltage

Vertical
≈ 220 V /div

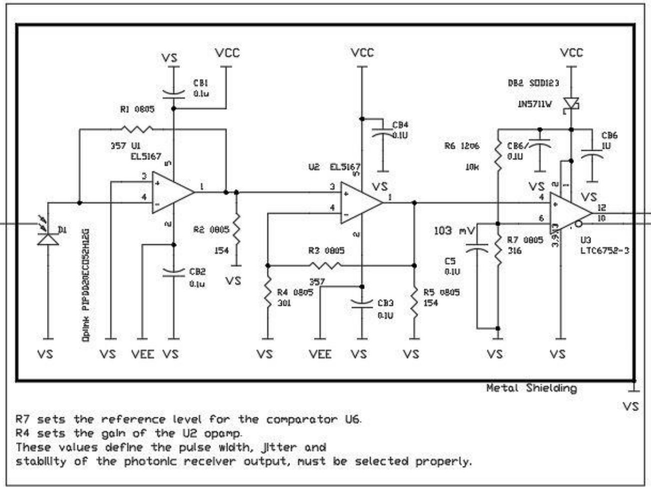
Horizontal:
20 ns /div

Remaining Design Issues – all straight forward

- Design MEBT Kicker instrumentation interface
- Upgrade GaN FET gate driver stage
- Improve GaNFET PCB layout
  - In-line not in a loop
- Mount switch driver circuits against the feed-throughs
  - No coax
- Design mechanical mounting
  - Drivers
  - Loads
- Address operating voltage limitation
  - Operating voltage now limited to 500 Vdc

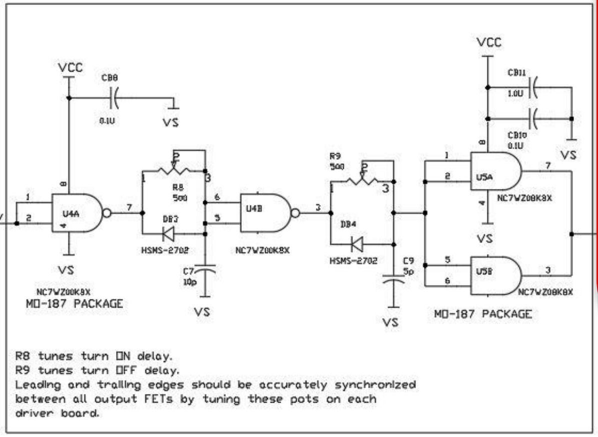
Upgrade GaN FET Driver Stage

Detector Stage



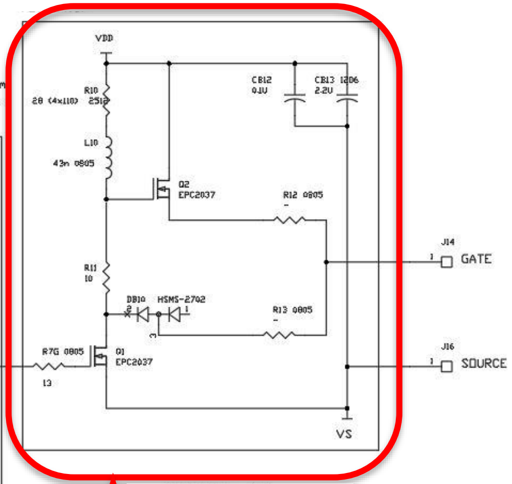
R7 sets the reference level for the comparator U6.
R4 sets the gain of the U2 opamp.
These values define the pulse width, jitter and stability of the photonic receiver output, must be selected properly.

Delay Tuning Stage



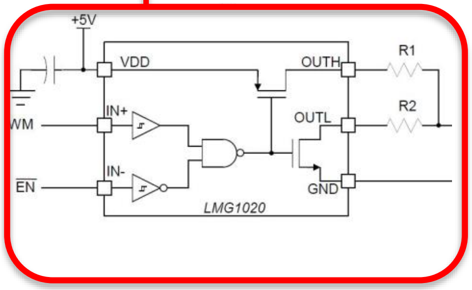
R8 tunes turn ON delay.
R9 tunes turn OFF delay.
Leading and trailing edges should be accurately synchronized between all output FETs by tuning these pots on each driver board.

GaNFET Gate Drive Stage



LMG1020 GaN FET Gate Driver

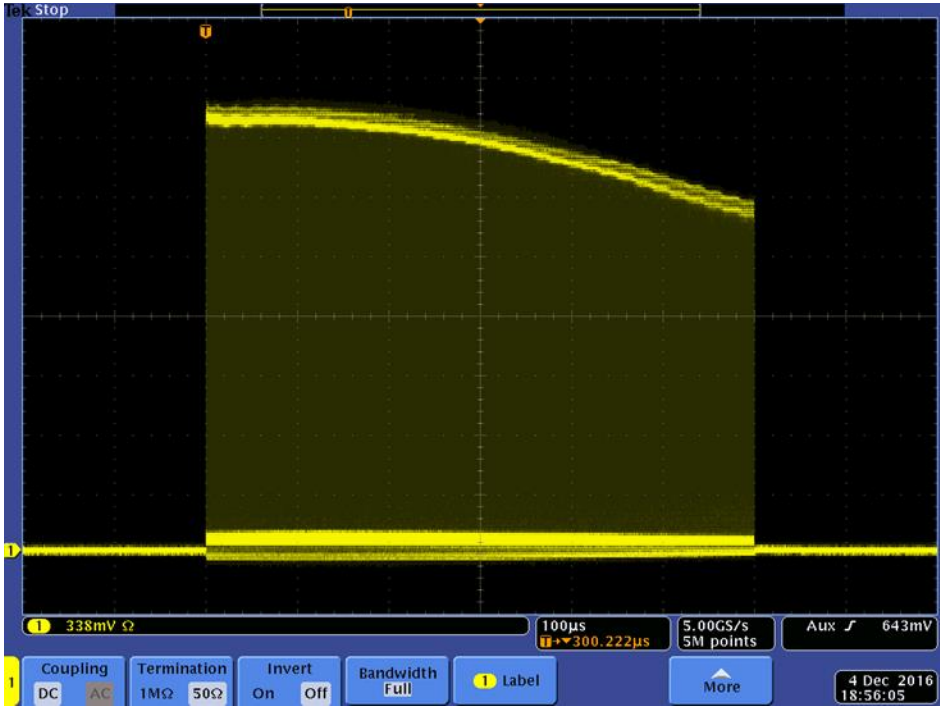
0.4 ns Trise/fall into 100pF
1 ns pulse width
7A source, 5A sink currents
60 MHz CW rep rate



- Eliminates inductor performance compromise
- Circuit power reduced from 1.25W to 0.1W
  - Forced-air cooling needed to prevent turn-on and –off timing shifts
- Enables reducing PCB size & decrease Driver Circuit parasitics-to-everything

Operating Voltage Limitation

- Problem is an average power dissipation issue
  - Operating voltage envelope sags during the 550 μs
- FET gate threshold voltage is temperature dependent
  - Junction temperatures are not matched
  - FET timing diverges at junction temperatures about 70 ºC (absolute)
- Switches do not break;
  FETs recover



Cooling enhancement options for >530 V operation

- 5% added to 528 V = 550 V providing desirable margin
- Option 1: build 4-FET switches instead of 3-FET
  - Total switch power dissipation remains roughly the same
  - Per-FET power dissipation would be less
- Option 2: mount GaN FETs on AlO_2 ceramic substrate
  - Cost estimate is ~$1800 for 10 substrates
- Option 3: improve cooling on existing G10 PCB
  - Increase air flow rate
  - Added small radiators on PCB bottom side

Summary

- A 200 Ω kicker lowers power dissipation everywhere and made it possible to develop a switch-driver and achieve bunch-by-bunch chopping
  - Even for only Booster delivery with its 550 μs macro bunches, 0.5 MHz average rep rates
  - Current helix design will simply be replicated for two kickers
- Both switch driver versions operated with beam at PIP2-IT demonstrated inherent multi-FET switch capabilities:
  - Switching speed to kick and pass bunch-by-bunch
  - Operation at and above 500 Vdc bias
  - To switch at Booster average 45 MHz switching rate
  - Operation at 81.25 MHz for 10’s of microseconds at 20 Hz
- Photonic trigger system proved crucial
  - Allows delivery of the arbitrary waveform for Booster injection
  - Provides fine temporal adjustment of on/off delay as well as pulse width
- 4-month test proved GaN FET reliability despite junction thermal cycling
- There are a number of options to improve cooling and allow operation >530 Vdc bias

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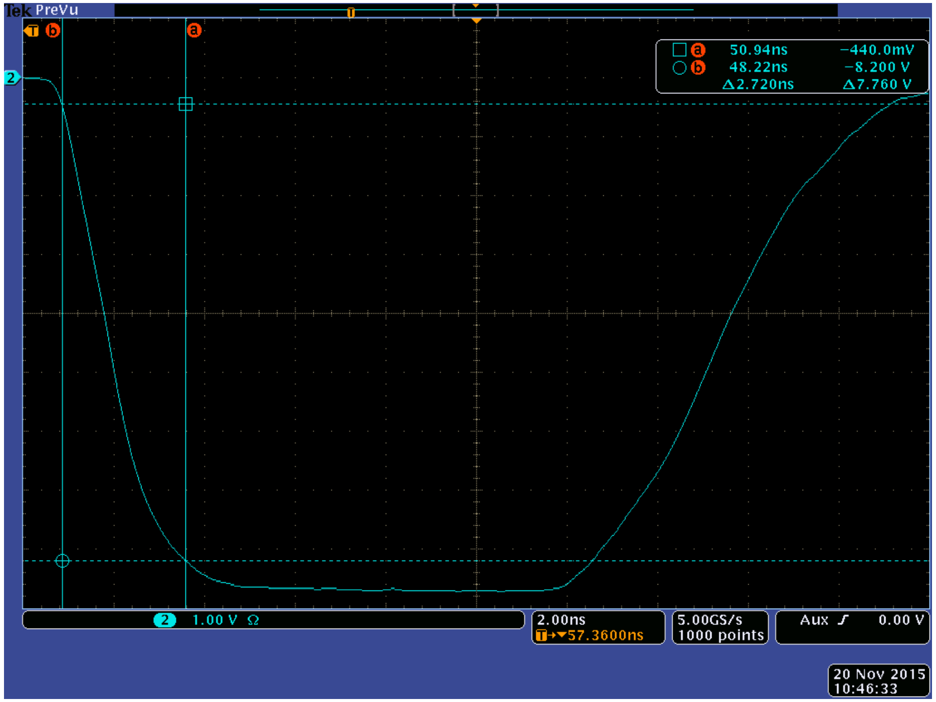
END

Issues regarding high rep-rate multi-FET switch

- Switching losses at megahertz rates dominate FET dissipation
- Solution: transition faster (for example: well below 2 ns rise/fall)
  - Lowers FET dissipation
  - Increases difficulty of setting and maintaining synchronous timing match
- Reality of mismatched FETs
  - FETs originally timed close (+/- 100ps)
    - Tuned for ~2 ns turn-on time (5-95%)
    - They will be sharing to a significant degree even if we can measure differences in temp.
  - GaN FET rating is 650V
    - They won’t break even if grossly mismatched (we’ve demonstrated this)
  - Mismatch problem is timing shift not thermal melt-down
    - Timing shifts occur at ~70ºC junction
  - How many FETs in series to use?
    - 1 FET or 2 FETs not enough
    - 3 or 4 both work
- Real issue is to provide enough substrate cooling for average power

Switch turn-on/-off time difference without output compensation

Turn-on = 2.72 ns



Turn-off = 6.58 ns