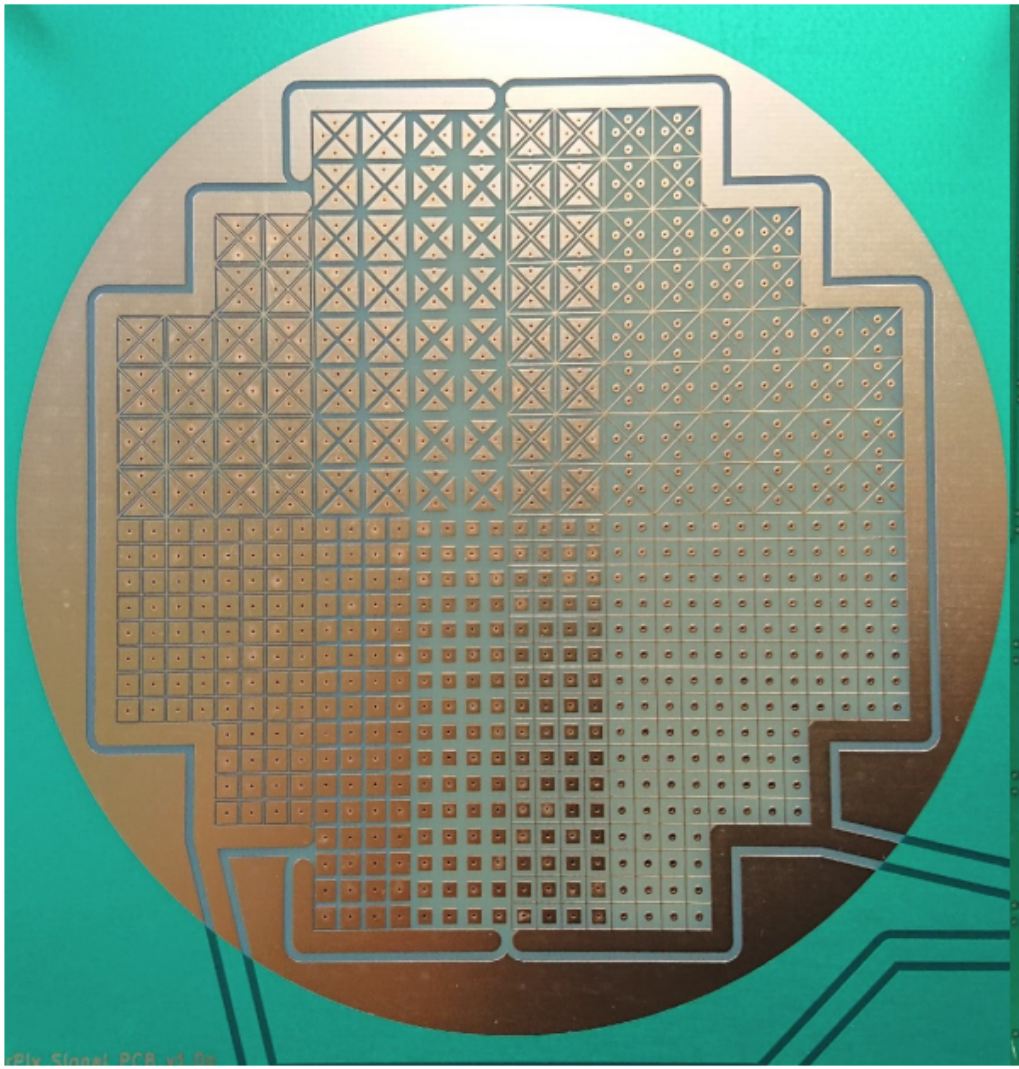
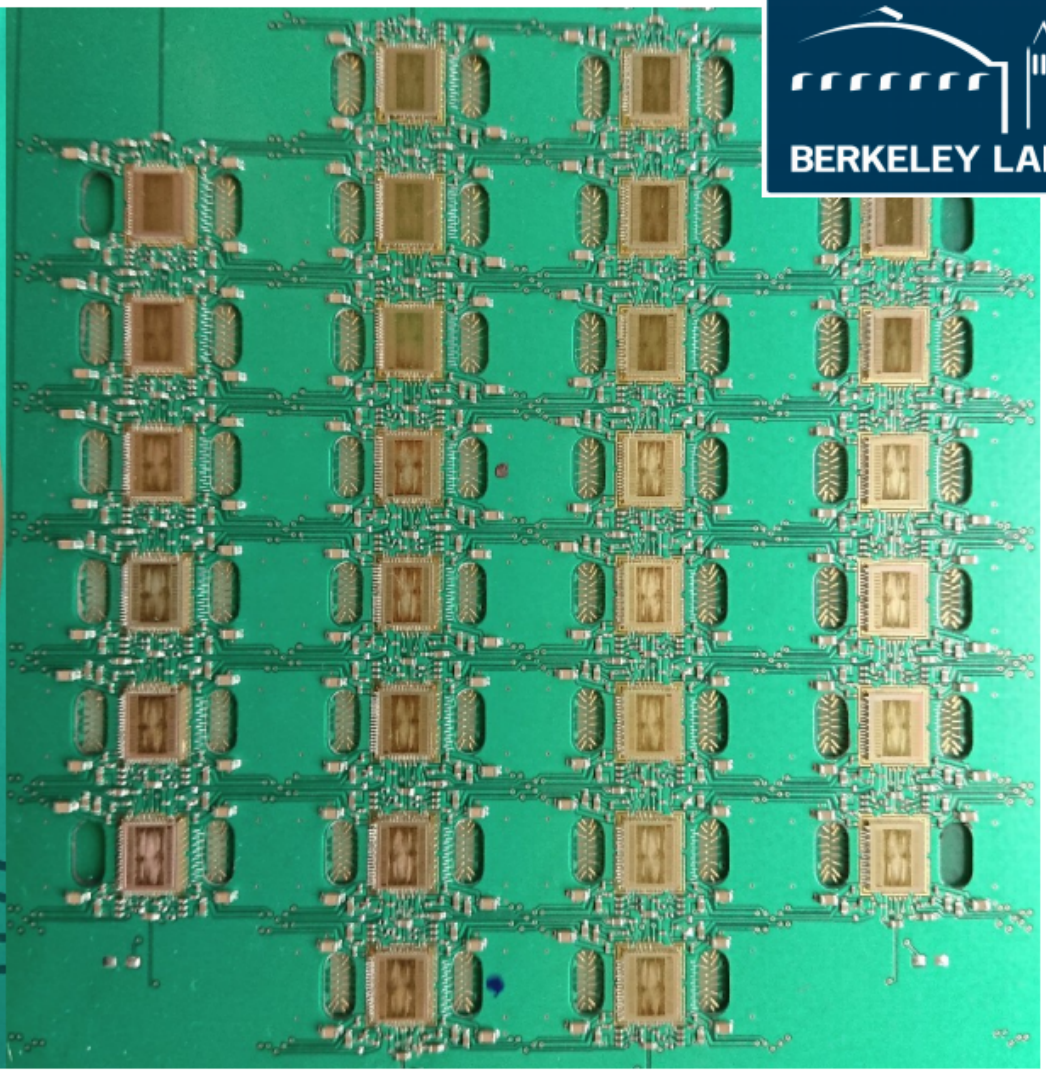
LBNL/Bern Pixel Status and Prospects





Jonathan Asaadi
University of Texas at Arlington

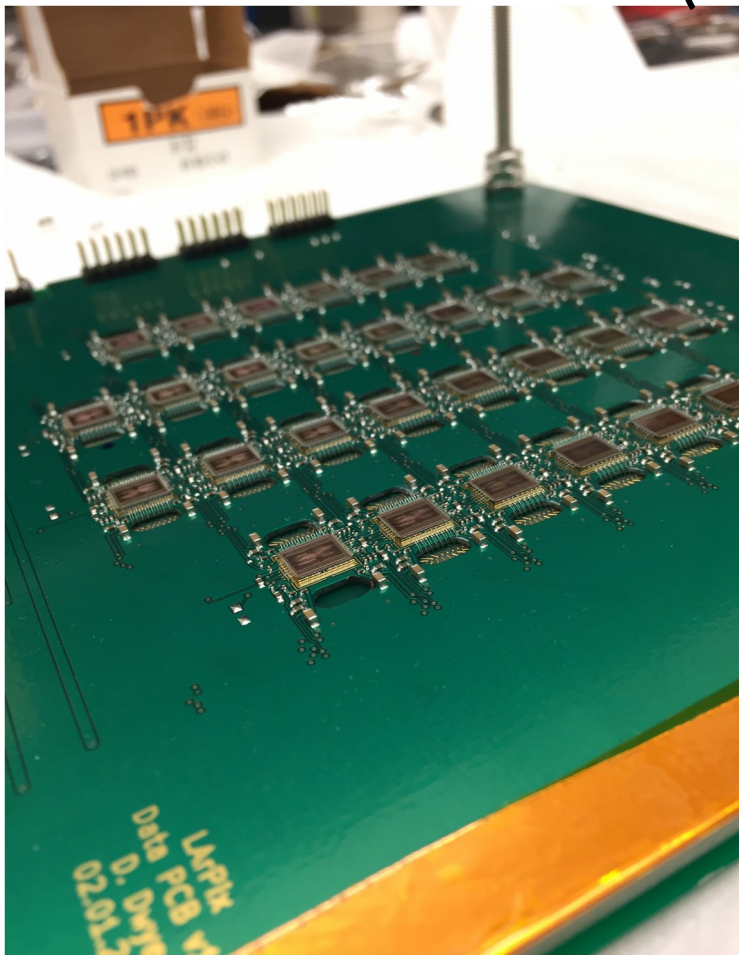
Talk in two parts

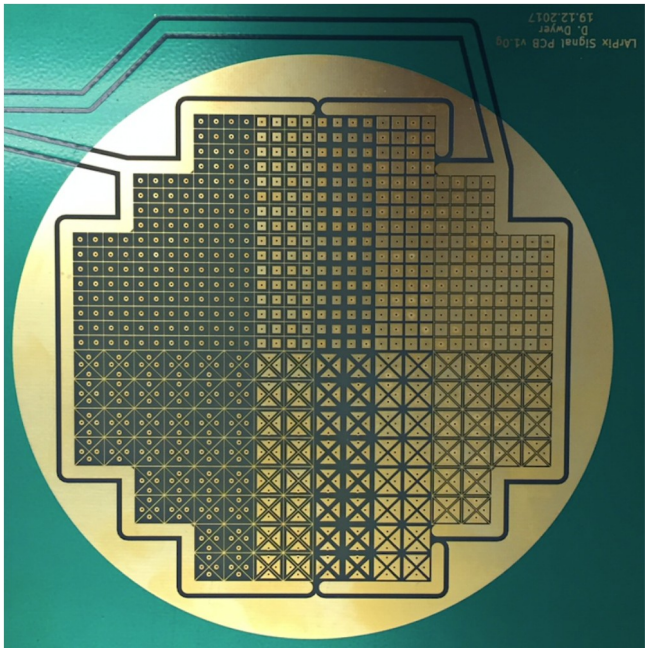
- **Demonstration of a true 3D micro-power readout for liquid argon time-projection chambers (LArPix)**
  - Talk on behalf of Dan Dwyer

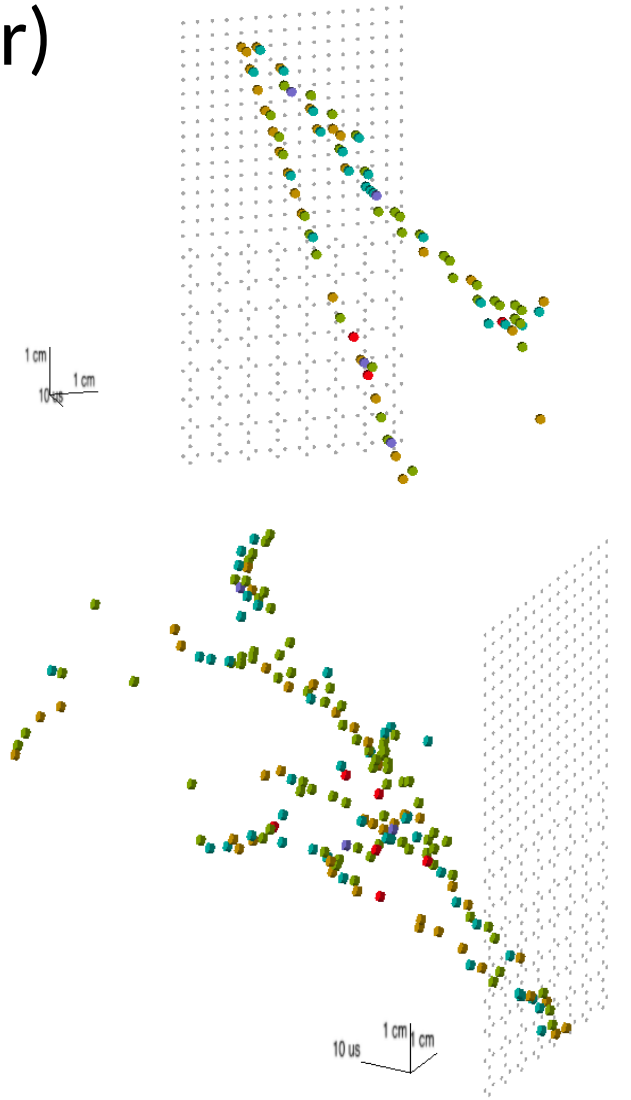
- **Recent and future tests**
  - Tests at Bern and FNAL

Demonstration of a true 3D micro-power readout for liquid argon time-projection chambers

(on behalf of Dan Dwyer)





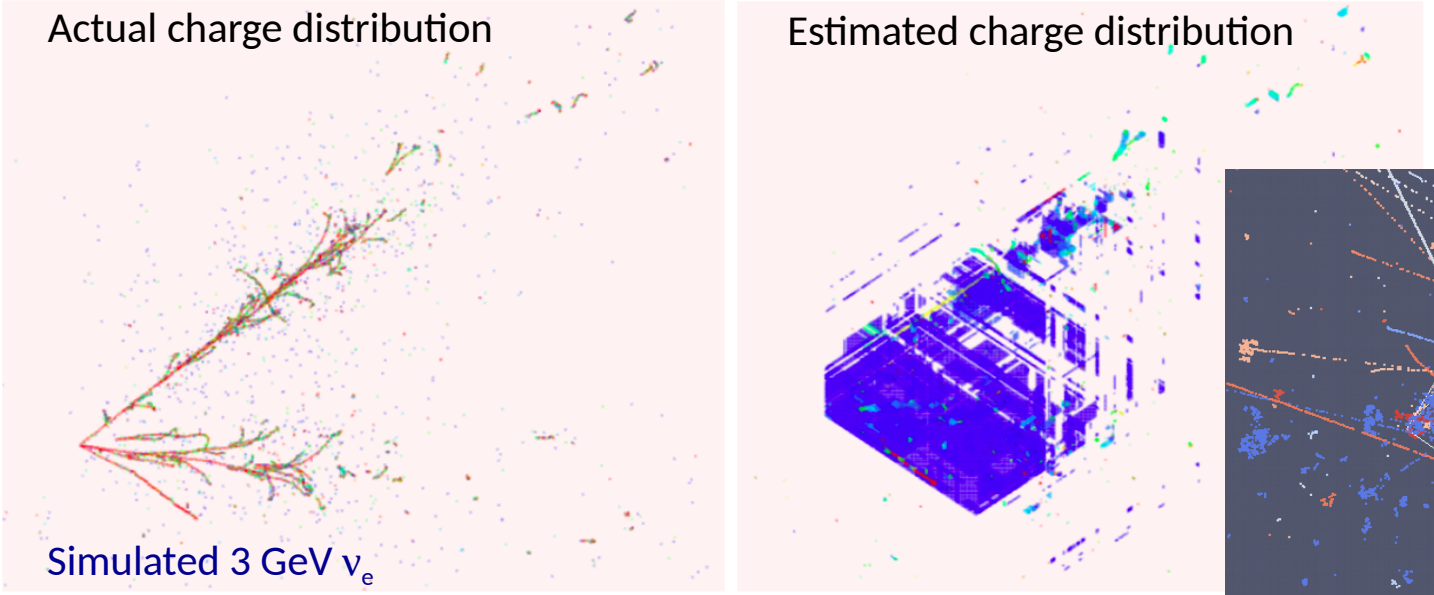


Caveat

- **Dan was unable to join the meeting today, but agreed to have some of his material presented here**
  - I am here to parrot some of his more recent presentations
- **All credit for the work shown here belongs to Dan and the LBNL team**
  - I am a collaborator with Dan on the ArgonCube project as part of the DUNE Near Detector
- **Recent paper posted to the arXiv with lots of details**
  - LArPix: Demonstration of low-power 3D pixelated charge readout for liquid argon time projection chambers (arXiv: 1808.02969)

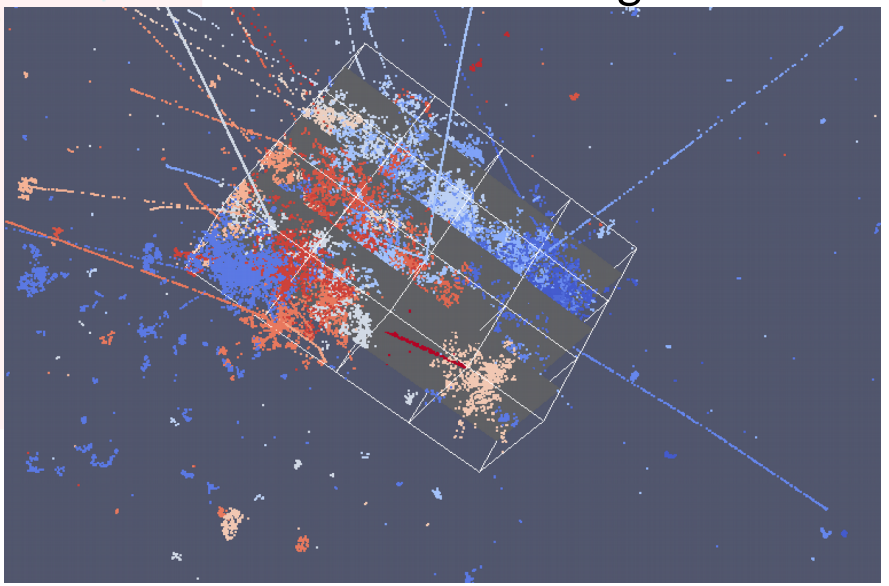
3D LArTPC: Motivation

Ambiguities in projective wire readout:



DUNE Near LArTPC:

High neutrino rate exacerbates ambiguities.



Example neutrino signals from one LBNF spill

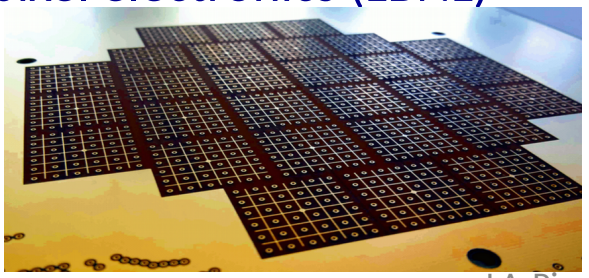
Pixel Readout Development

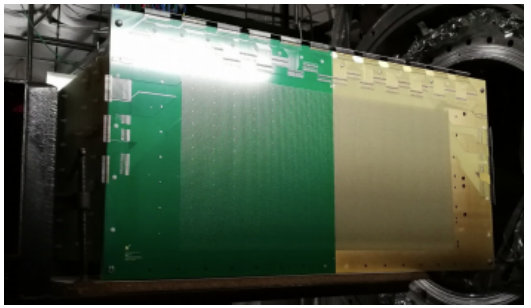
Demonstration of pixel sensor feasibility (Bern/ArgonCube)

Progress with in-beam tests (PixLAr)

→ Low-power pixel electronics (LBNL)

ArgonCube



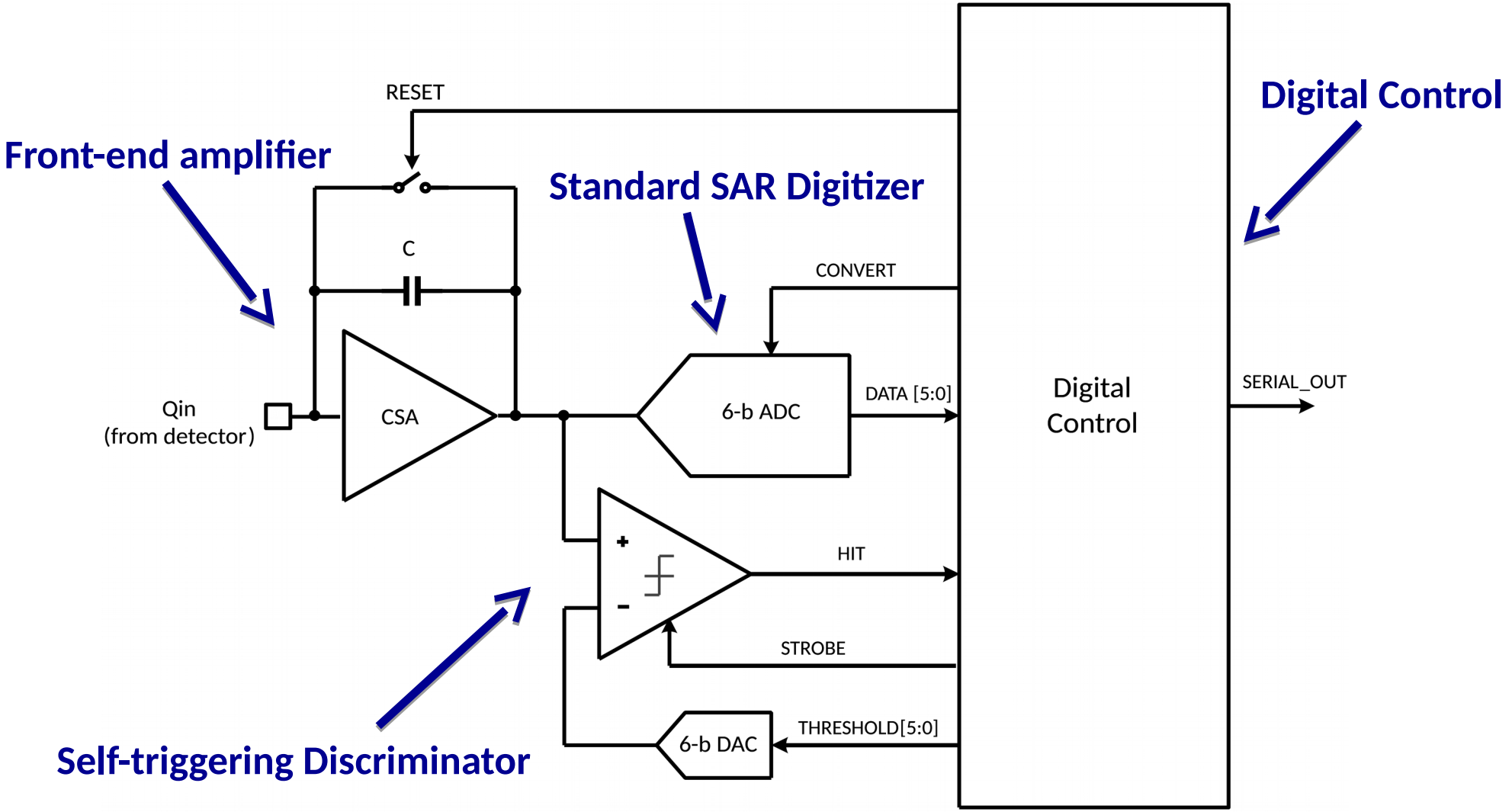


PIXLAR

A LArLAT production

LArPix-v1: Design Concept

Amplifier with Self-triggered Digitization and Readout



Achieve low power: avoid digitization and readout of mostly quiescent data.

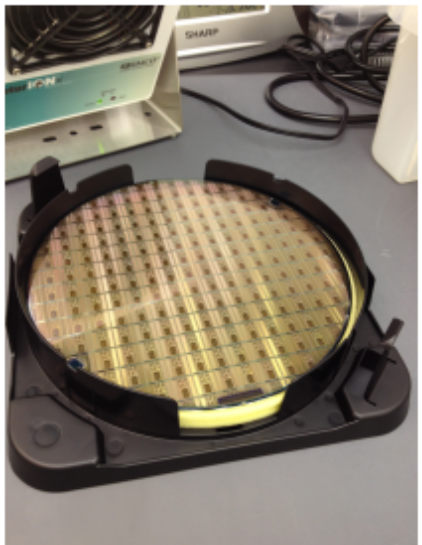
LArPix-v1 Progress

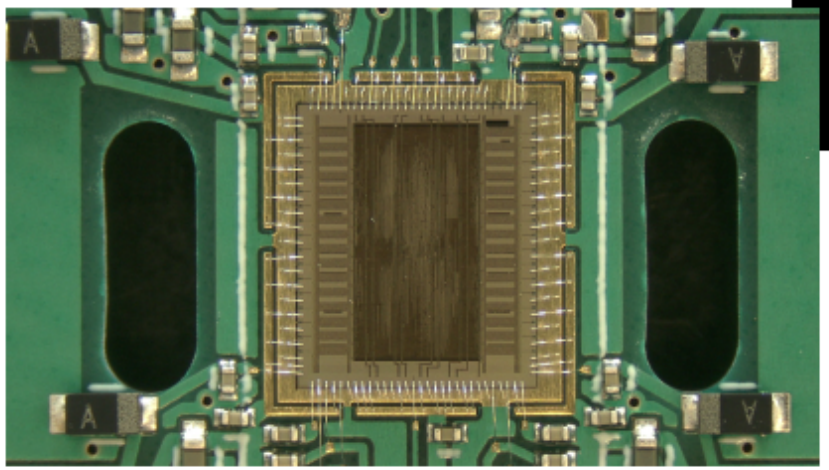
LArPix-v1 ASIC:

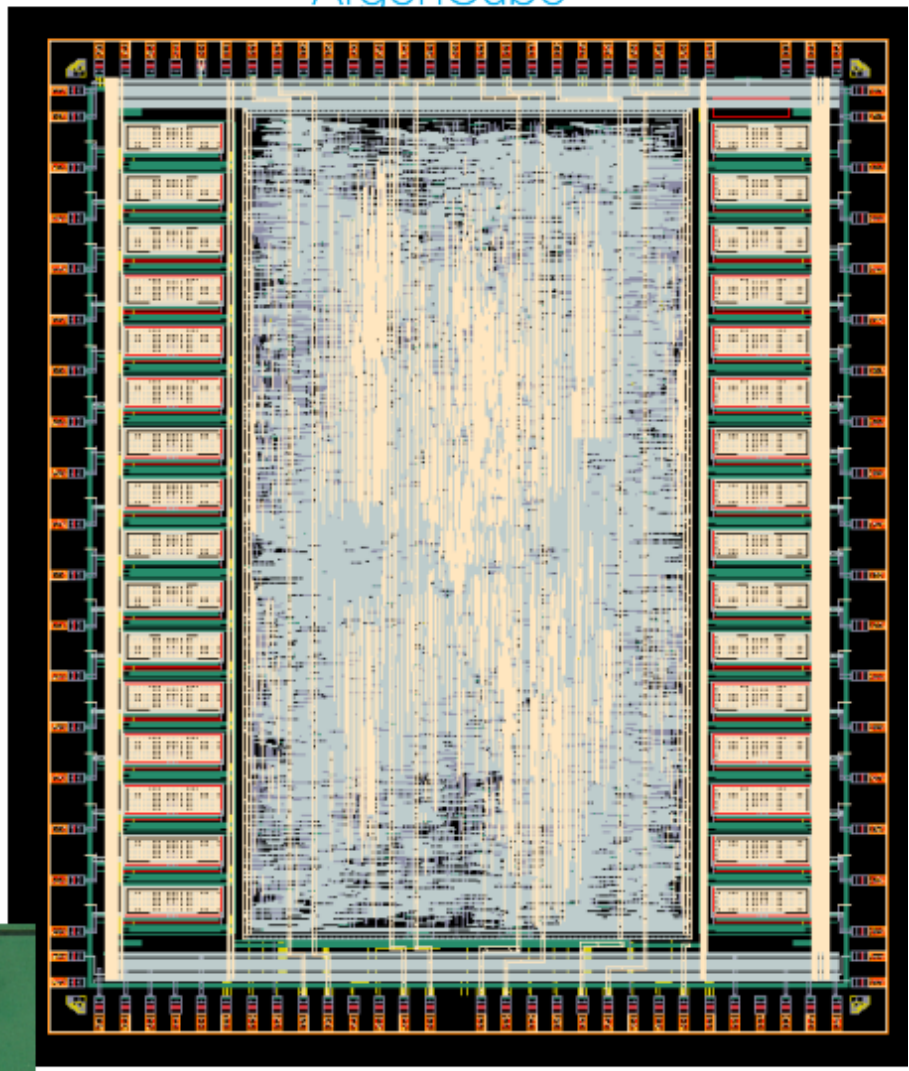
- Dec. 2016: Design began
- June 2017: Submitted for fabrication
- Oct. 2017: First chips, test boards @ LBNL
- Dec. 2017: Bench tests successfully completed
- Jan. 2018: Assembled sensor, integrated LArTPC

Progress

- Feb. 2018: First tracks from true 3D LArTPC @ LBNL
- Mar. 2018: Developed integrated control system
- Apr. 2018: Assembled scalable 512-channel system, operated in 60-cm-drift TPC @ Bern
- May 2018: Operated 832-channel system @ LBNL







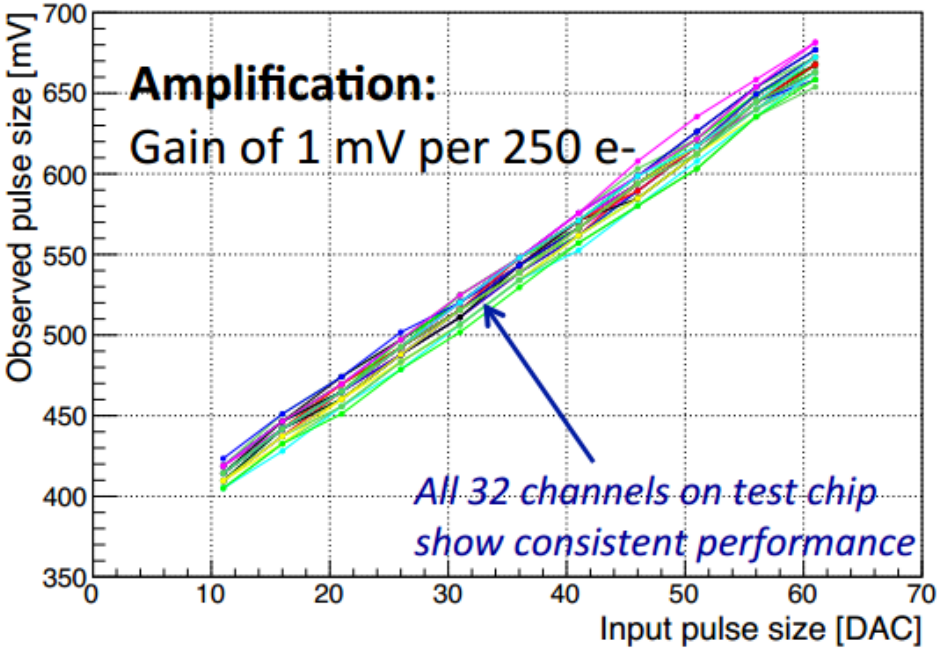
Process: 180nm bulk CMOS

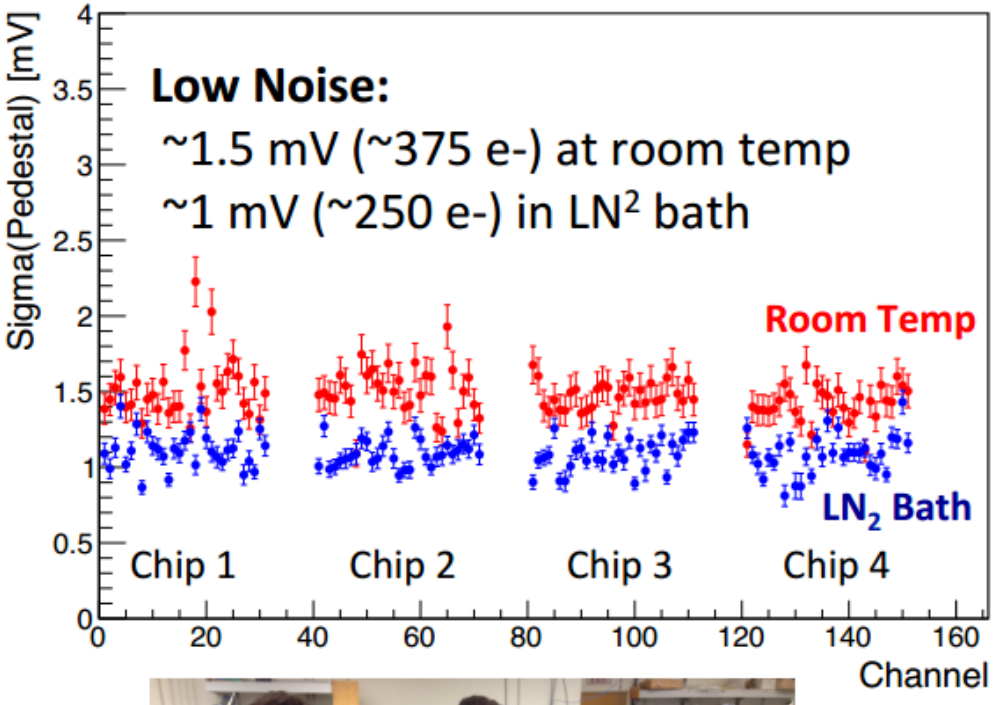
Design and testing team @ LBNL:

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stezelberger, S. Kohn, P. Madigan, H. Steiner

Gain, Noise, Power

Demonstrated low-noise low-power cryogenic amplification, digitization, and readout:



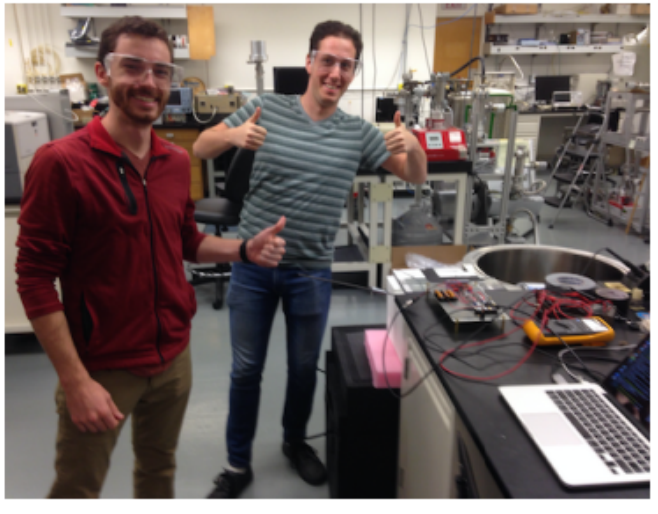


Low Power:

Average power for 128-channel readout:

- Analog: 24 µW/channel
- Digital: 38 µW/channel
- **Total: 62 µW/channel**

See talk from DUNE Collaboration Meeting (January 2018) for more details.



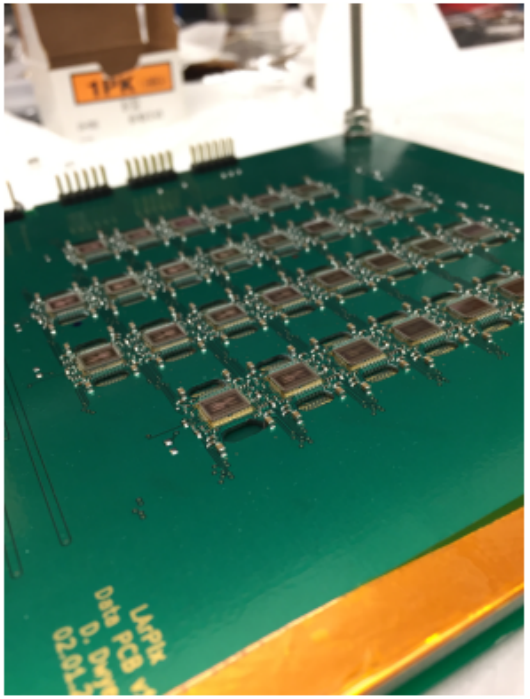
P. Madigan, S. Kohn: drove testing effort

Control System

Developed Prototype Control System:

- Warm electronics for LArPix sensor operation
- Provides power, reference voltages, clock, data I/O, and integrated DAQ system
- Main components:
  - Off-the-shelf Cmod FPGA module ($60): Provides real-time clock, I/O
  - Raspberry Pi Zero ($5): Complete DAQ system, control computer
- Requires: 5V power supply or battery, ~400 mA average current.
- Access via wifi

Pixel system



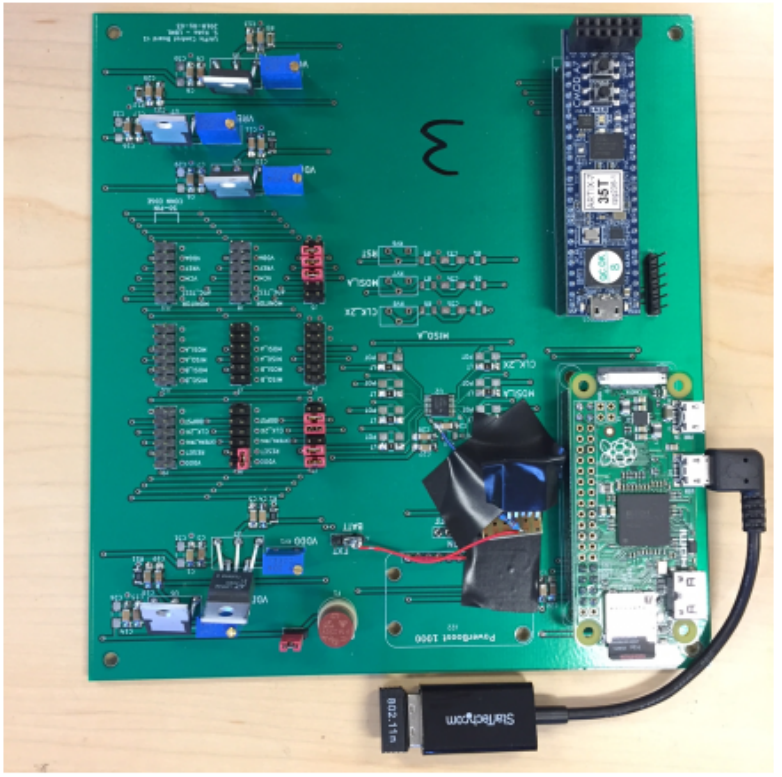
Inside Cryostat

50-pin ribbon cable

Existing layout should scale to ~8000 pixels.

With minor changes to FPGA firmware and PCBs, should support up to ~10^5 pixels.

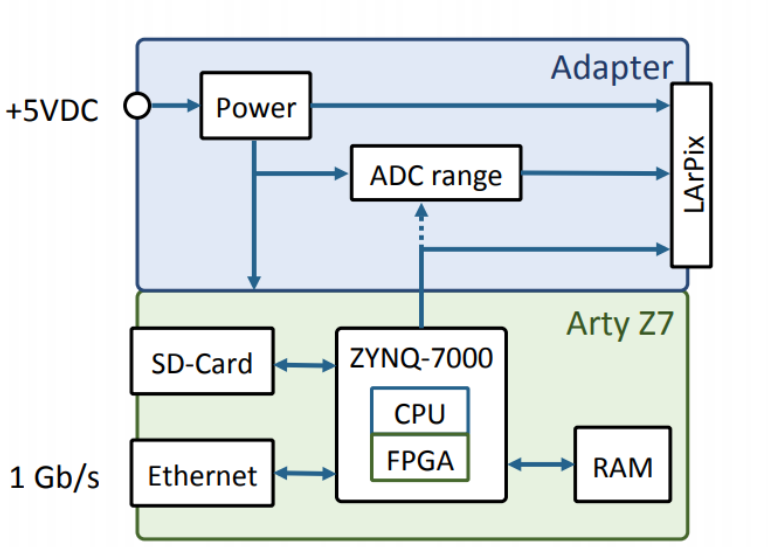
Control System



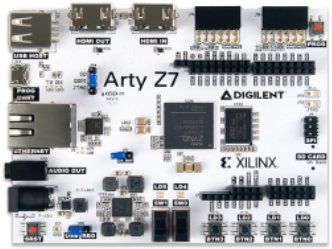
Outside Cryostat

Updates:

- **Exploration of a different readout box using a commercial FPGA front end board has been underway from University of Bern**
  - Using an Arty Z7 board
  - Initial tests look very promising as a low cost front end board to read the LArPix data
  - Seems scalable to larger pixel readout
  - Testing continues at University of Bern in collaboration with LBNL group

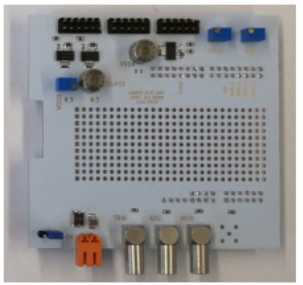


Arty Z7



- ZYNQ-7000
  - FPGA
  - Dual ARM Cortex A9
- Ethernet (1Gps)
- microSD slot

Adapter



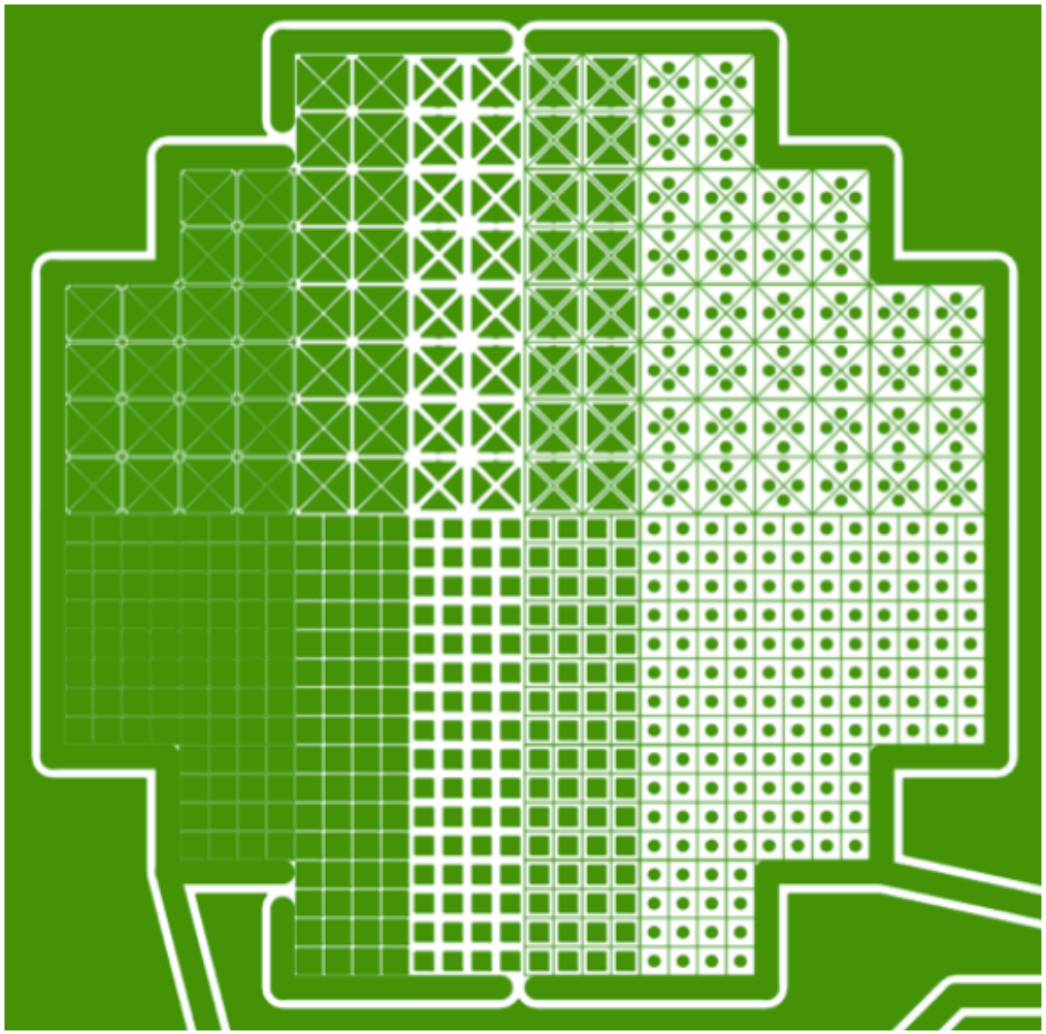
- Power
- Analog lines
- Digital data lines (2 daisy chains)

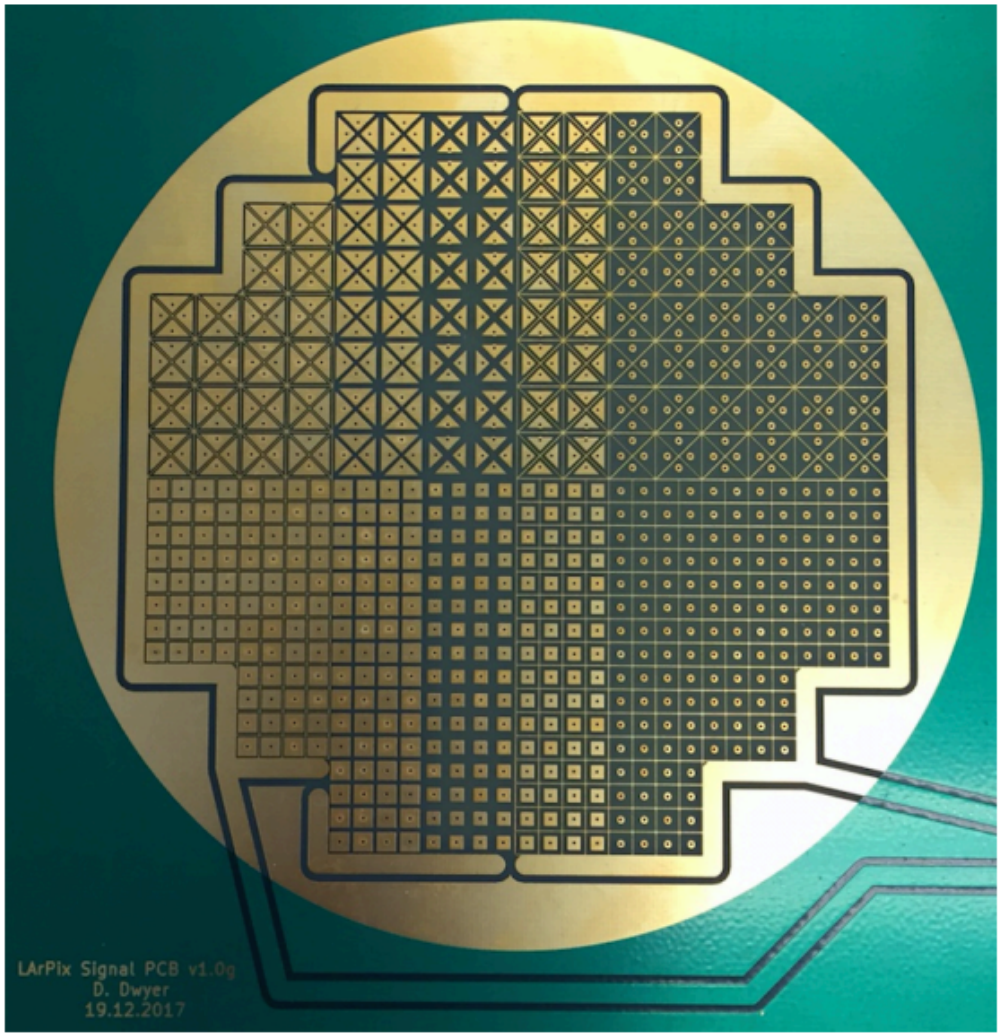
Pixel Prototypes

Prototyped a variety of pixel geometries

Sensor PCB board designed to fit Bern Pixel Demonstrator TPC

Includes 10 different pixel geometries/configurations



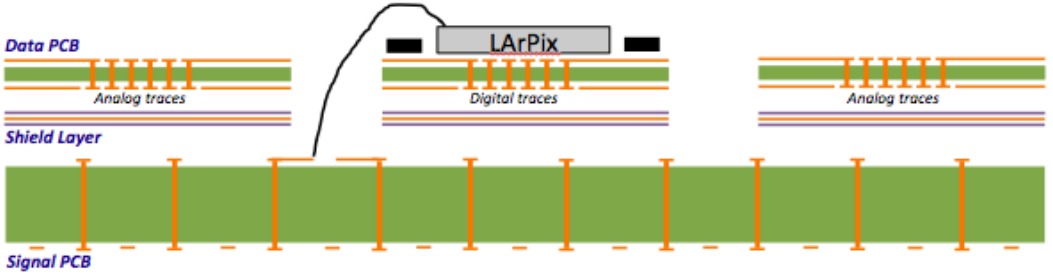


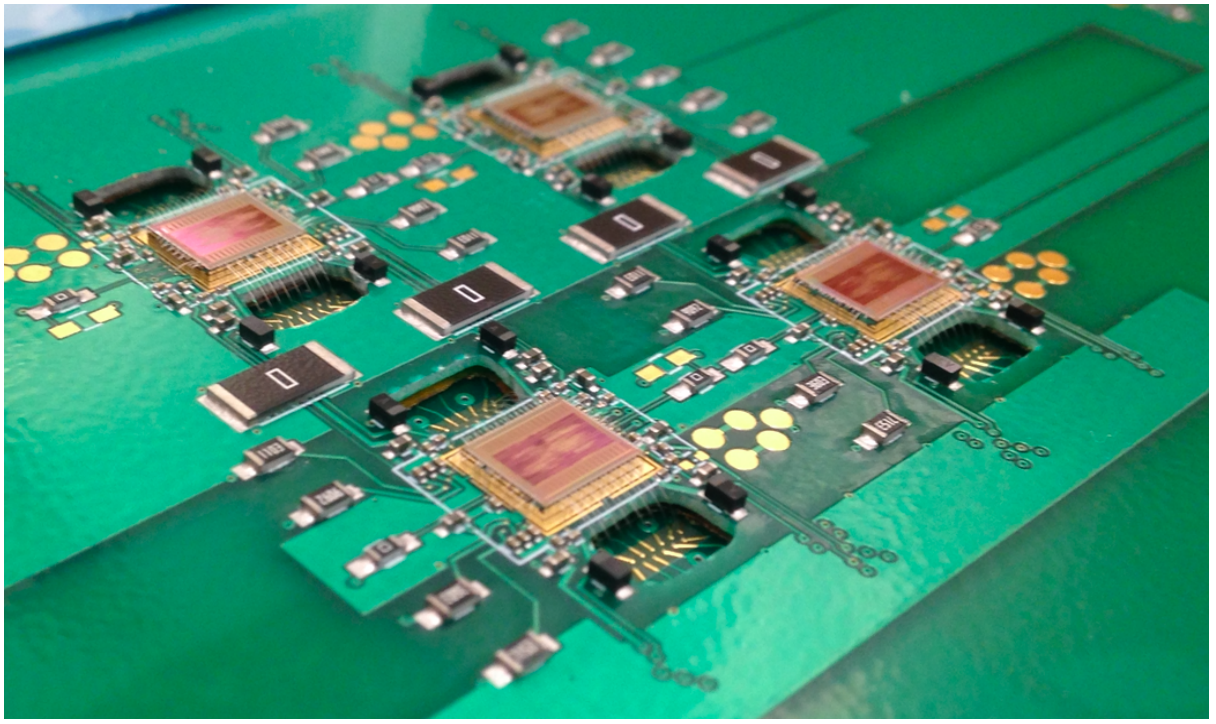
LArPix-v1: Sensor Assembly

LArPix data board attached to sensor board

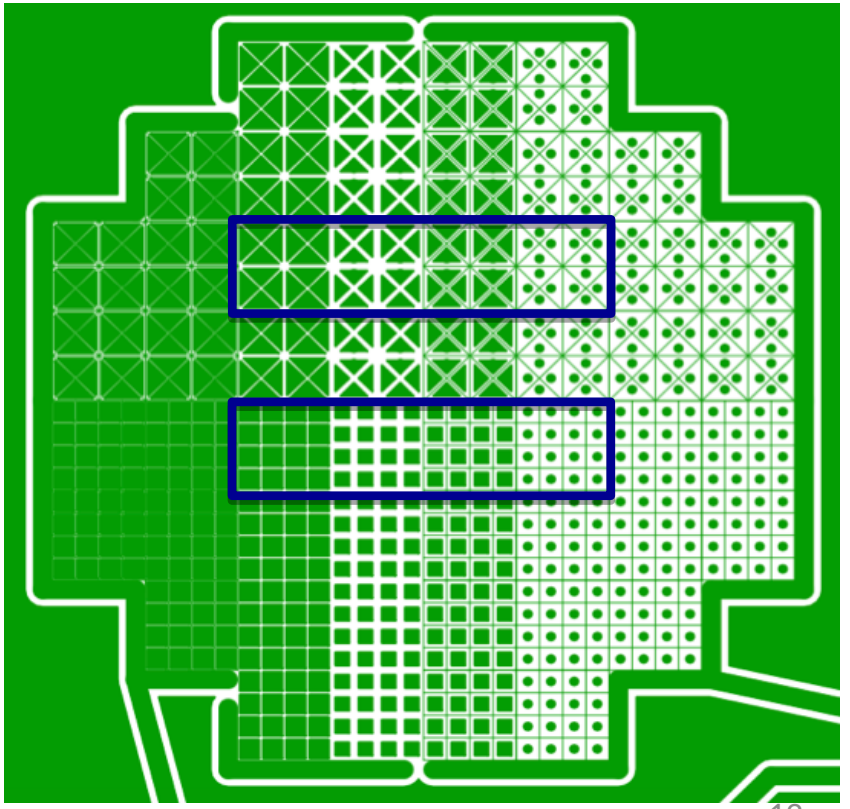
Careful consideration of system grounding and routing for low-noise operation

First test: 128-chip data board used to partially instrument pixel readout plane

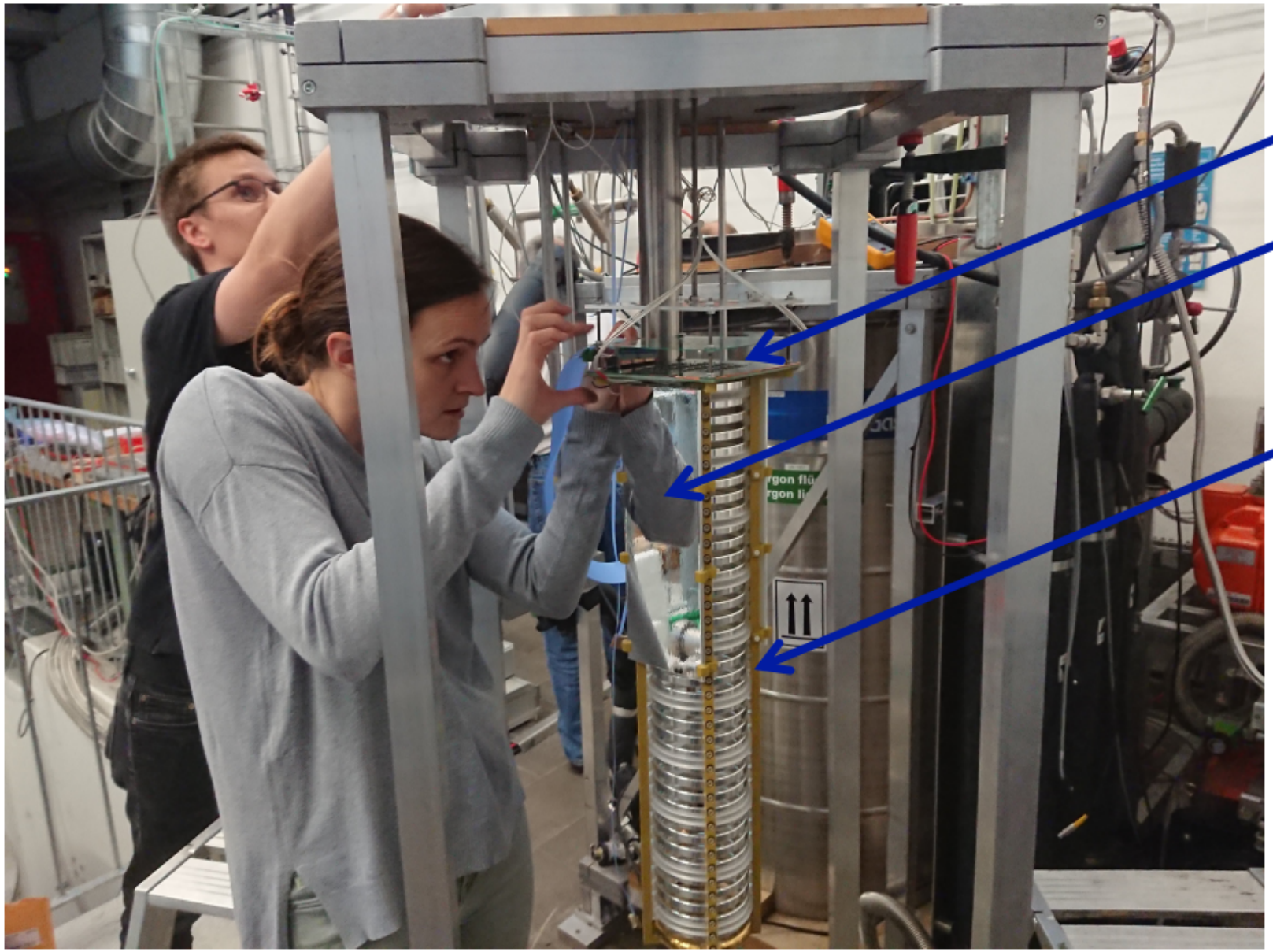




Instrumented regions during initial tests

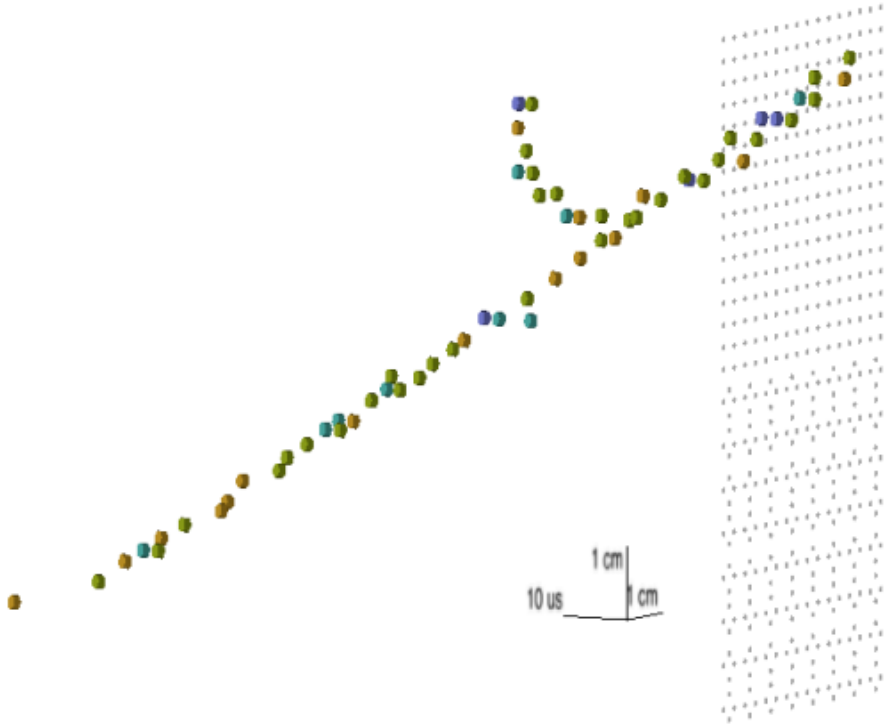


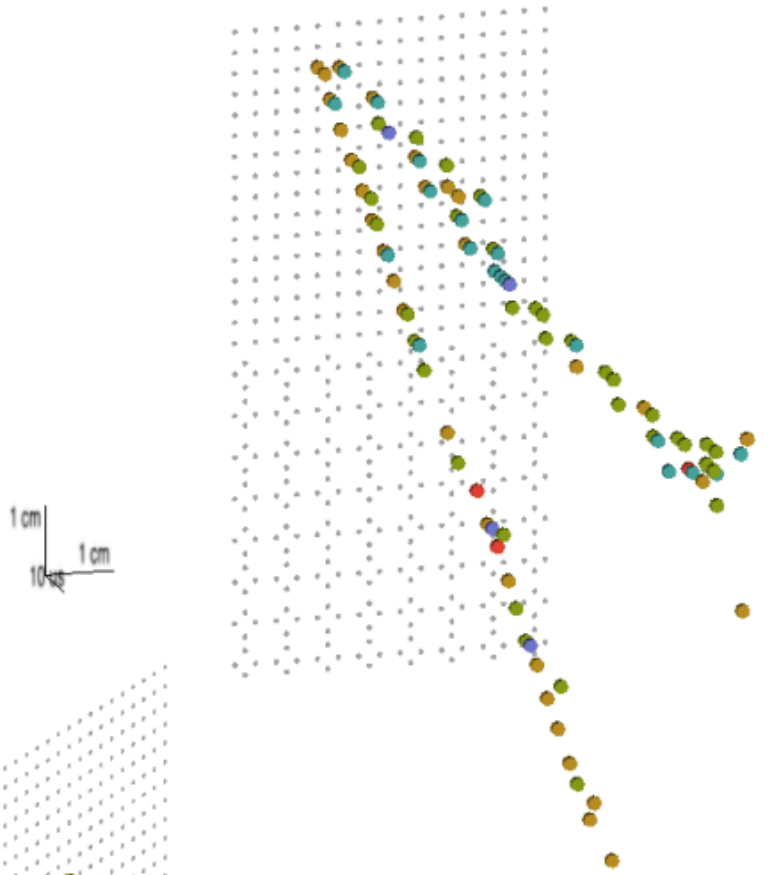
512-channel @ Bern



512-channel @ Bern

Slightly more interesting topologies

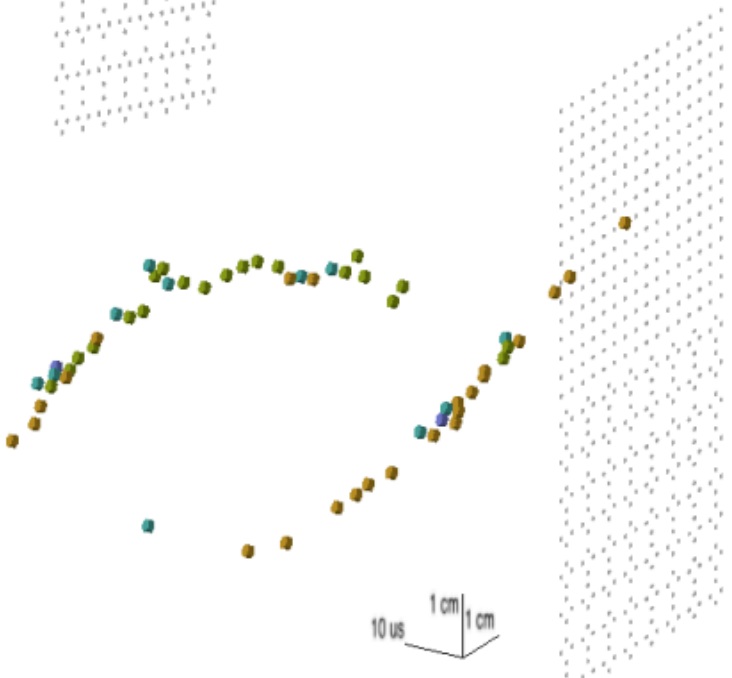




Straight MIP (at 45° to sensor):
35 ± 5 ADC (over pedestal)

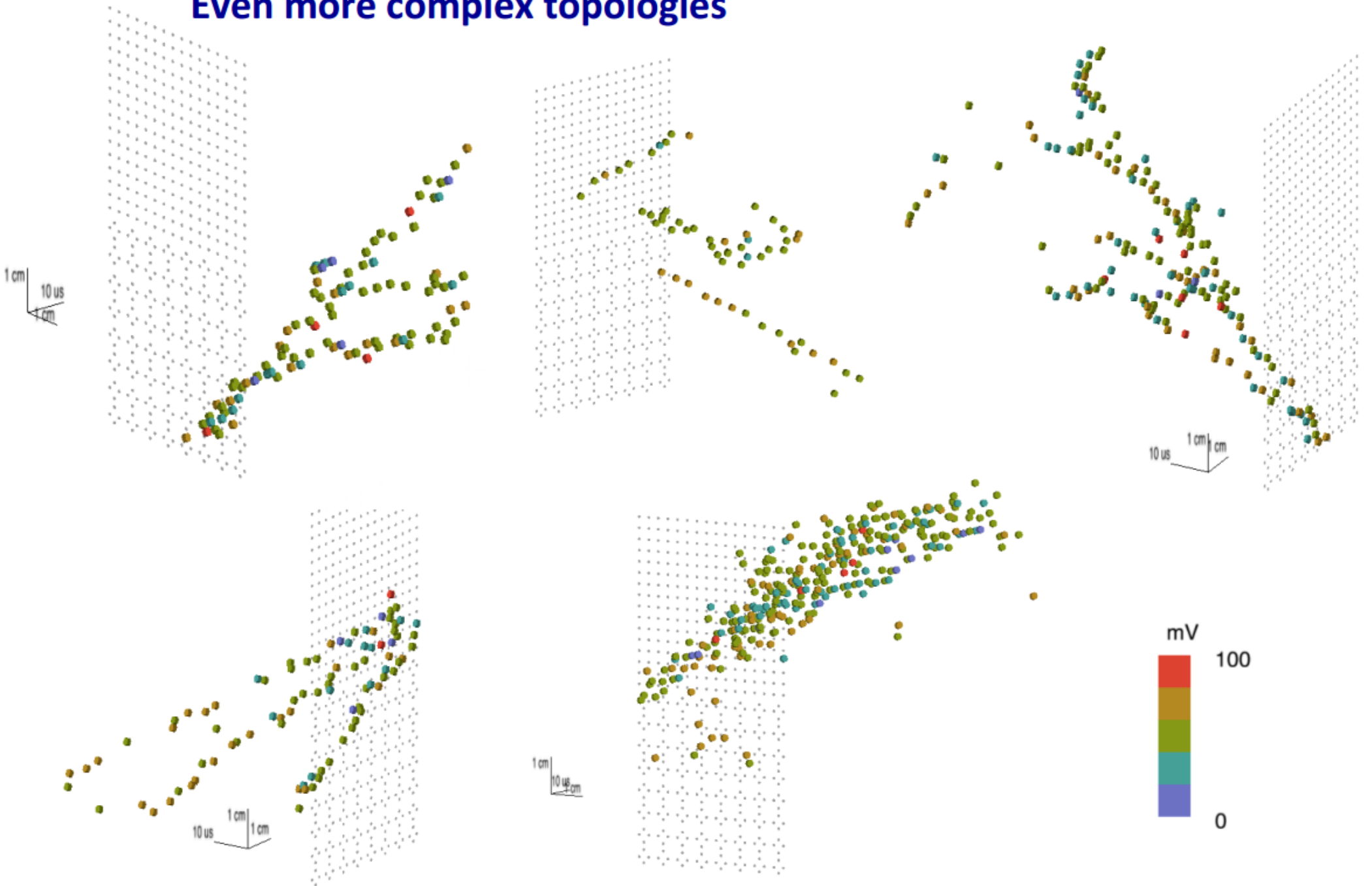
Noise:
2 ± 0.5 ADC

S/N Ratio:
17 ± 3 ADC



512-channel @ Bern

Even more complex topologies



Next Steps

Characterization of pixelated readout:

1) Establish calibration techniques
2) Comparison of performance of pixel types
   → Will determine the design for version 2 of Pixel Readout PCB
3) Assess performance of LArPix triggering and readout
   → Will motivate targets for LArPix version 2 ASIC design

Near-term system revisions: targeting improved prototype system

1) v2 Readout PCB:
   - Improve isolation between pixel inputs and digital activity, facilitate bypassing
   - Intermediate step toward modular readout tile
2) v2 Control Electronics (warm):
   - Work with LHEP to establish scalable (>10^6 pixel) control electronics
   - Stepping-stone to ArgonCube 2x2 control system
3) v2 Control Software:
   - Improve structure of high-level python configuration and control
   - Add flexible interface to low-level hardware communication with LArPix ASICs

Mid-term system revisions: targeting LArIAT, ArgonCube 2x2 Demonstrator

1) v2 LArPix ASIC (see next slide)
2) v3 Readout PCB (see slide after next)

LArPix-v2

Exploring LArPix-v2 for full physics performance:

Simultaneously obtain high resolution and large dynamic range for charge signal

(with LArPix-v1 you can only choose one or the other at a given time)

Make daisy chain I/O robust to chip failure.

Improve hit timestamp: catch rollover and remove jitter.

Reduce input pad voltage requirements.

Improve default configuration settings.

Improve handling of chip ID.

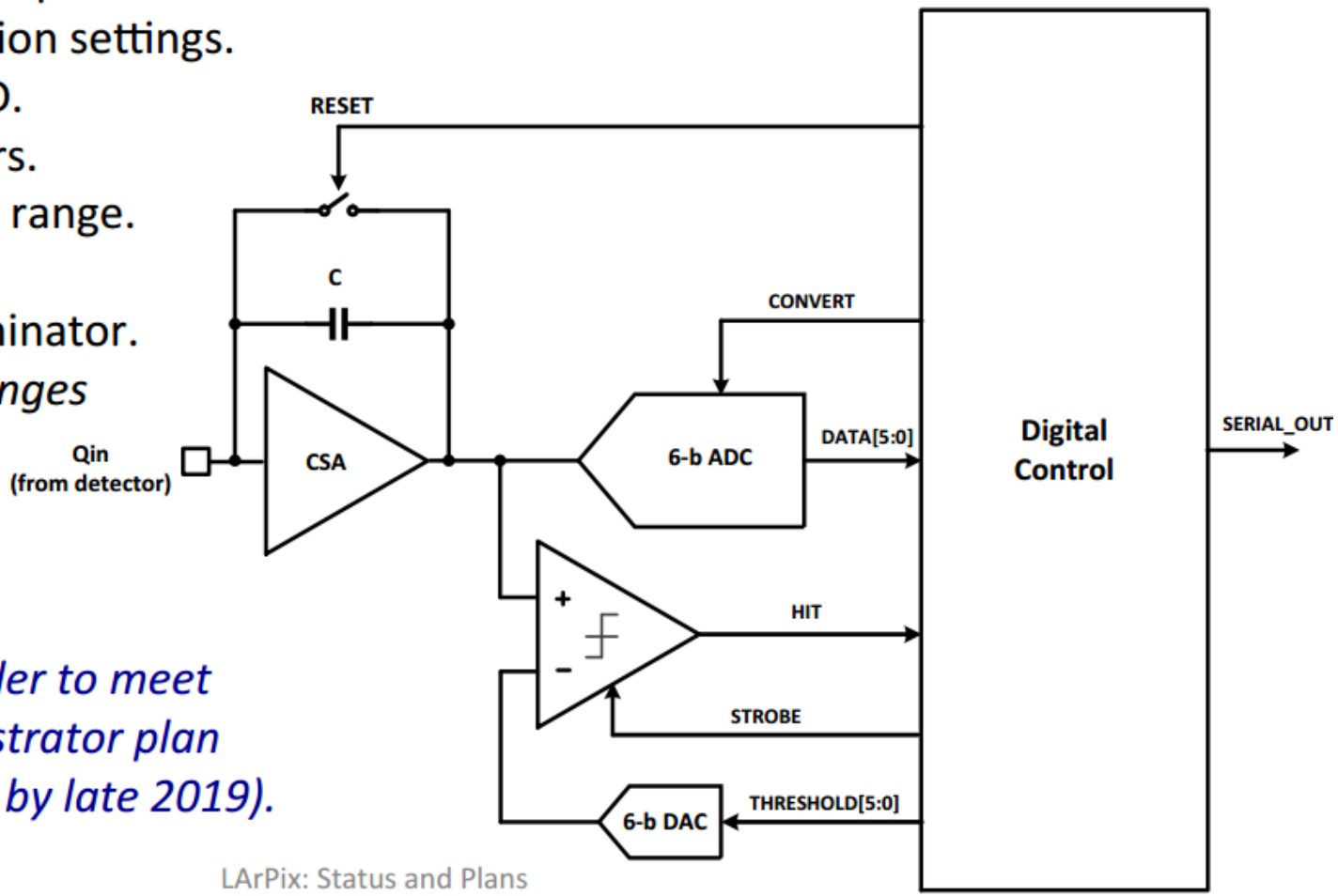
Add internal bias generators.

Increase channel threshold range.

Improve front-end pulser.

Tailor bandwidth of discriminator.

Plus a number of other changes

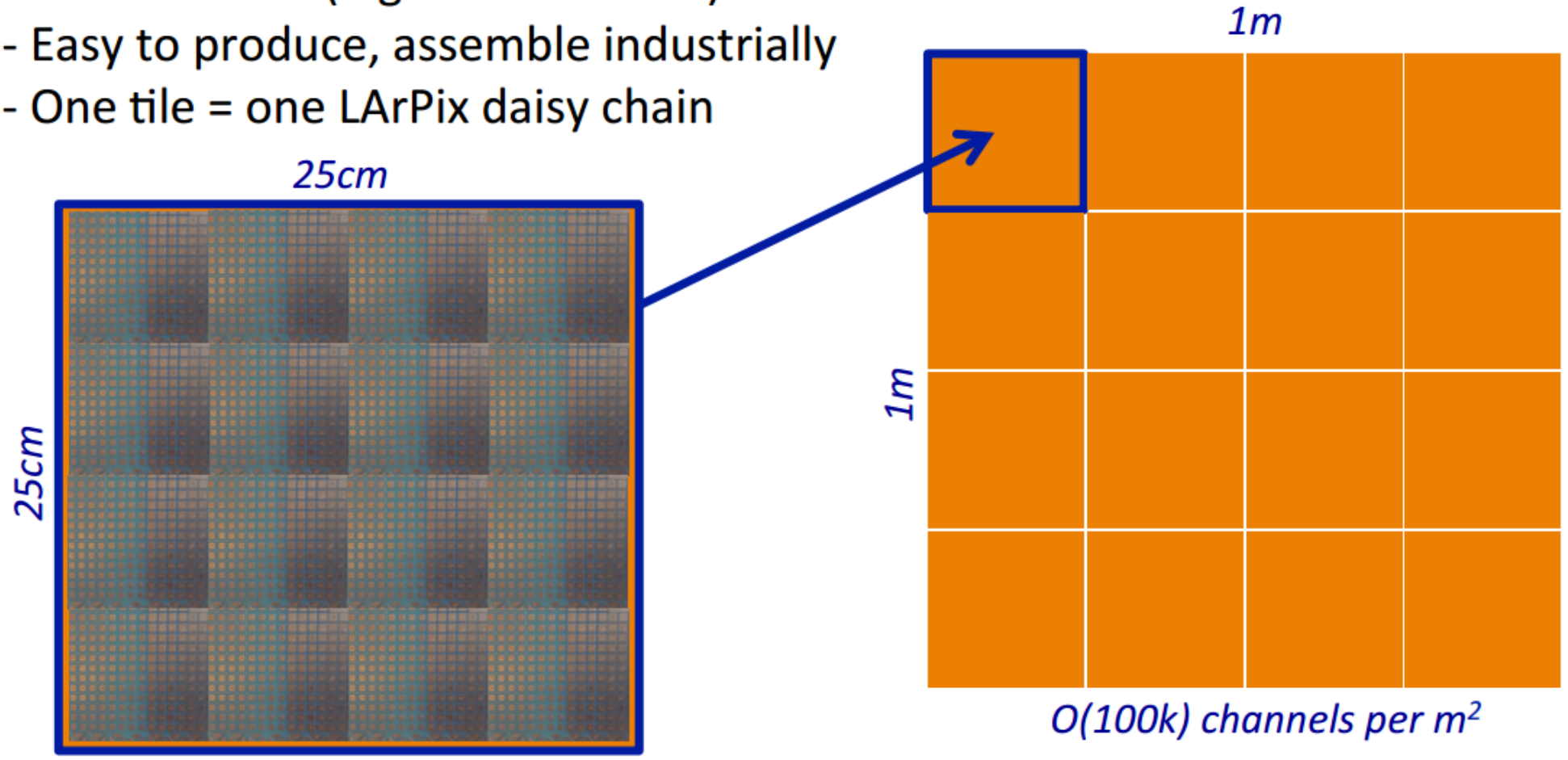


→ *Should start soon in order to meet ArgonCube 2x2 Demonstrator plan (~6 m^2 of readout ready by late 2019).*

Scalability

Design modular pixel tile for instrumenting large area sensors

- Standard size (e.g. 25cm x 25cm)
- Easy to produce, assemble industrially
- One tile = one LArPix daisy chain



Demonstration targets:

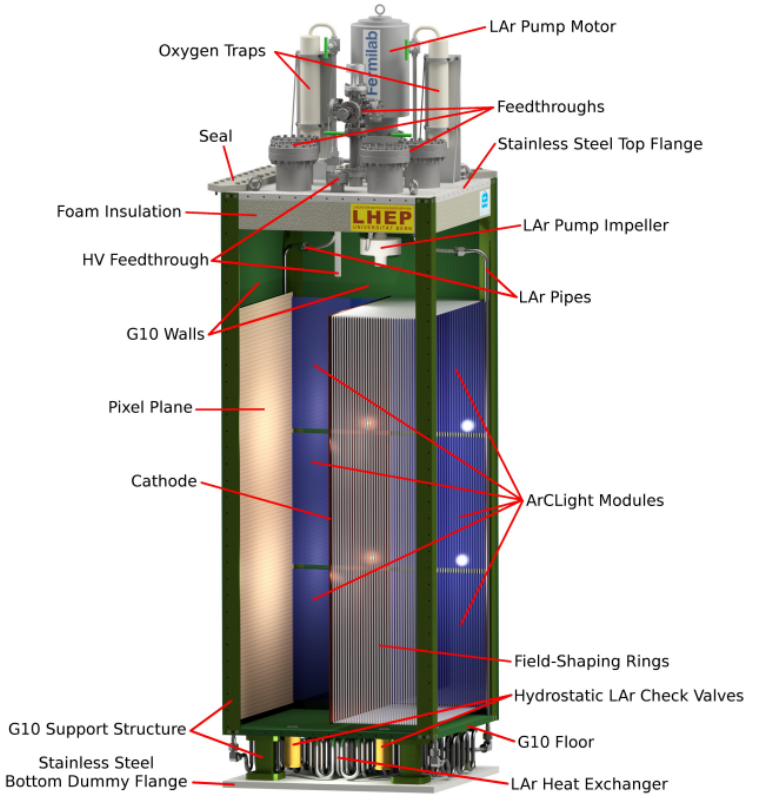
- Spring 2019: LArIAT TPC: collect particle test beam data at FNAL
- Autumn 2019: ArgonCube 2x2 Demonstrator, 6-m^2-scale, a stepping-stone to the DUNE Near Detector.

Some thoughts from Dan

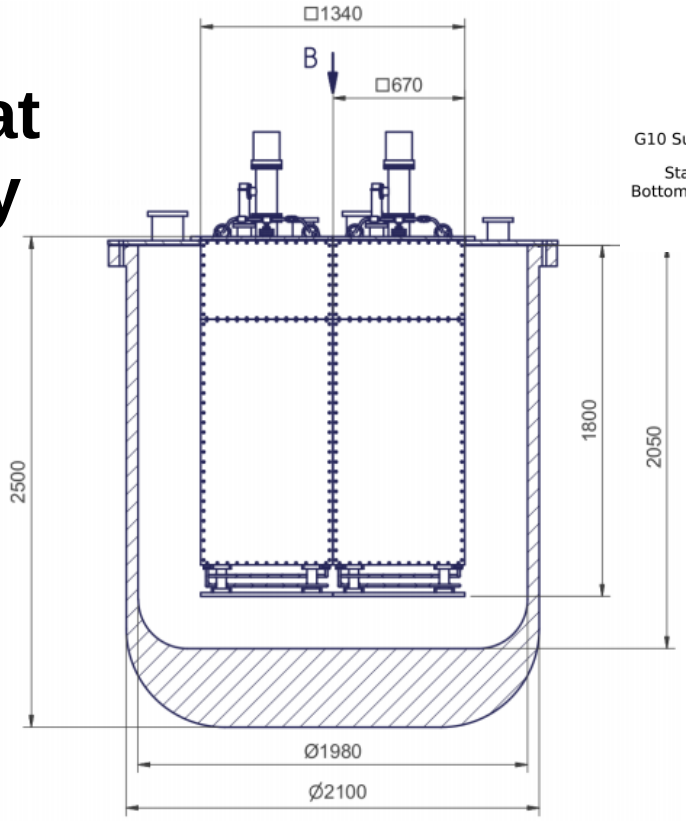
- **Current “ambitious” schedule**
  - Late 2018: Commission dedicated LAr system at LBNL. Design and test ‘modular' PCB tiles, using existing v1 chips.
  - Early-Mid 2019: Produce v2 chip. Build readout system for LArIAT. Operate in test beam.
  - Late 2019: Production of ~6 m^2 system for ArgonCube
- **Things Dan could use help with:**
  - Testing of prototype modular readout tiles.
  - Establish calibration techniques
  - Studies of potential system design improvements.
  - Studies of cryo-qualification and longevity
  - Engineering design for full anode assembly (beyond modular tiles):
  - Mechanical: anode frame, tile attachment, cryo-compatibility
  - Electrical: electrical distribution to tiles (power, clock, I/O), cabling, connectors, feedthroughs.
  - Establish methods for large-scale testing, QA/QC, performance (critical for far detector)

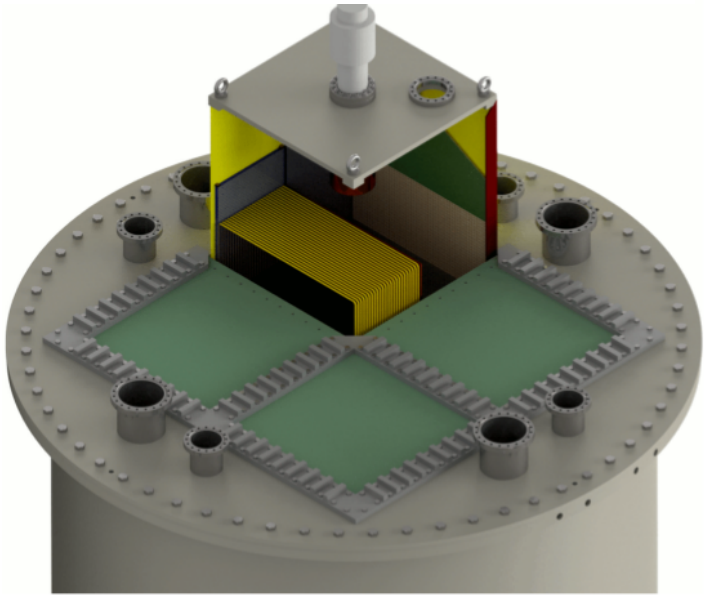
ArgonCube 2x2 Demonstrator

- **The 2x2 demonstrator looks to deploy four identical ArgonCube pixel based LArTPC's utilizing the LArPix chip and ArcLight photo detectors**
  - Dimensions (67x67x180) cm^3
  - Test ~O(100k) pixel sensors in-situ with full detector
- **Initial deployment at Bern for cosmic ray run in early 2019**
  - Planned neutrino beam running at Fermilab later in 2019



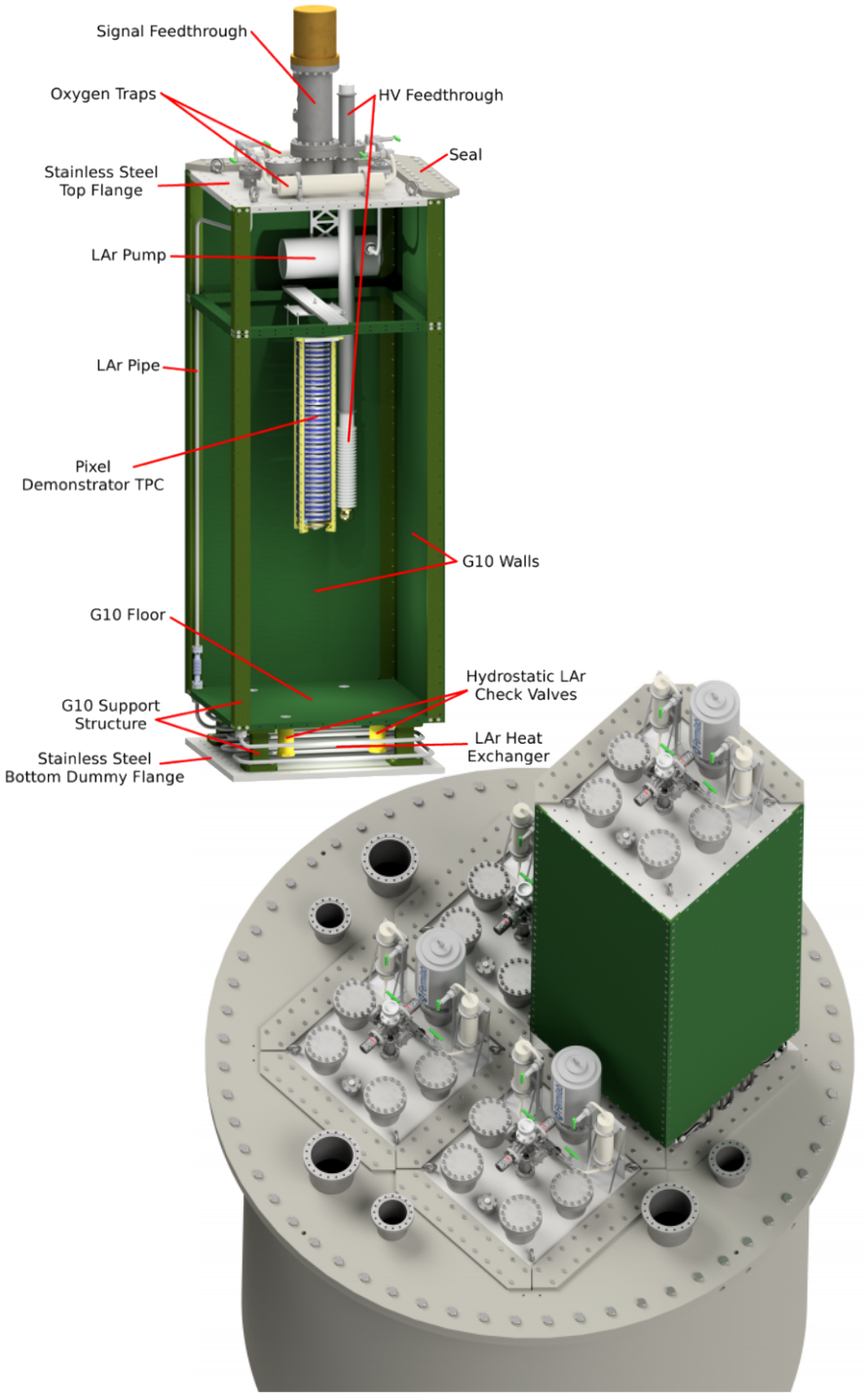
Cut-away illustration of an ArgonCube module

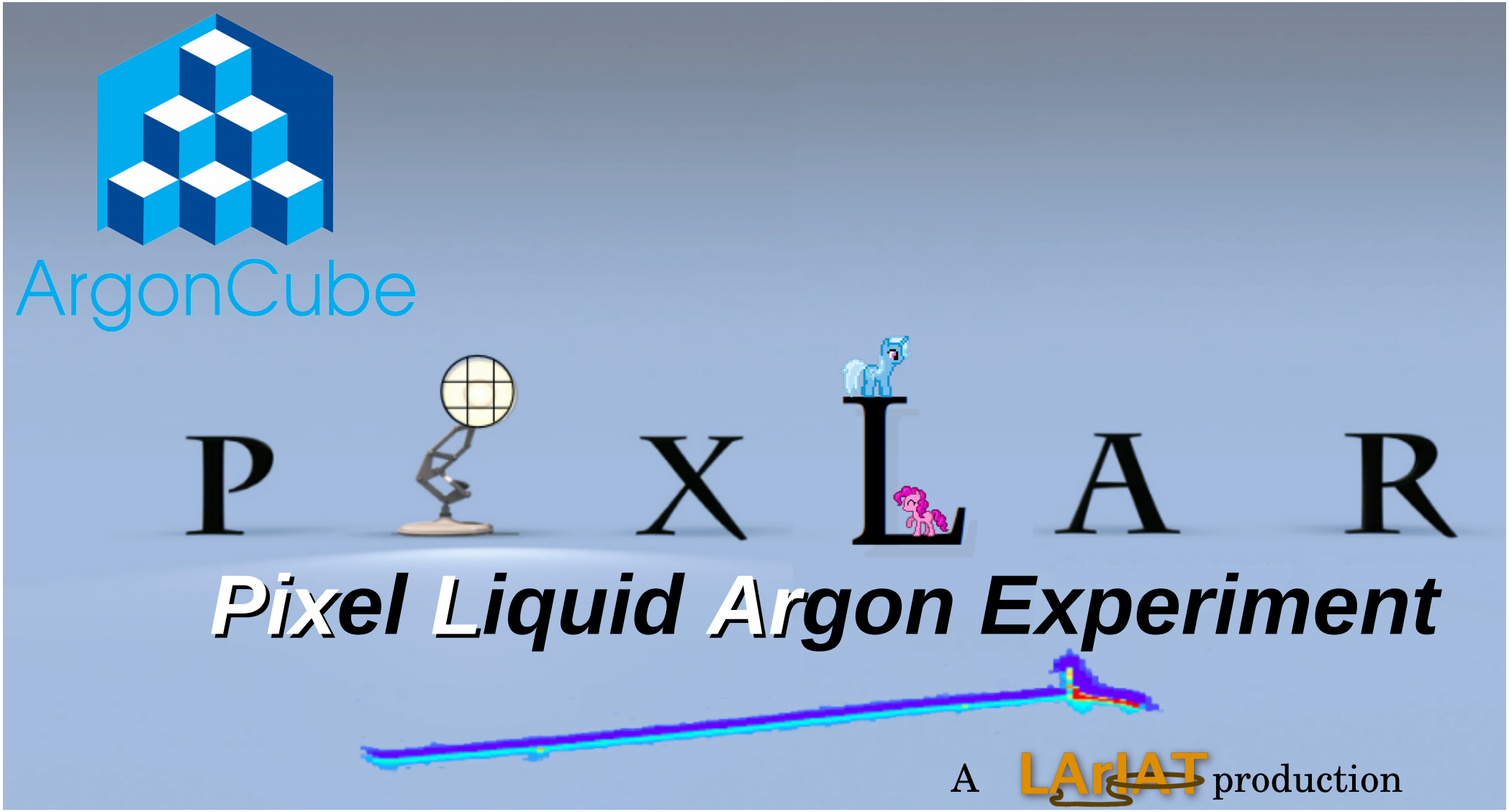




ArgonCube 2x2 Purity Tests

- **One of the design features of the ArgonCube detector is that individual modules can be extracted for servicing**
  - The idea is this allows a LArTPC have less stringent requirements on its operation and allows for upgrades/replacements
- **Demonstration that the liquid argon within the modules can be purified after a “hot” extraction and reinsertion**
  - Will utilize the small LArPix demonstrator as a “purity monitor”
  - Further validate the cryogenic design being considered for the DUNE near detector
  - Testing ongoing at University of Bern

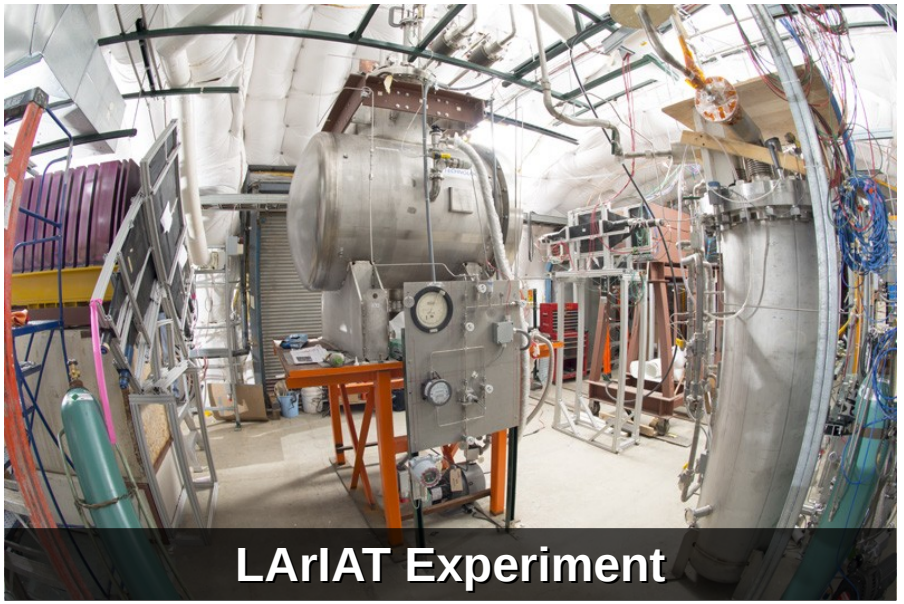


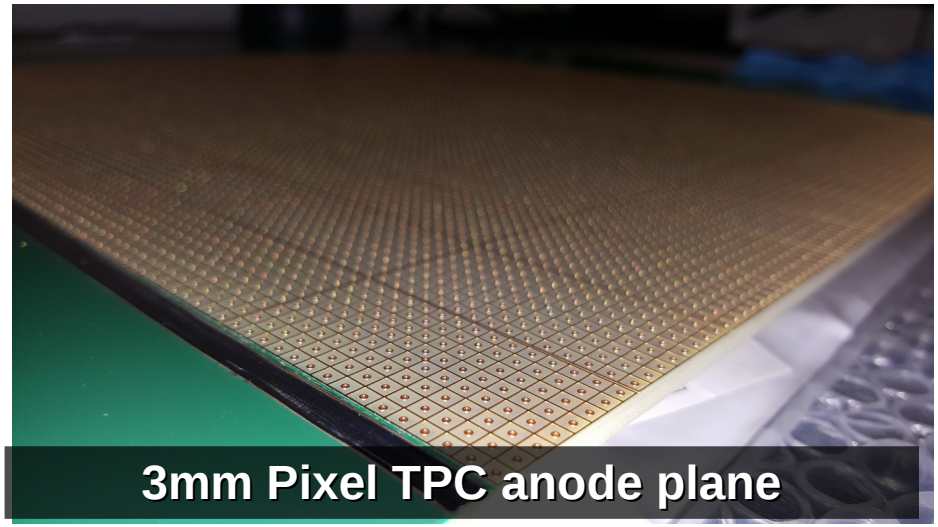


Going to outline quickly a test-beam run that took place at the start of the year and future plans to re-utilize this setup

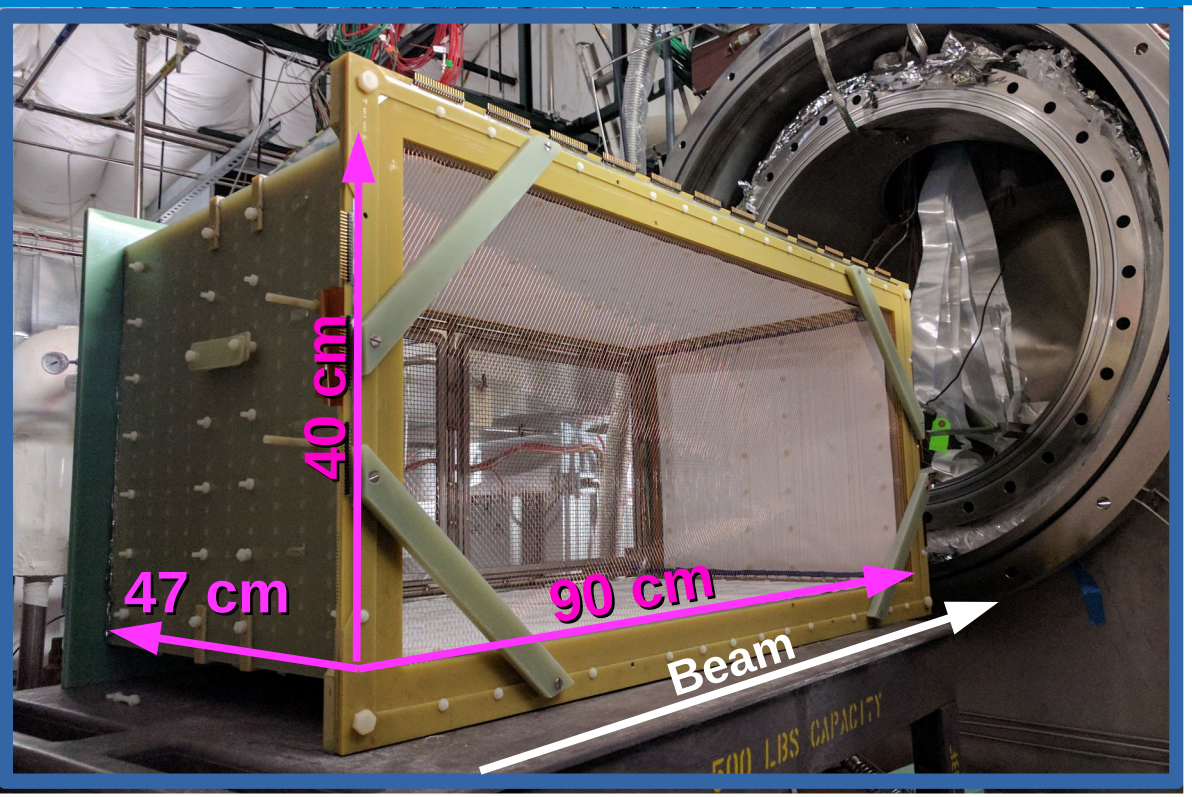
What is PixLAr?

- **PixLAr is the use of the Liquid Argon in A Testbeam (LArIAT) setup, with a pixel based charge readout**
  - The first run utilized the existing cold electronics (LarASIC)
  - Next step is to utilize this setup again with the LArPix chips to help characterize their performance
  - The pixel plane was a PCB based on the option being considered for the DUNE near detector
    - In order to accommodate the existing electronics readout, some multiplexing had to be done
- **Main goals of the initial PixLAr setup**
  - Feasibility of pixel based LArTPC in an operating experiment
  - Demonstration of the ability to cope with a high multiplicity environment
  - Utilize the charge particle beam to perform physics measurements (dE/dX, pion interactions, etc...)
  - Explore additional light readout R&D

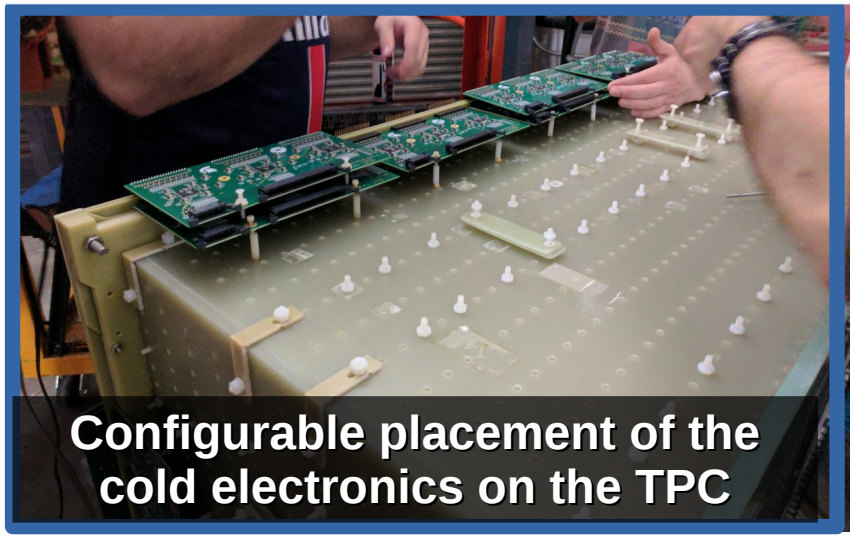

LArIAT Experiment

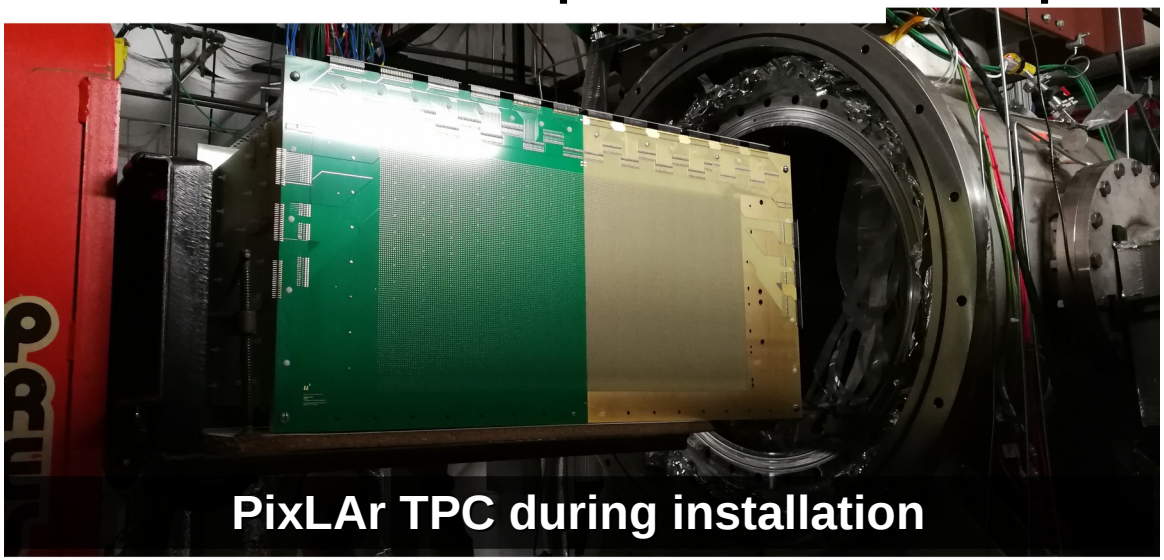

3mm Pixel TPC anode plane

Inside the LArIAT Cryostat (TPC)

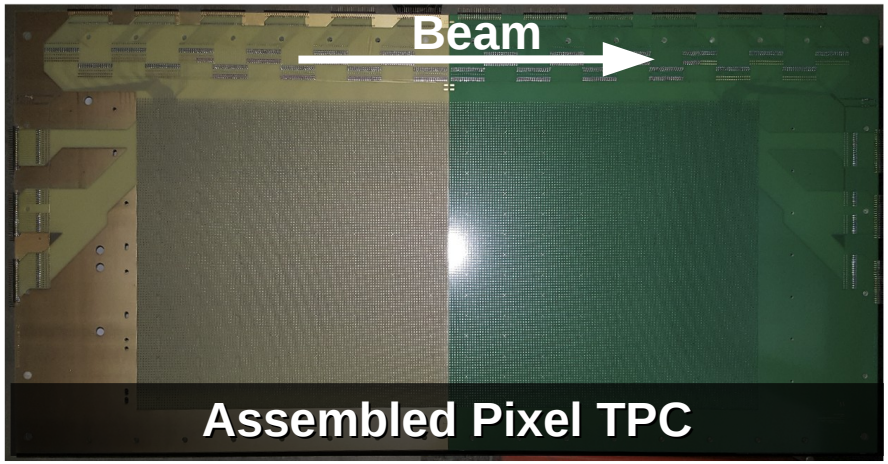


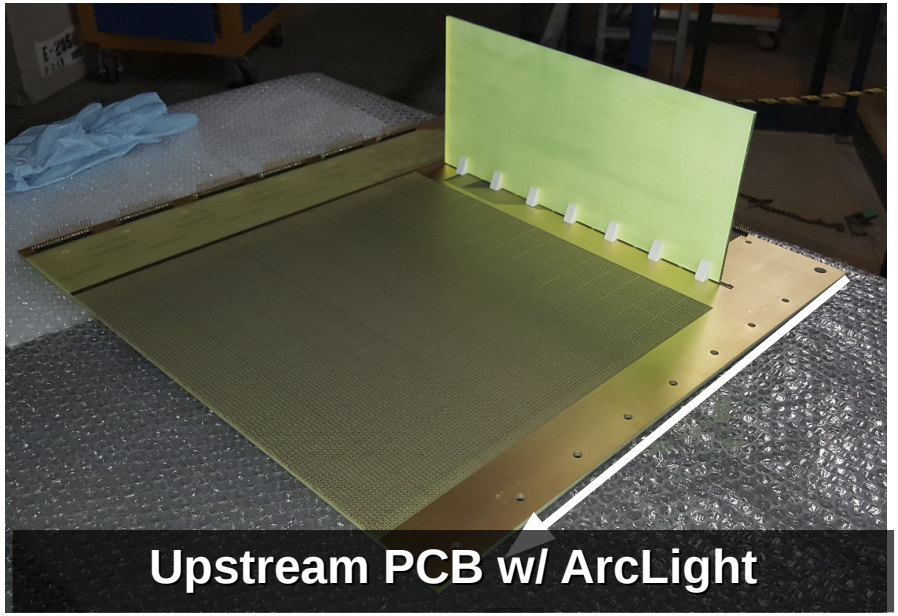
- **90 cm long (beam directions) 47 cm wide (drift direction) 40 cm tall TPC**
- **480 TPC channels available**
  - LArASIC's on custom motherboards (designed by MSU)
    - Same ASICs used by MicrBooNE
  - Output into CAEN 1740 digitizers
  - Great signal to noise achieved in previous wire readout runs
- **500 V/cm nominal field**
- **Ability to integrate various light readout options into the setup**


Configurable placement of the cold electronics on the TPC


PixLAr TPC during installation

PixLAr Pixel Plane

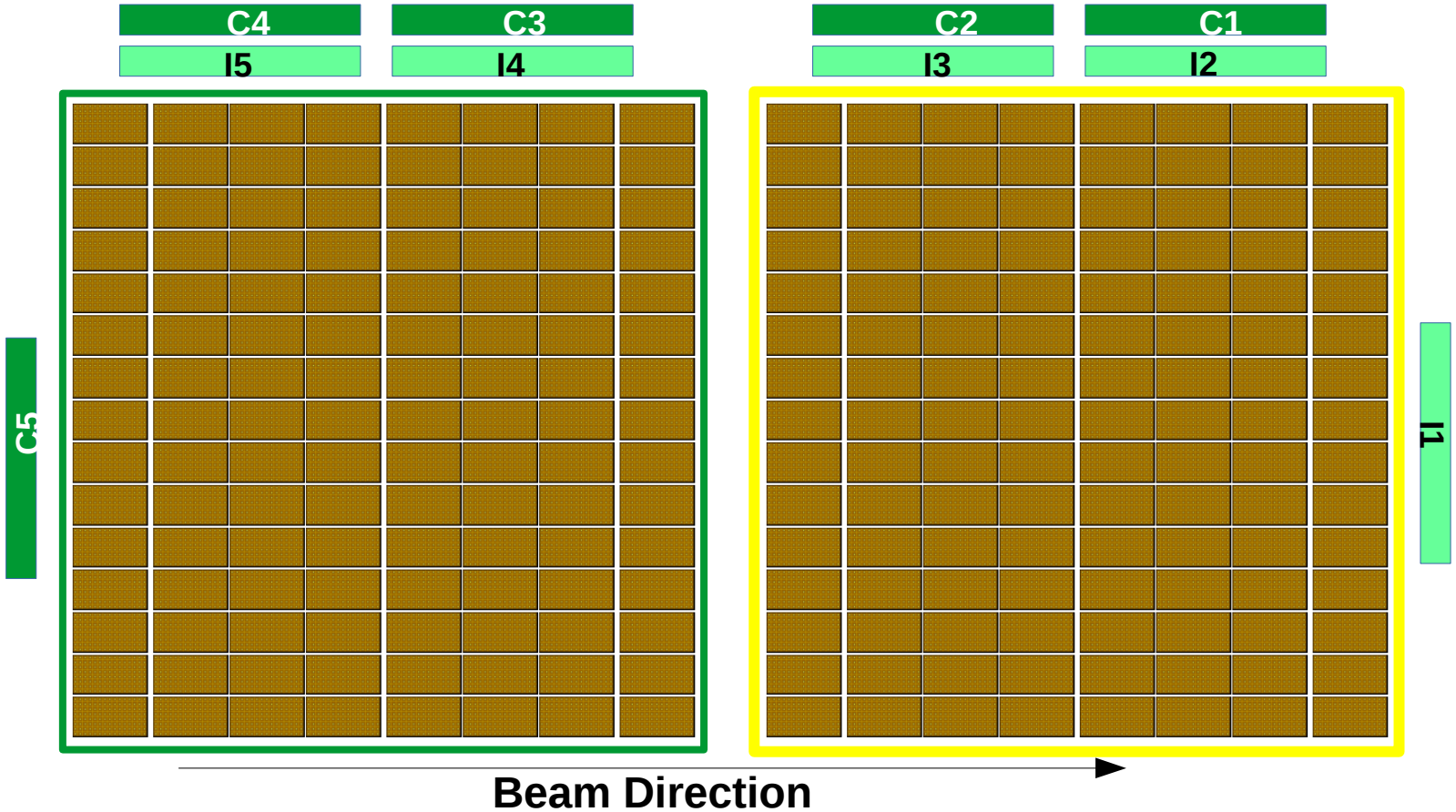




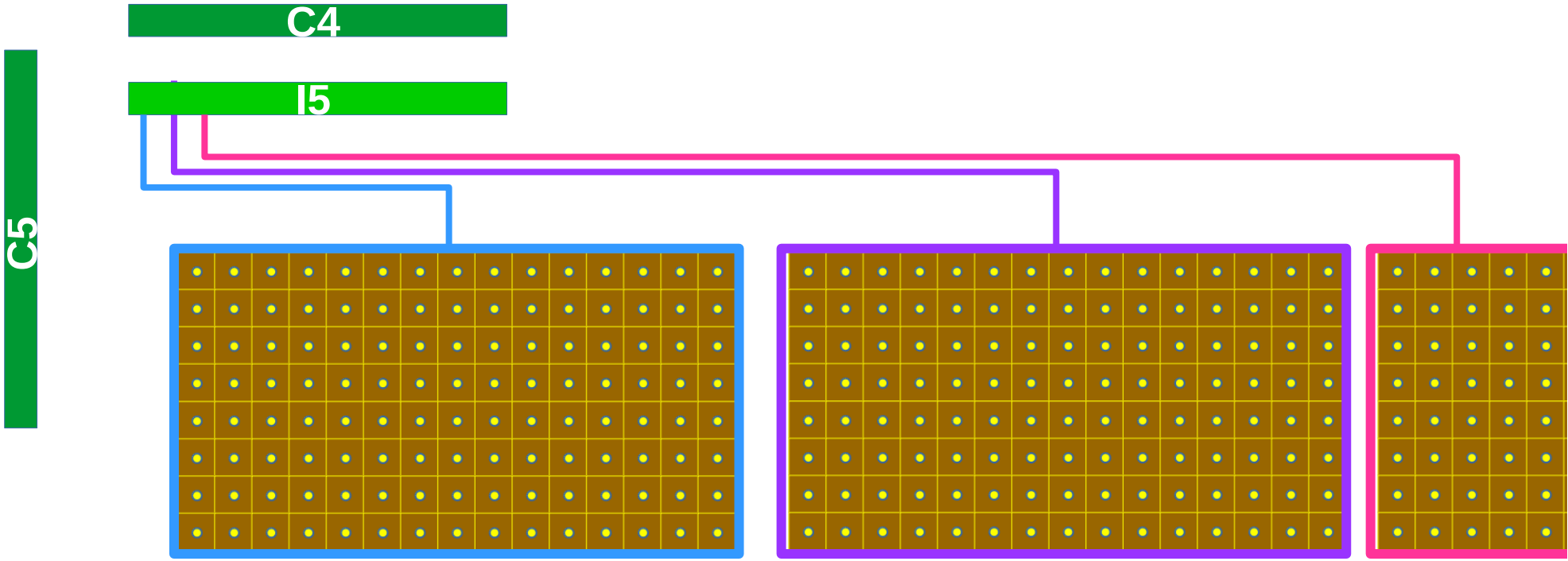
- **The PCB pixel plane was manufactured by the University of Bern**
  - Pixel plane broken into two halves and mounted on the TPC
  - Each plane had a 36 cm^2 active pixel area
  - 14,400 pixels per PCB
    - Total of 28,800 pixels
  - Light detection devices were mounted on the available space in the upstream and downstream portion of the detector
- **Similar setup will be utilized for future test beam runs with the LArPix chips**
  - This initial run was simply to establish the viability of using the pixel PCB and the LArIAT setup

How to get 28k pixels with 480 channels

- **LArIAT's 480 channels are readout on 10 motherboards with 48 channels each**
- **The requires multiplexing the pixels across the TPC to an individual channel (many pixels = 1 readout channel**
  - This means you need a technique to break the ambiguities
    - Will use induction pulses to break this ambiguity
  - Important to note that the demonstration of a pixel ASIC (LArPix) reduces the necessity for such acrobatics
    - Good to have a proof of principle that the method works even with existing electronics

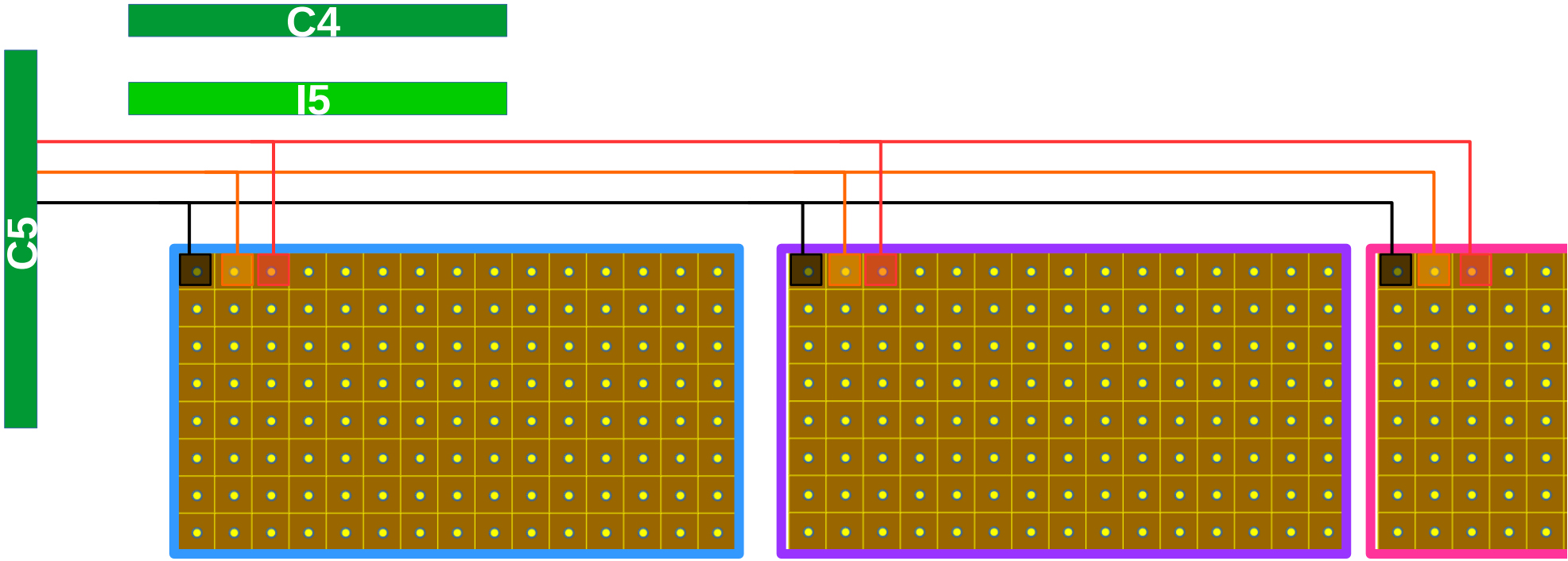


How to get 28k pixels with 480 channels

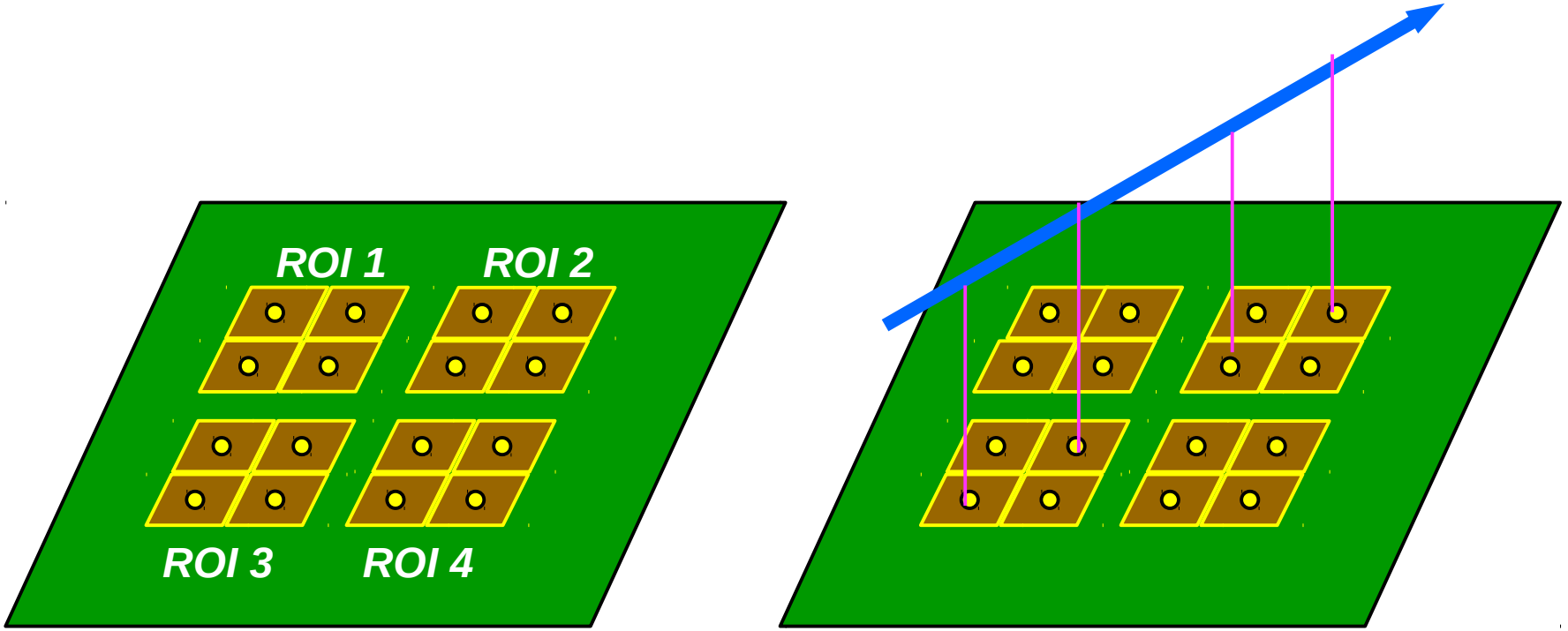


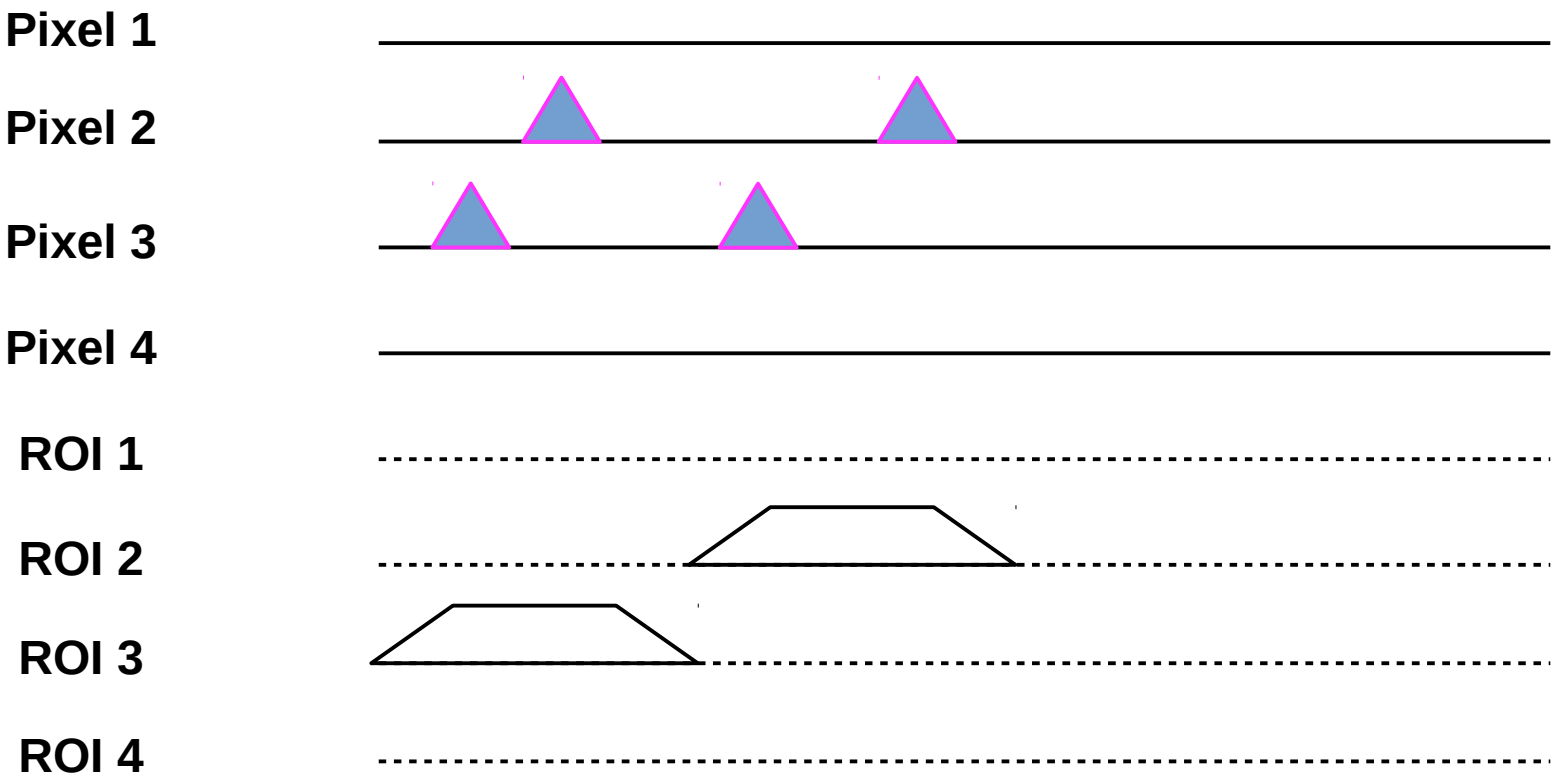
- **The way the multiplexing is done is to treat every 8x15 array of pixels (120) pixels as its own Region of Interest (ROI) which provides an induction pulse**
- **Each one of these ROI's is mapped to an individual channel in the readout**
- **For each PCB there are 120 ROI's arranged into the 36 cm^2 area**

How to get 28k pixels with 480 channels



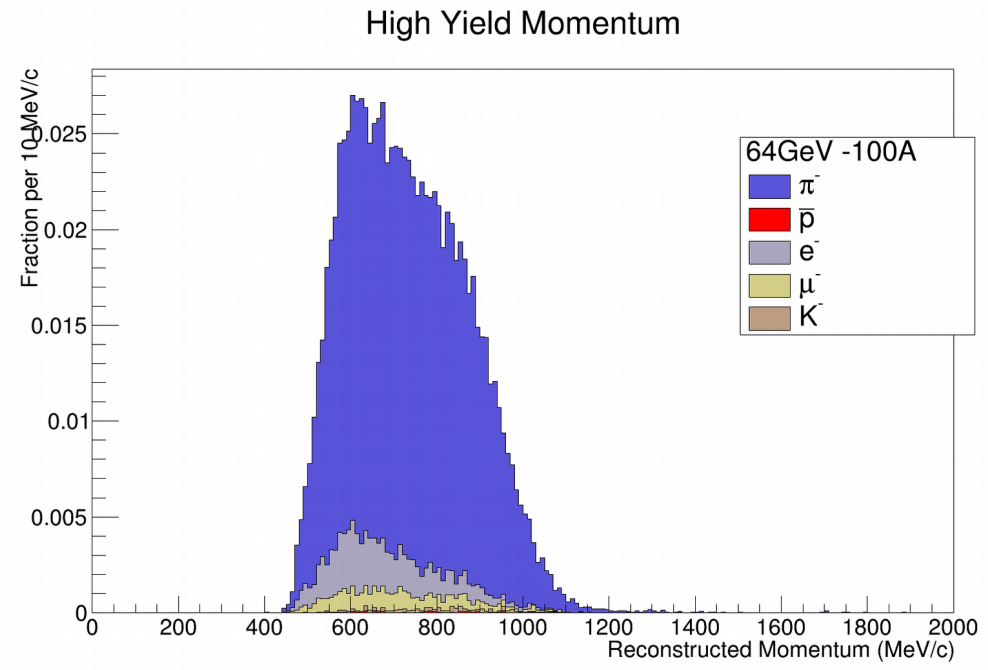
- **Each unique pixel from each ROI is ganged together to reduce the overall channel count**
  - e.g. **Pixel 01/ROI 01** is multiplexed with **Pixel 01/ROI 02**, **Pixel 01/ROI 03**, and **Pixel 02/ROI 01** is multiplexed with **Pixel 02/ROI 02**, etc...

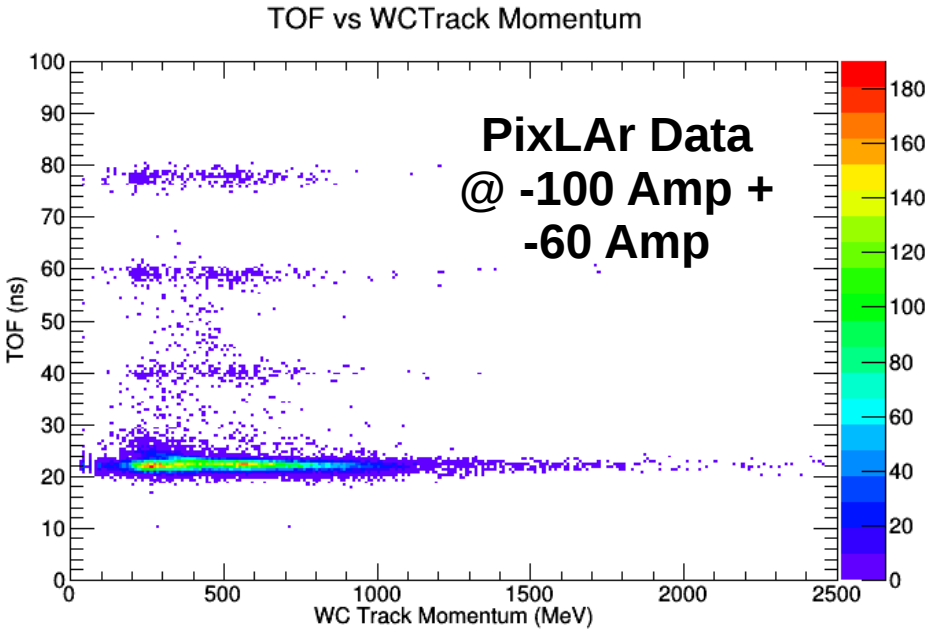

ROI 1
ROI 2
ROI 3
ROI 4


Pixel 1
Pixel 2
Pixel 3
Pixel 4
ROI 1
ROI 2
ROI 3
ROI 4

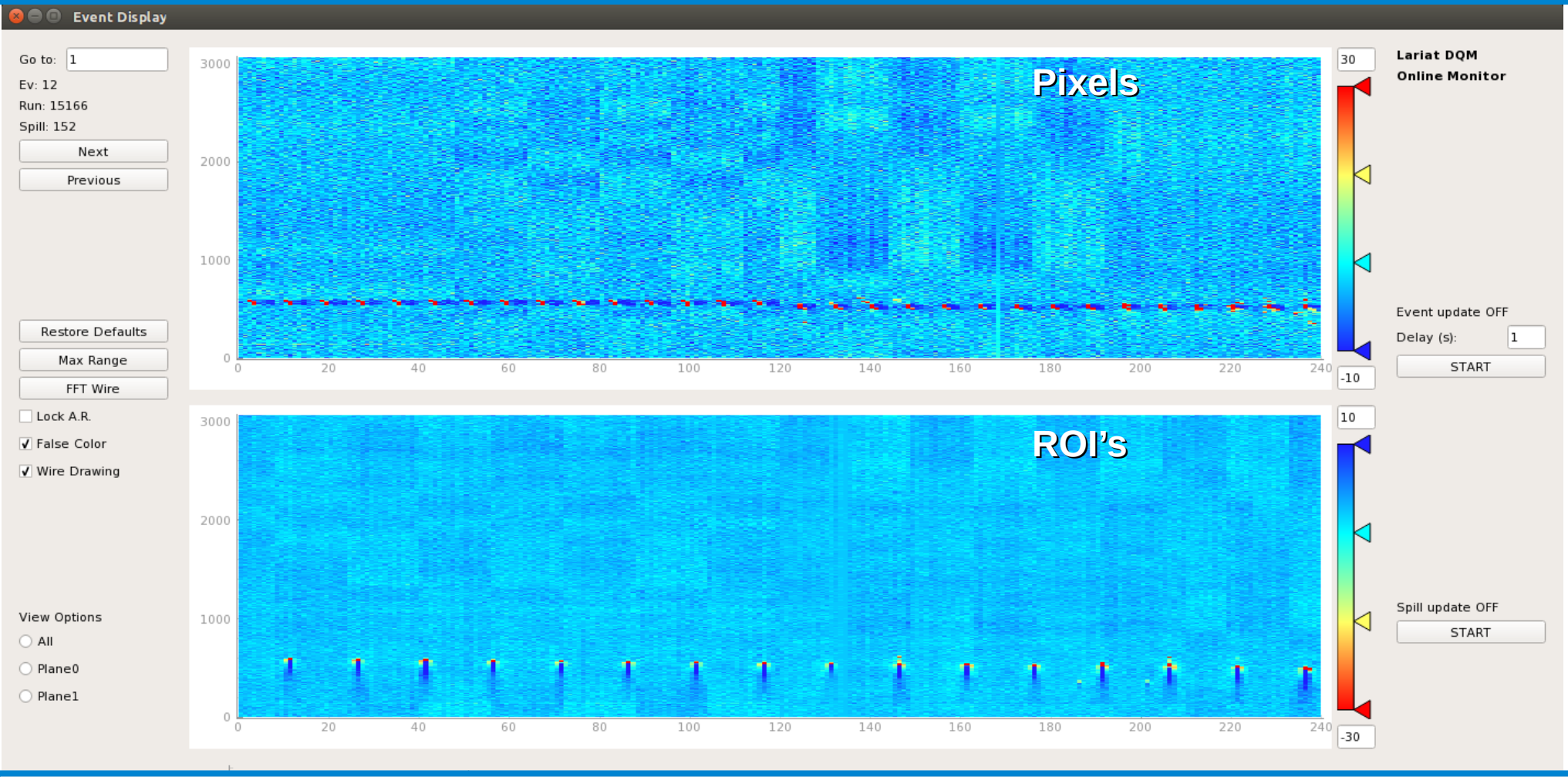
PixLAr Data Taking Campaign

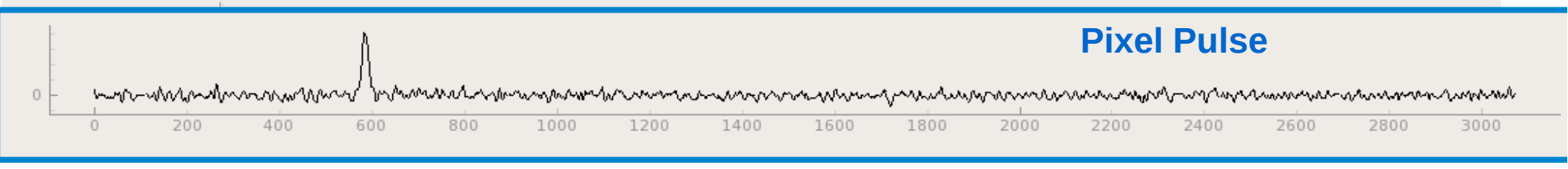
- **PixLAr took data from 12/1/17 – 1/25/18**
  - 7 weeks of data taking in a number of different beamline configurations
    - Both magnet polarities and at low and high momentum
  - Also triggered on cosmic rays using LArIAT cosmic paddles
    - Provides a nice sample of tracks which cross anode to cathode to help with calibrations and reconstruction

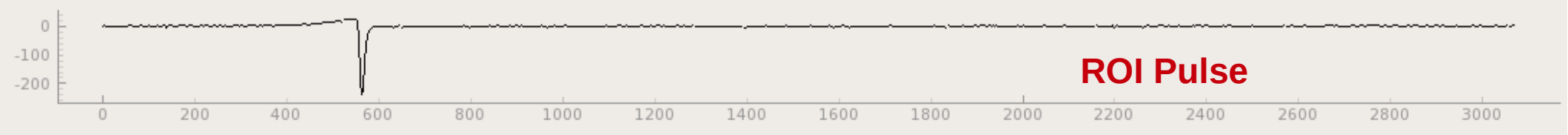


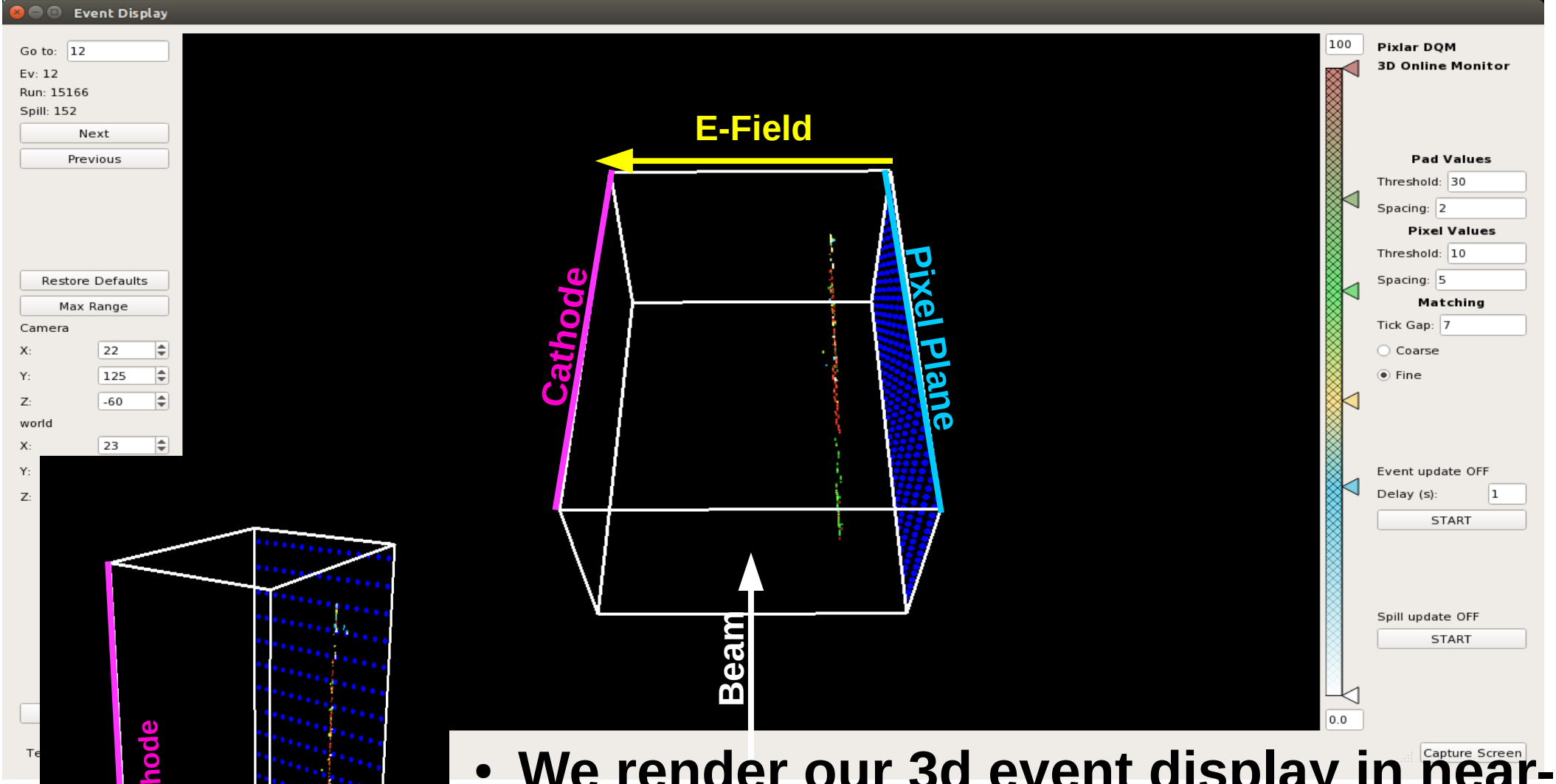


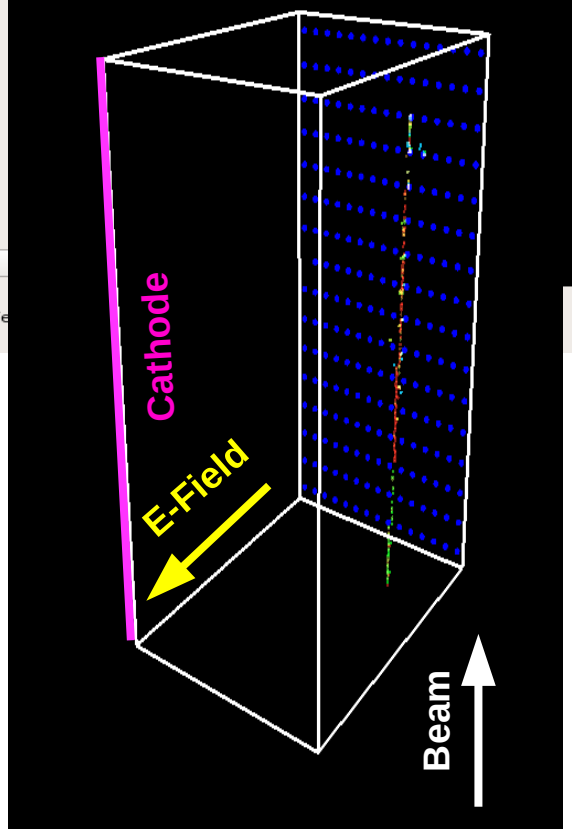
Pixel / ROI Event Display





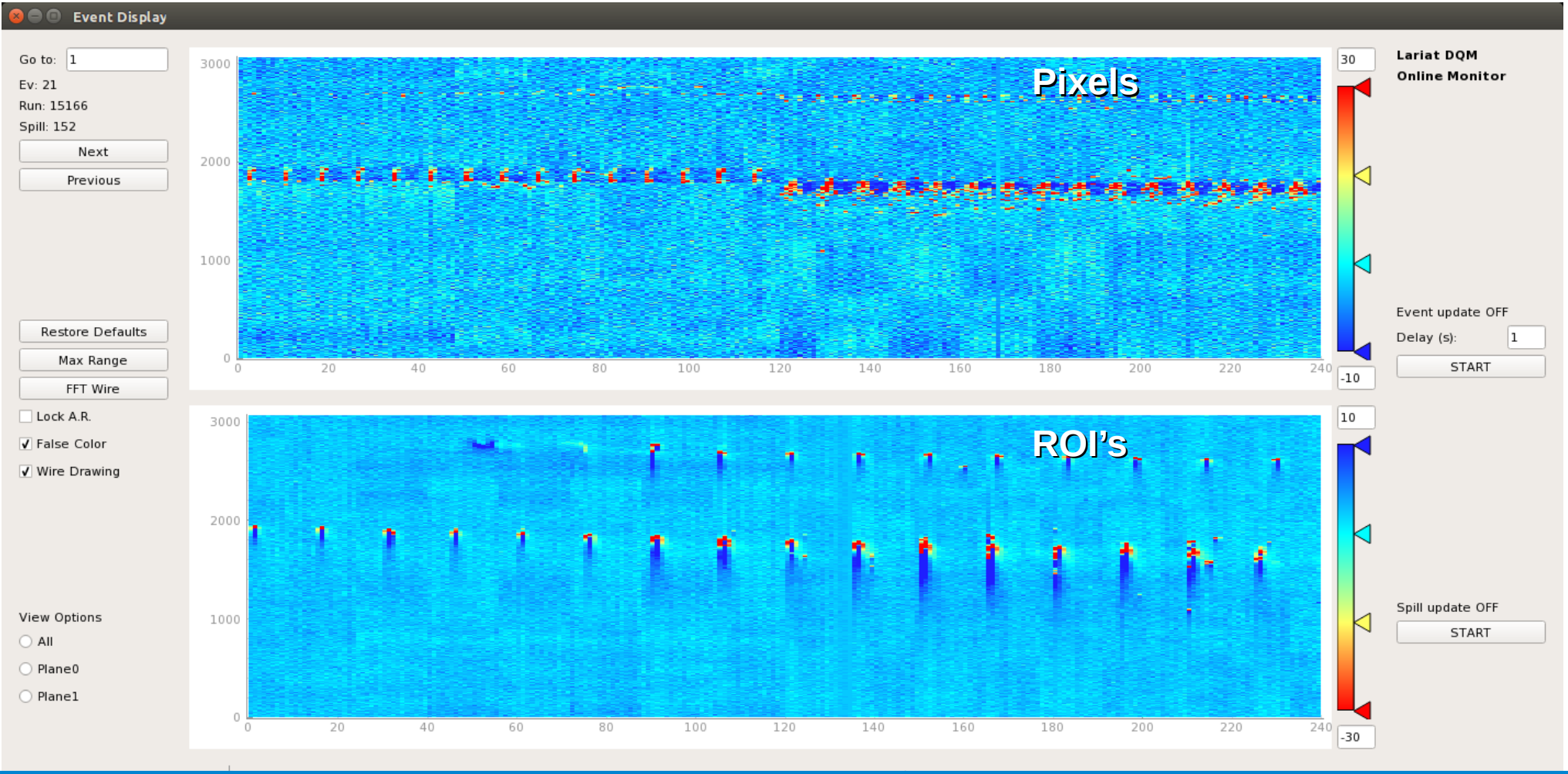


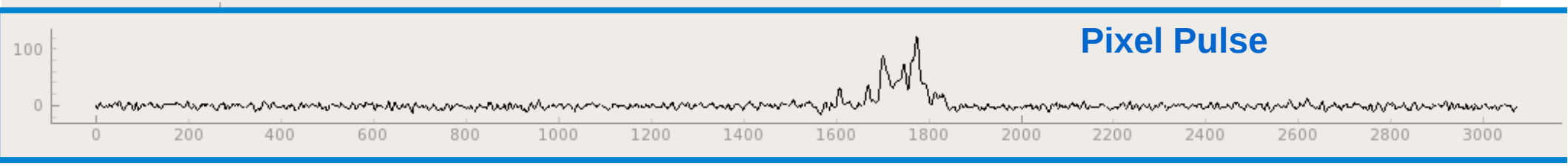


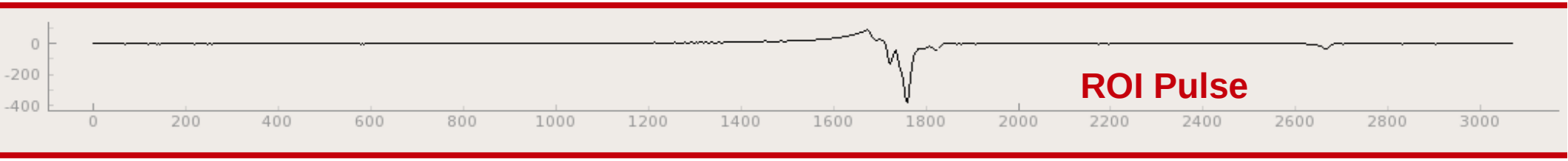


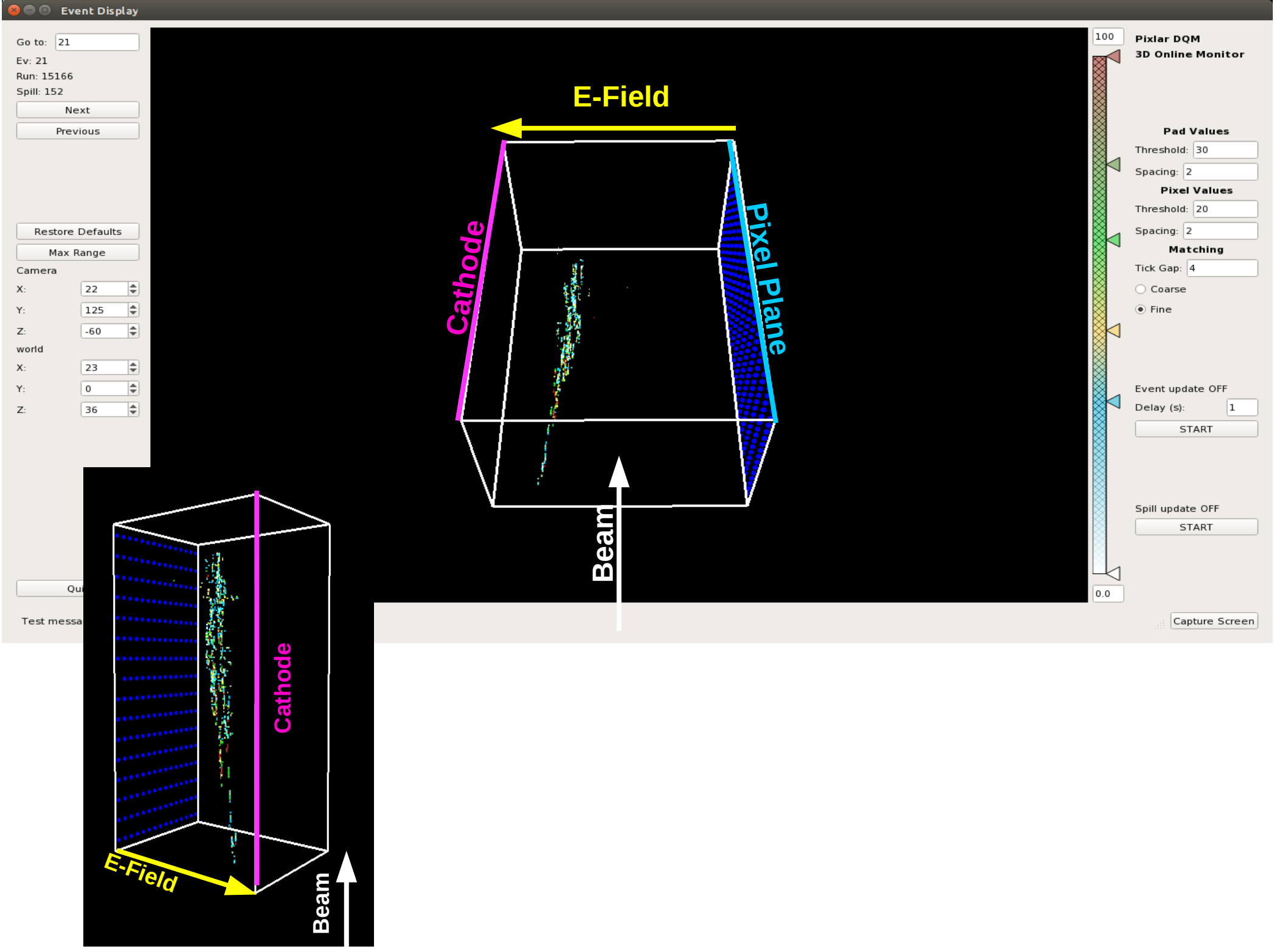
- **We render our 3d event display in near-real time (~1 min lag behind the DAQ to process the event)**
- **Here Pixel/ROI matching has been done**
  - For speed we typically only plot the ROI block

Pixel / ROI Event Display (EM-Shower)



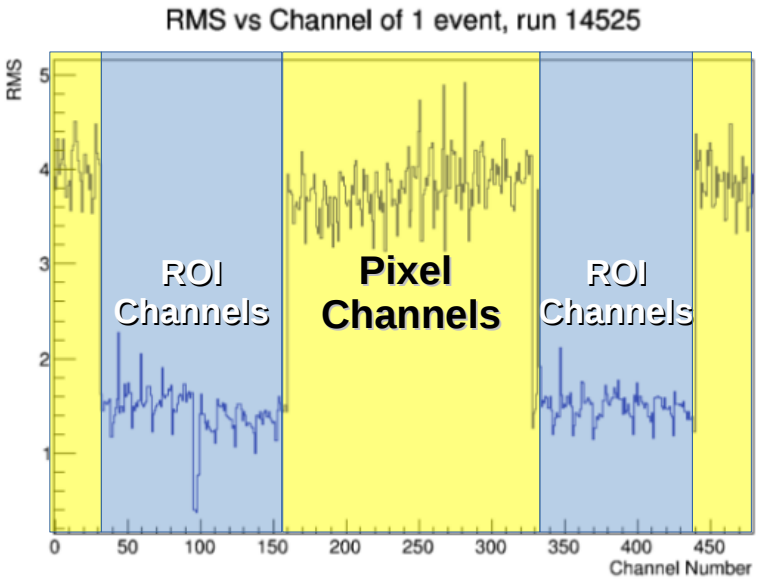


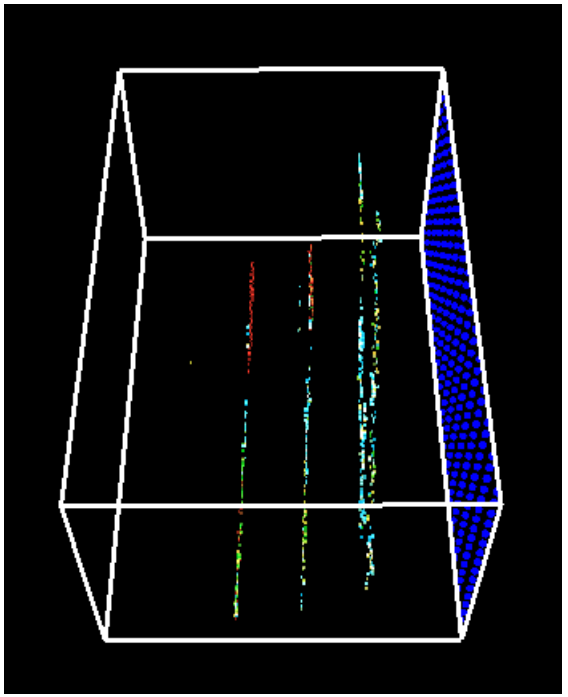



Event Display
Go to: 21
Ev: 21
Run: 15166
Spill: 152
Next
Previous
Restore Defaults
Max Range
Camera
X: 22
Y: 125
Z: -60
world
X: 23
Y: 0
Z: 36
Qui
Test messa
E-Field
Cathode
Pixel Plane
Beam
100
0.0
Pixlar DQM
3D Online Monitor
Pad Values
Threshold: 30
Spacing: 2
Pixel Values
Threshold: 20
Spacing: 2
Matching
Tick Gap: 4
Coarse
Fine
Event update OFF
Delay (s): 1
START
Spill update OFF
START
Capture Screen
Cathode
E-Field
Beam

What we've learned so far

- **PixLAr was able to achieve resonable signal to noise even with the extensive multiplexing done for the pixels**
  - With no noise filtering we are seeing ~12:1 S:N
  - We expect this will improve slightly with some software noise filtering
- **High multiplicity events don't seem to pose a problem for this technology**
  - We can clearly disentangle 3-4 tracks per 45 cm drift region with no problems
  - I claim we will easily reconstruct 8+ tracks per 45 cm drift region
    - This work is ongoing to give solid performance numbers for minimum track distance and high multiplicity, but even simple event displays and rudimentary matching shows promise
    - DUNE near detector won't contend with the multiplexing we had to do here (thanks to the LArPix work)

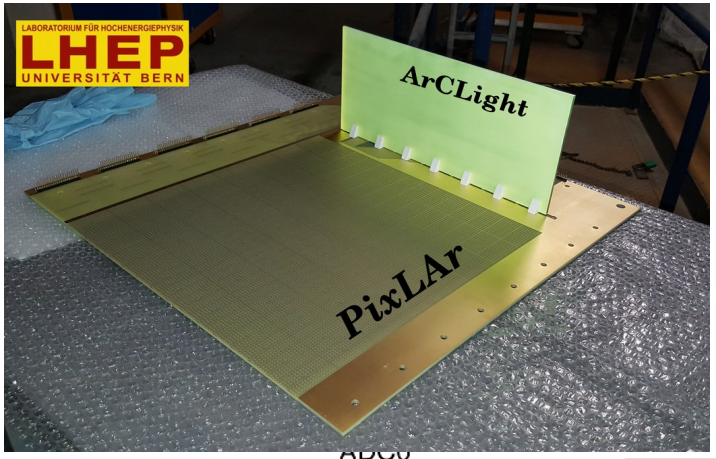


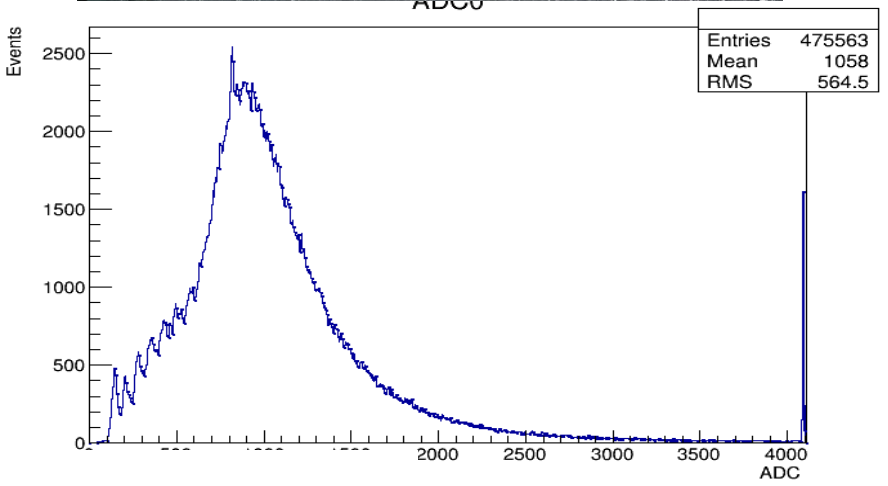


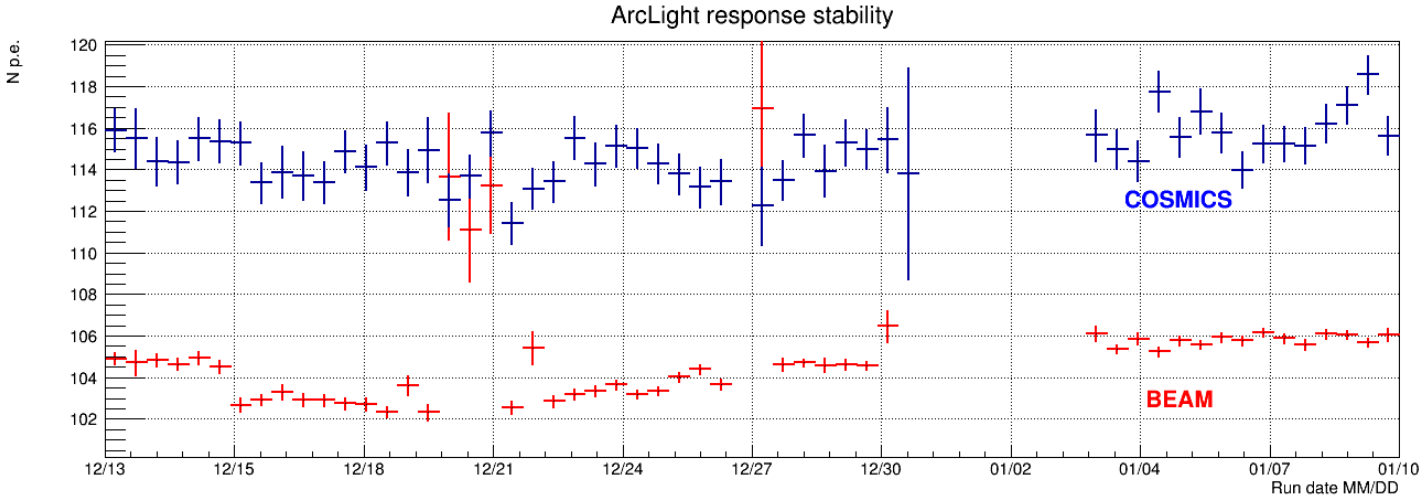
4 through going tracks

ArcLight Performance

- **4 out of 8 SiPM's worked**
  - Not clear what caused the other 4 to lose response
- **Single PE response seen in both beam and cosmics**
  - Very preliminary photon detection efficiency ~0.24%
    - Expected ~0.35%
    - Work still ongoing….
- **ArcLight response was stable over the course of our run**

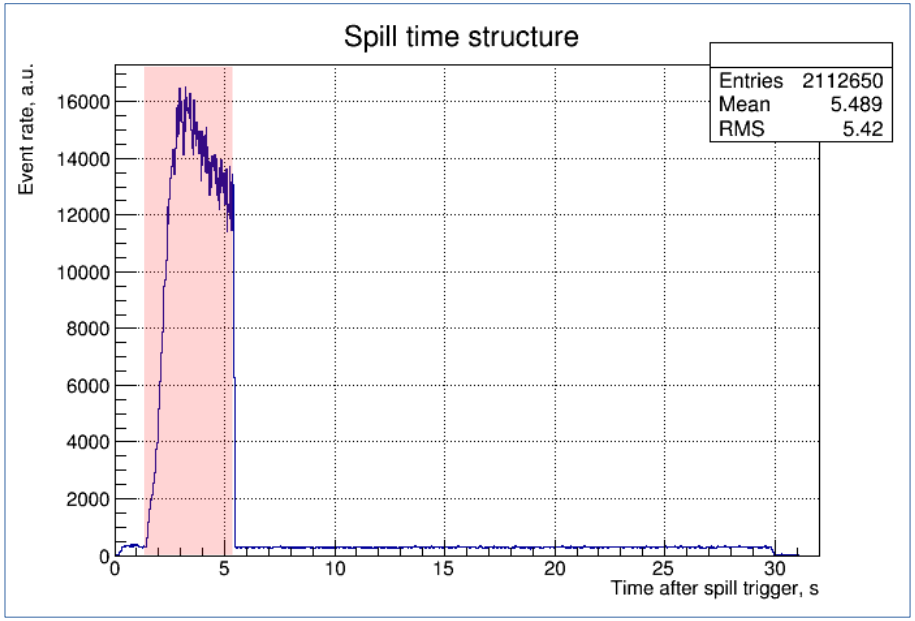


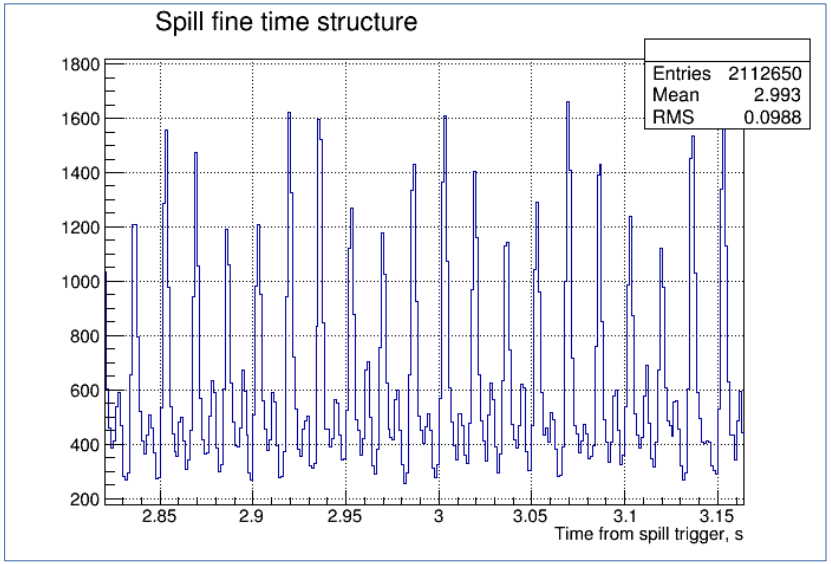


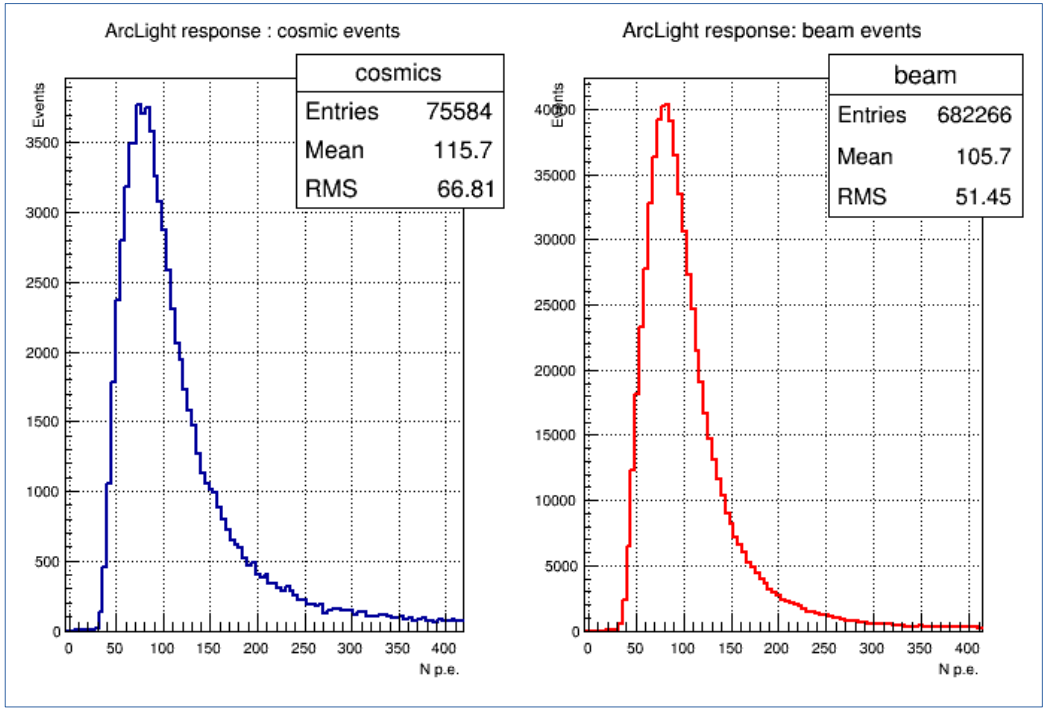


ArcLight Performance

- **Using the timing information from the ArcLight, the beam spill structure becomes apparent!**
- **Light Yield for both beam and cosmics is very consistent**







PixLAr Conclusions

- **PixLAr completed its test beam data taking earlier this year**
  - We have a veritable treasure trove of interesting pixel LArTPC data in hand!
  - Will be working in collaboration with LArIAT to hopefully do some interesting cross-comparisons between the wire and pixel readout
    - Note: Since the hardware multiplexing was used for this setup, it isn't a true demonstration of the power of pixel readout...but a good step in that direction!
- **We continue to work toward the full 3d reconstruction of these events**
  - First results just starting to come to maturity
  - Nearline 3d rendering of the events shows the real power of these detectors
  - More detailed reconstruction still to be done
- **Both the Arapuca's and ArcLight successfully took beam data during the run**
  - Combining the output of both these detectors should provide useful input to the ongoing LAr-Light readout R&D

Parting thoughts….

- **LArPix readout technology has come along rapidly and successfully to demonstrate a low power, low noise pixel based readout for LArTPC**
  - Version 2 of the chip currently being designed
  - Ongoing tests with version 1 to help establish baseline performance and inform version 2
- **Number of test stands currently being used to continue the work with pixel based LArTPC**
  - Test stands at University of Bern, LBNL, Fermilab, and UTA
  - Future planned runs with next generation LArPix chips coming up fast!

Thank you for your attention

Questions/Comments