A Pixelated Readout System

What does one want for a real DUNE sized system?

Rick Van Berg

Penn

8/14/18

General System Considerations

- Power
- Complexity / Reliability
- Data volumes

- Requirements
  - Sensitivity
  - SNR
  - Data – time, charge, location…???

Power – Crude Estimate

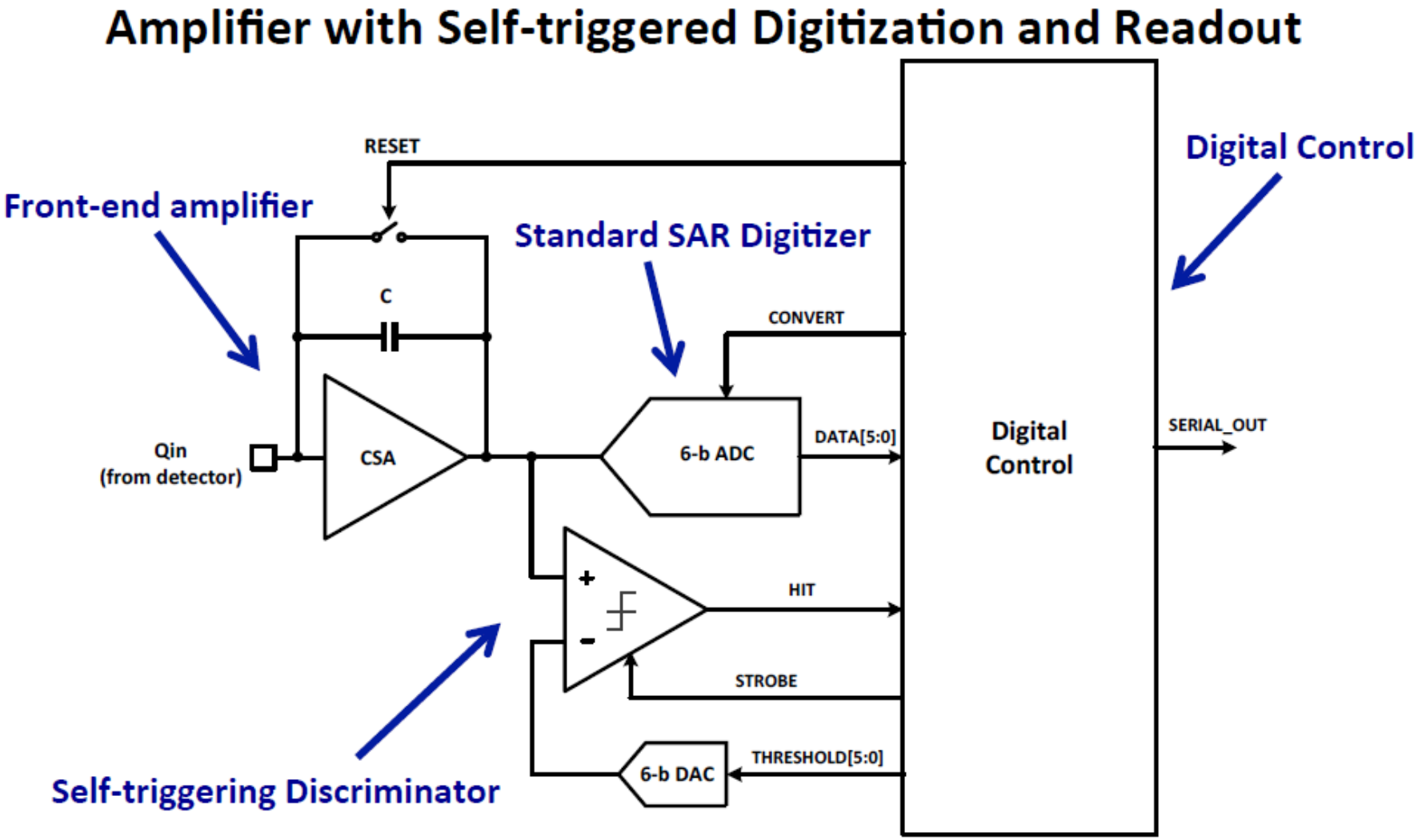
- DUNE limit – cryo plant - < 50 mW/channel x 2560 ch/APA = 128W
- → < 0.2 mW / 5x5 mm pixel or < 0.1 mW / 3x3 mm pixel
- LBL LArPIX-v1 ~0.062 mW / channel (Dan Dwyer May Collab. Mtg.)
- Penn simulation estimate (for front end only) ~0.054 mW

- Apparently not a show stopper – we can proceed

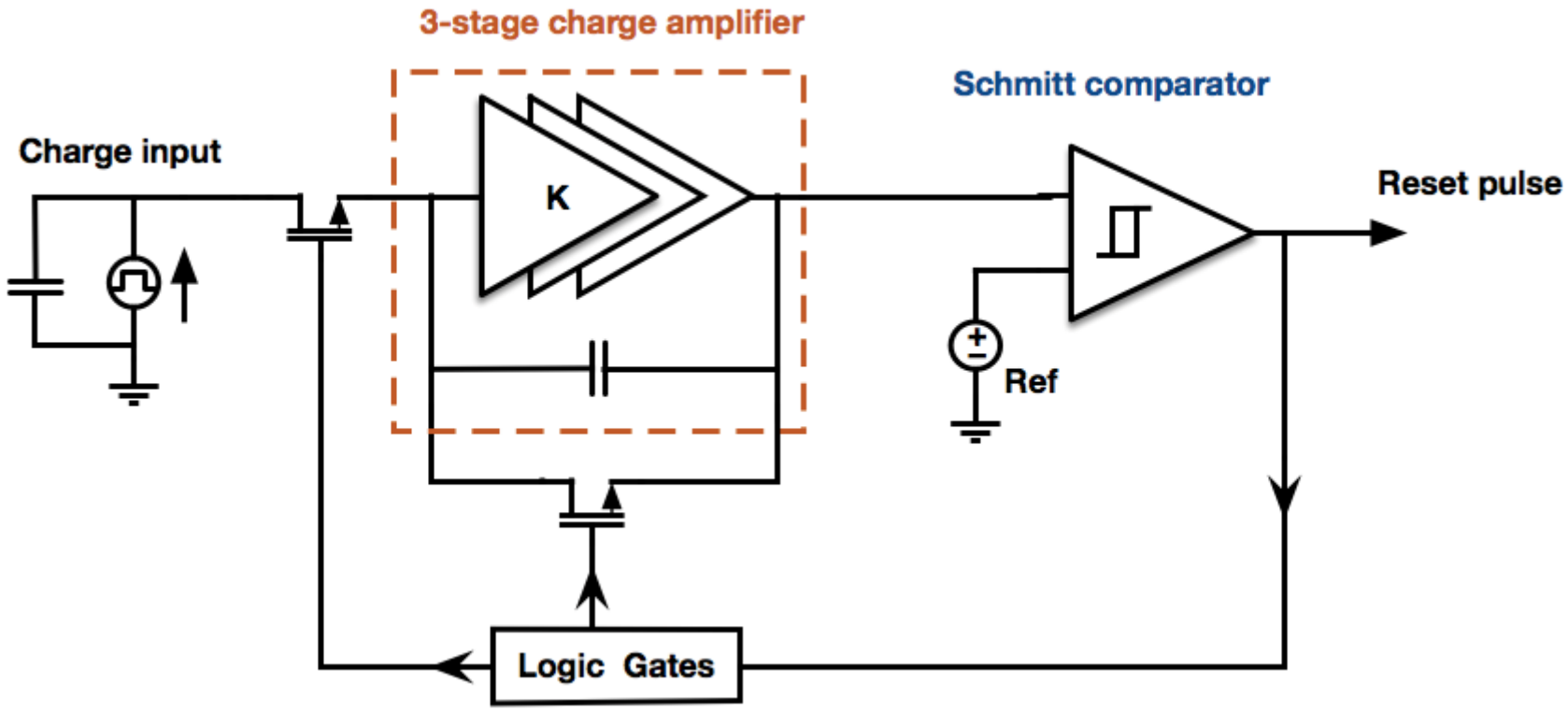
Complexity & Reliability

- Natural tension – the more complexity the less reliability – how to optimize? What would Mr. Ockham do?
- What is simple?
  - One output line per pixel is “simple” but 600,000 cables per APA is not
  - Self healing, self routing data paths through myriad chips is “simple” but the logic for that is not (think routers, name servers, retransmission…..)
  - What intermediate solutions are possible?

LBL LArPix-v1 – Dan Dwyer



Penn – P. Wang, L. Du – TSMC 65 nm



0.054 mW – unit charge counter – simulation only

Data Volume – Crude Estimate

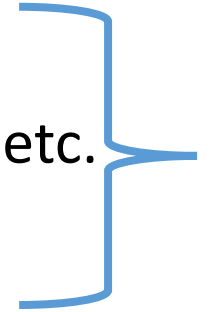
- Assume 5 mm x 5 mm pixel → 500 x 1200 for DUNE APA = 600,000 px
- 10 MBq/cavern → 50,000 Ar^{39} / APA volume / sec
  - Pix # - 20 bits
  - Time – 32 bits (if 2 MHz clock, rolls over in ~ ½ hour)
  - Charge – 8 bits?
  - → 8 B / hit → 400 kB/sec (vs. 5 GB/s!)

A Vaguely real scheme

- How many channels per chip?
  - A packaged chip is ~ 1 cm^2
  - Pixel capacitance drives noise so connections should not be overly long
  - 64 pixels 5x5 mm = 16 cm^2 (2 cm trace) so near that limit plus at ~ 100 pins near cheap / simple package and assembly limit ➔ assume from 32 to 100 channels per chip ➔ so for one APA → 6,000 to 18,000 chips per APA
- For simplicity take 64 channels per chip, ~10,000 chips per APA
- Cheap circuit boards want to be < 22” x 22” so do 0.5m x 0.5m pcb – 10,000 pixels per board → 156 chips/board and 60 boards per APA

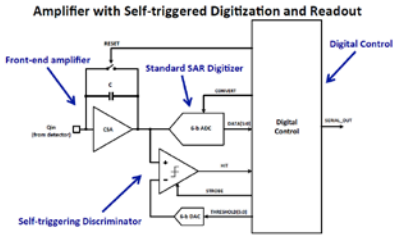
System Aspects – in the cold

- What inputs and outputs does the pixel chip need?
  - Want a clock and a synch input (one line with encoded synch?)
  - Want a control path in and out (two lines) to set DACs, read registers, etc.
  - Want a data path out (one line)

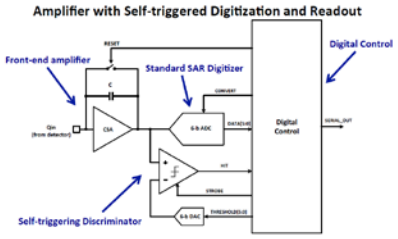


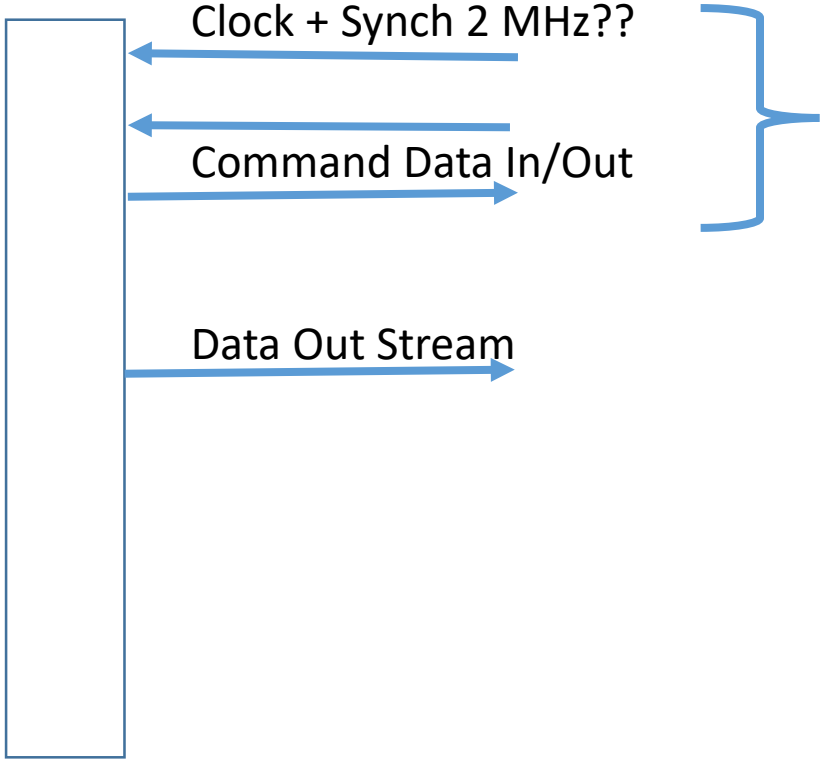
- Per chip that is a lot of lines given 10,000 chips per APA
- Per board it is not so many (per APA 240 diff pairs vs. 160 diff pairs in present DUNE design but MHz vs. GHz so much smaller gauge works)
- So need one (?) more ASIC to mux data in and out and fanout clocks and commands

Crude Scheme – FE chip



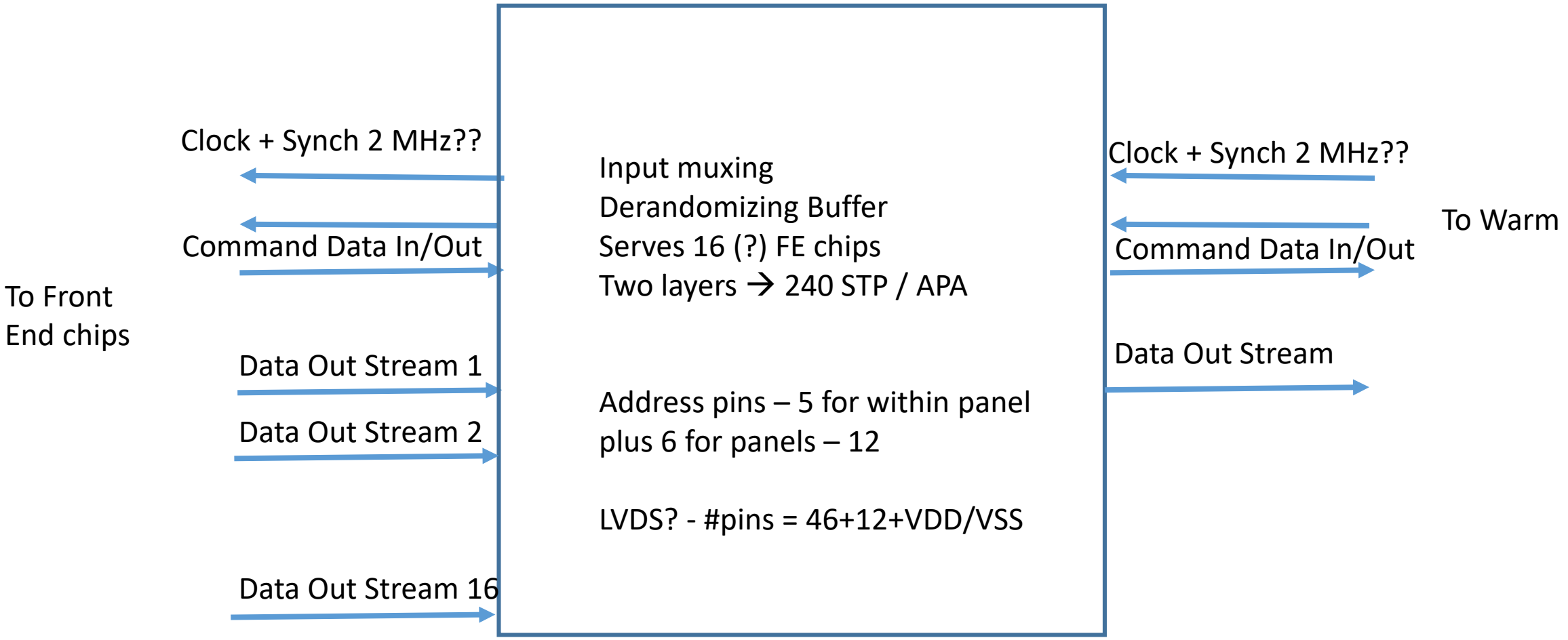
Pixel logic
Local data buffer?
64 (?) channels





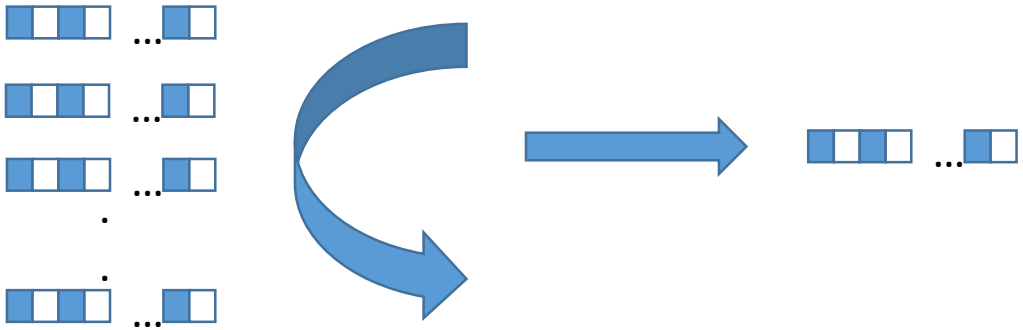
FE Control Block
Derandomizing buffer – ?kB
Control interface
Other bells and whistles?
No. pins = 64 + 8 LVDS + ??

Crude Scheme II – Buffer Chip



Readout FIFOs

- All 8 or 10 Bytes wide to fit basic datum
- Per pixel – 4+ words to derandomize into FE central FIFO
- FE FIFO – 1+? kWord to allow for perpendicular tracks in several pixels
- Buffer chip – several kWord (??) to derandomize to output
- Need physics driven simulation to set the numbers – they seem, at first look, relative modest for 65nm or 130nm – is that true?



System Aspects – in the warm

- Provide common clock (and synch) to all pixels
- Provide control path to and from each FE chip
- Concatenate data into “events” or “fragments” or just an unordered but mux’ed stream?

Warm Side DAQ

- Slow control path to/from 60 panels per APA
- Mux and forward 60 data streams into 1 stream per APA (<< 10 Mb/s)
  - Into Ethernet switch? Into computer farm? Arduino farm?.....
- Power?
  - Regulate in warm, sense from cold probably most conservative
  - Do we need local regulators on panels? If so probably need to design ones for cryo use and worry a lot about low frequency oscillations

Requirements – from Physics

- Energy sensitivity down to near Ar^{39} level (efficient for SN events and other low energy physics) – so “trigger” at a few MeV or less? Want as little trigger bias as possible – this sets noise level of << 1,000 e^-
- Rate capability – assume nearby SN, >10^6 events in 10 sec so >> 1 hit per second per pixel – OR – track perpendicular to pixel plane - ~ 100 hits in 0.5 ms so either deep first stage buffer or readout at hundreds of kHz / hit – shared buffers in front end chip probably best but need simulation
- Pile up rejection – c’mon, this is neutrino physics
- Others?

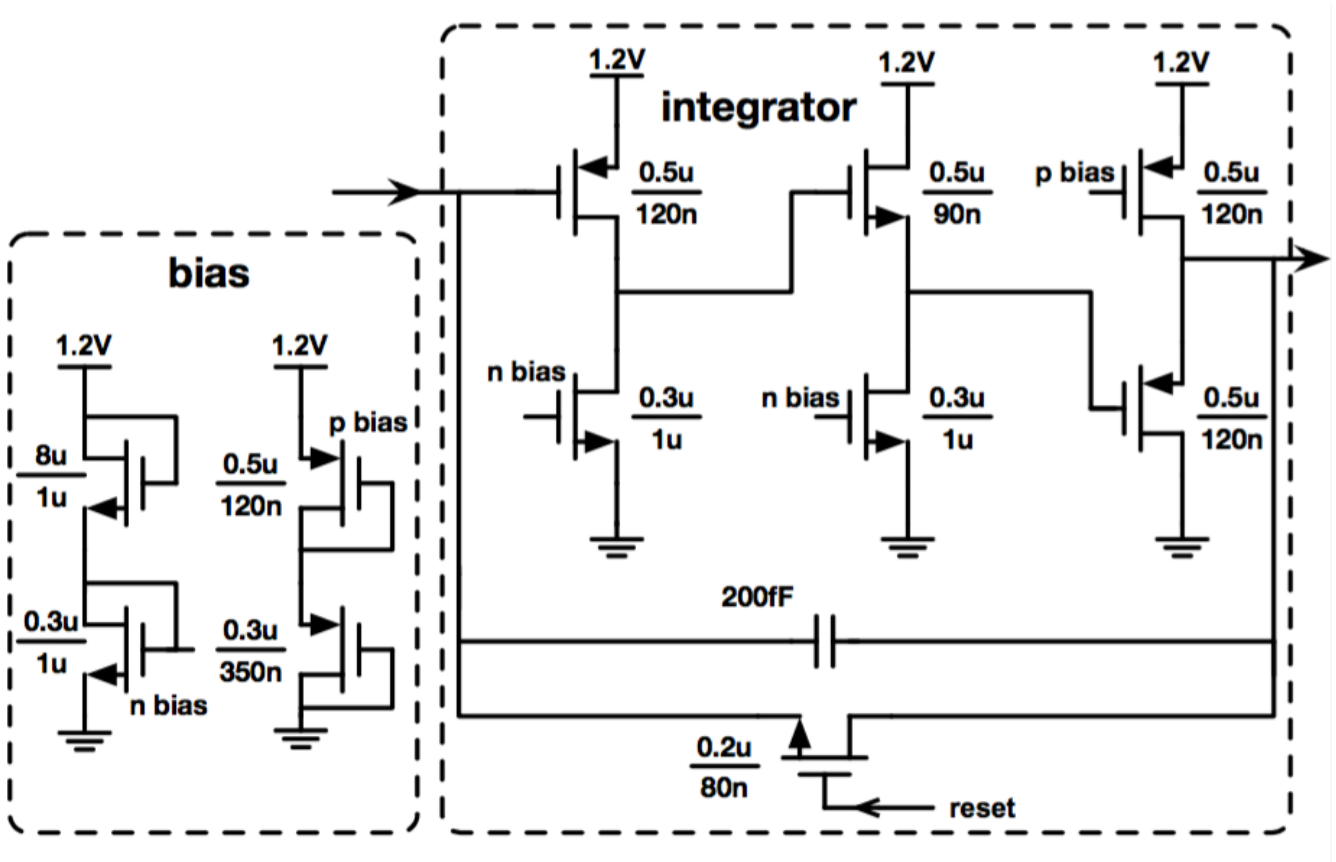
Mechanical Issues

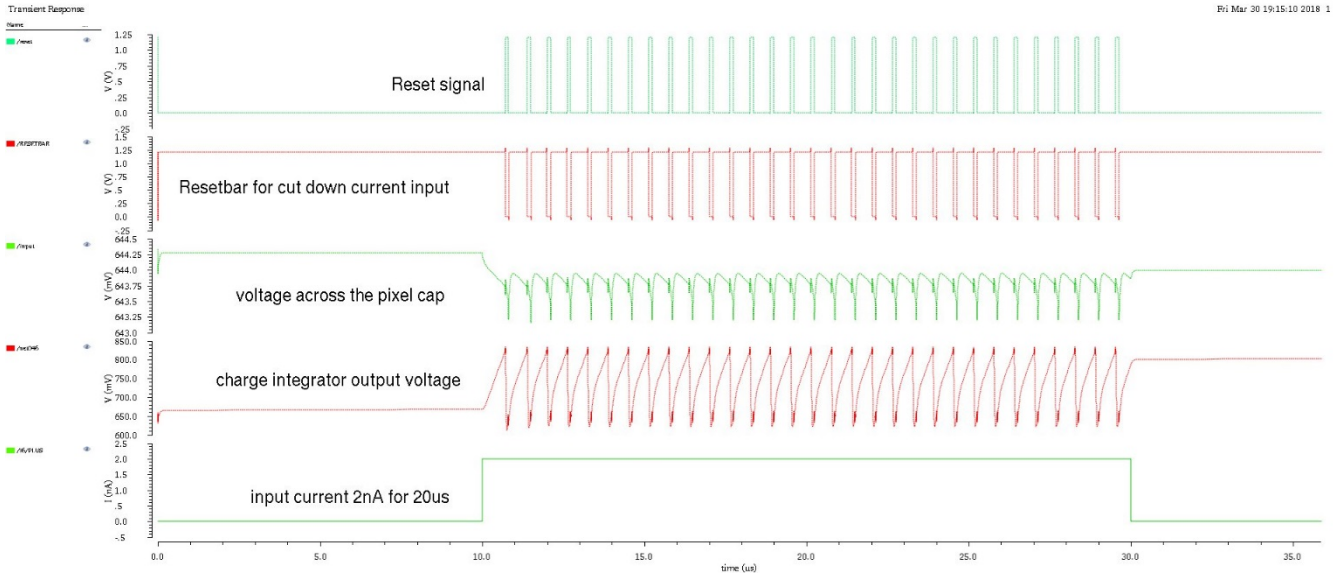
- How to make a flat APA with 60 sub-panels – how flat does it need to be?
- No tension forces so maybe a much lighter frame??
- If one does a double sided APA as in DUNE then can hide wiring and supports in interstitial space between opposite panels
- Can panels extend over frame to eliminate dead regions? Precision?
- How do photon detectors? Cathode, in front of pixels, field cage?????

What are we missing?

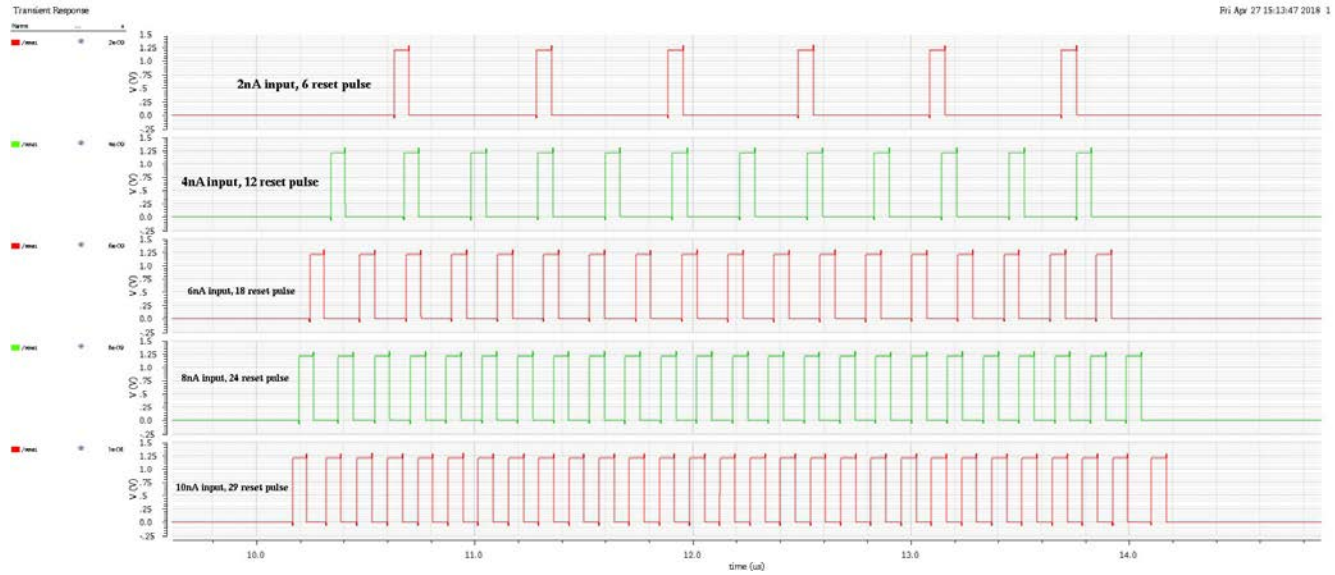
Backup

P. Wang, L. Du, Charge Integrator





Simulation results for 2nA_20us input current



Reset pulse waveform for different current input – post layout

Layout