6x6x6 Light detection system meeting

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APC - Astroparticule et Cosmologie

Development Goals

CatiROC

Implement an PMT dedicated, latest generation ASIC

\+ integrate with an state of the art Stratix IV FPGA

Advanced, non ASIC features

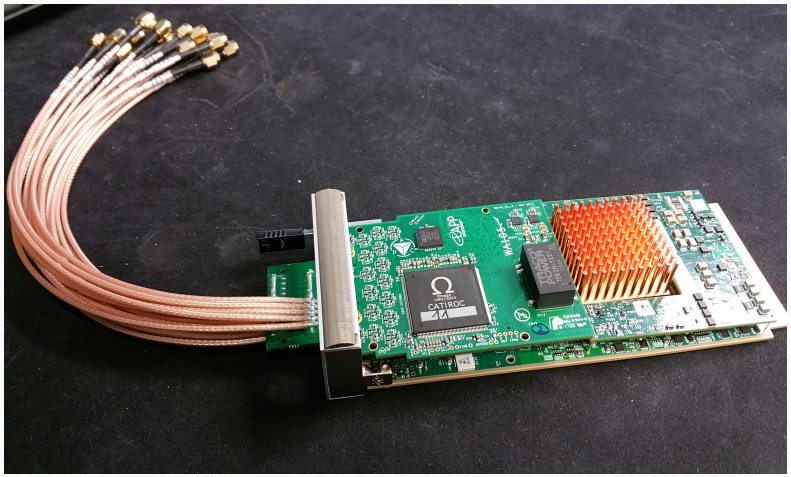
- Dead timeless monitoring system + digital event tagging
- Online trigger efficiency computing
- Endless (x-bits) time stamping, etc.

ADC

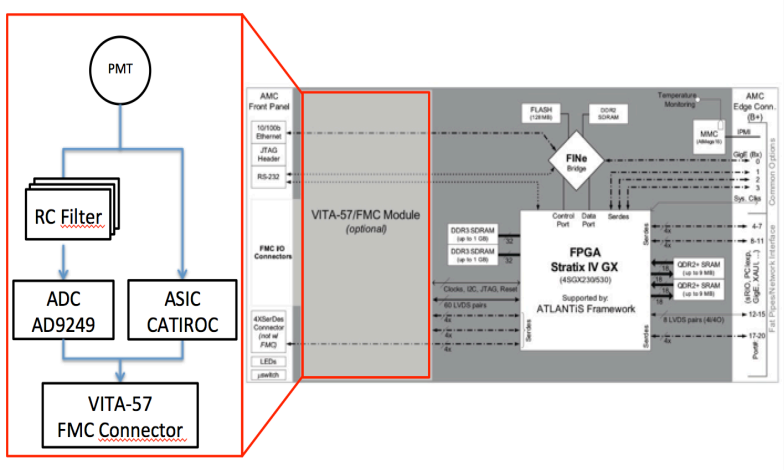
Perform DPP on the samples within FPGA fabric

- Sampling @40 MHz of analog signals
- Computing falling tail, averaging, windowing, etc.
- Event rejection, pile up handling, etc.

FMC Mezzanine Overview



AMC + mezzanine / Block diagram



- Splitting of 16 PMT analog inputs
- Anti aliasing, low pass filter
- FMC connector / Mother board Bittware S4AM
- Dedicated ASIC, software controlled
- Full analog processing
- Readout from ASIC to FPGA
- Provides light trigger to experiment
- ADC to improve measurement of charge
- Samples are merged and processed in FPGA
- 4 Spare I/0 signals

Current Status

Electrical test OK

All reference voltage levels (2.5 V. Vadj, 3.3 V., etc.) OK

IO spare signals OK

Reference 1.2 V. and - 0.4 V. levels OK.

Comparators and level shifters OK

All S4AM/FMC interface signals OK

Full pinout validated - No surprises there

Issue with 100 Ohms adaptation seems solved - measured, to be confirmed by Bittware

No Jtag available: minor issue, annoying for the developer ...

Firmware: CatiROC controller IP

Validated by experience with few different hardware (slow control, data capture, etc.)

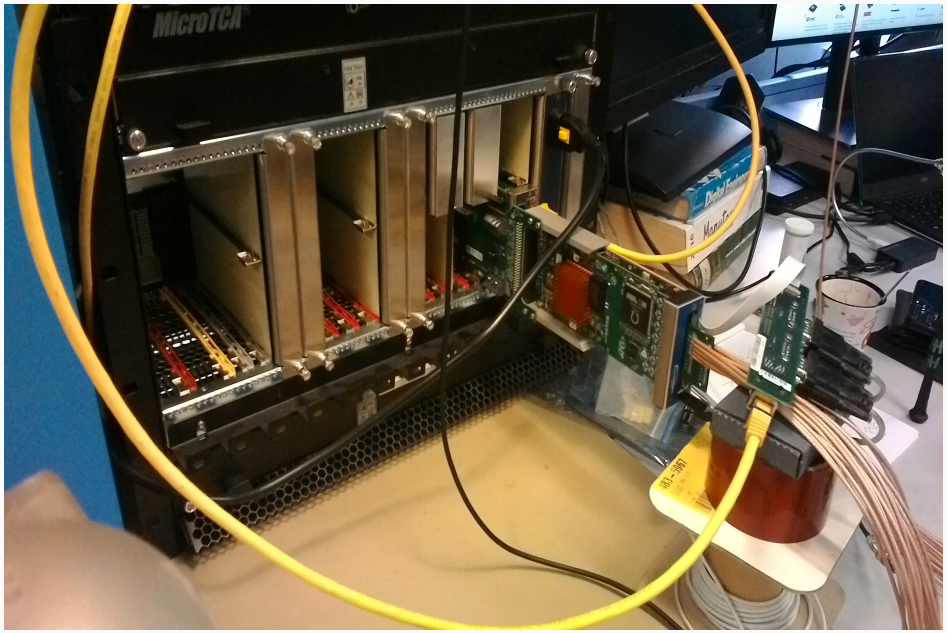
Online under GPL3 at http://bit.ly/2JPJFOa

Firmware: ADC

IPNL example template project running - all setup checked

Under adaptation from 8x8 ADCs to 1x16 ADC - Same component

Next Steps



- Adapt example code (FIFO based)
  - Oscilloscope mode
  - Capture data from 1 ADC
  - Put data on disk
  - Perform data analysis
- Add CatiROC controller IP (stream based)
  - adapt NIOS software
  - adapt labview software
- Crosscheck data
- Perform fine analysis
- Implement multi board
- Work on sync

Conclusion

A lot still to do

Hardware almost validated

Firmware still under development

Backend software/DAQ supported by IPNL

CatiROC Proved, tested and characterized on different projets

uTCA Standard rather time demanding: too many tricks to know ...

Existing example code running + proved firmware IP ...

... but reduced manpower.

Hopefully, three latest July weeks should be more efficient for developments.

Ancillary: Global System Overview

12 channels x 3 slots = 36 channels / uTCA crate

All channels run synchronously, all events are time stamped

Integrated with the charge readout electronics via the common time base and the back-end receiving the data

12-Channels	Triggerless mode, with locally generated triggers (discriminator output of leading edge on fast shapper channel within the CatiROC ASIC)
AMC local trigger	ORing of all 12 triggers within the FPGA; output through spare outputs
Crate trigger	Daisy chain / star readout of AMC local triggers
System trigger	Global OR trigger of all channels

Triggerless operation or during beam time in an external trigger mode via white rabbit

Several crates in sync with the dedicated AMC slave node