LRO Front End to DAQ Interface and tests

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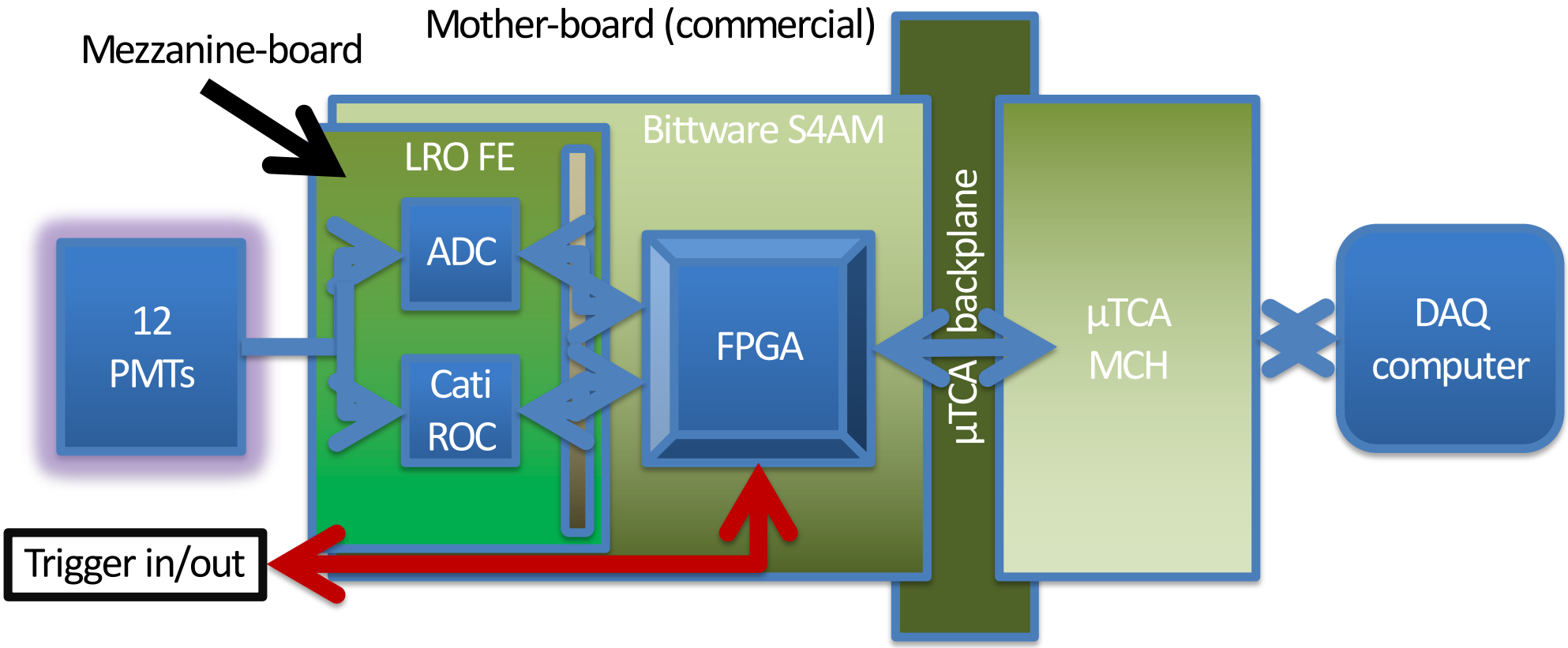
LRO FE block diagram



LRO FE Operation Modes

- **Light trigger** (not beam events)：LRO FE will provide a trigger signal to the DAQ by a LVTTL electrical signal.
  - The LRO trigger will be based on the coincidence of signals (over a threshold level) from selected PMTs during a time window.
  - All the parameters: time window, PMTs contributing and signal threshold will be programable.

- **Beam**: an external trigger via White-Rabbit will be received on the LRO FE.
- **Calibration**: an external trigger signal will be received at the LRO FE synchronized with the calibration system light pulse emission.

LRO FE Operation Parameters

A software interface is required to program on-line the different operation parameters of the LRO FE boards:

- **Operation mode:** light trigger, beam or calibration.
- **Sampling frequency:** from 15ns to 400ns.
- **Data output mode:** continuous or only after a trigger (during a time window to be defined).
- The **PMTs that contribute to the trigger**.
- **Signal threshold level** for the trigger decision.
- Length of the **coincidence time window** for the trigger.

Those parameters can be sent from the DAQ to the FE in a text file when any parameter must be updated.

LRO FE Debugging Interface

For the testing of the LRO FE a communication link with the DAQ is required for the debugging of the LRO FE hardware and firmware. With commands like:

- Reset
- Write / Read FPGA internal registers (trigger inputs, configuration parameters, status of the state machine, …).
- Write / Read Catiroc registers.
- Start / Stop data reading (from Catiroc or ADC)

Proposed tests

First tests can be done only with FE and DAQ, using signal generators for the PMT inputs:

- Check the interfaces (HW and SW) between the Catiroc and the FPGA: configuration interface, discriminator outputs, …
- Check the FE light trigger performance with different PMTs trigger levels and configurations.

Once we have a test setup with the **final electronics, PMTs, cables, feedthroughs,…** at least**,** for **one channel**:

- Measure the background noise in order to have an idea of the minimal gain required on the PMTs to distinguish the signal from the noise.
- Obtain the gain vs voltage calibration for one PTM with the Catiroc and the ADC in order to compare the results with both chips.
- Compute the maximum signal rate that the FE is able to time-stamp.

In any case a debugging interface is needed for the communication between DAQ and FE.

CATIROC ASIC

- **16 inputs** for negative signals that work in **trigger-less mode**: each input auto-triggers according to a programed threshold. External input available for **external trigger .**
- All the channels are **handled independently** by the digital part and only channels that have created triggers are digitized and then sent-out.
- **Each input signal** follows two paths:

- **Slow path** for charge and time measurement:
  - Programmable shaping time (up to 100ns)
- **Fast path** for auto-trigger:
  - Fast shaper (5ns) + programmable discriminator (same level for all the channels).
  - One trigger output pin is available per channel and also a pin with a NOR of the 16 trigger signals.

- Provides the "time of arrival" operating in self-triggered mode with a time resolution of 200 ps RMS. Given by the combination of :
  - **Coarse time** from a 26 bit counter at 40 MHz (set to 0 at the chip restart).
  - **Fine time** obtained by two TACs (Time to Amplitude Converters) per channel.
- The **conversion (dead) time** depends on the input signal magnitude. Conversion of large input signal could take up 6.4 µs, the average conversion duration is 3.2 µs.

ADC AD9249

- 16 channels with 14 bits resolution.
- Sampling frequency up to 65MHz (40 MHz on the FE).
- **Differential inputs** with 2Vpp voltage range and common mode voltage at 1V. So, **1V of dynamic range.** Conversion from unipolar PMT signals to differential ADC inputs is done in the anti-aliasing filter at the input.