16 Channel, 14-Bit, 65 MSPS, Serial LVDS, 1.8 V ADC

Data Sheet **AD9249**

FEATURES

- **Low power**
  - **16 ADC channels integrated into 1 package**
  - **58 mW per channel at 65 MSPS with scalable power options**
  - **35 mW per channel at 20 MSPS**
- **SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)**
- **DNL: ±0.6 LSB (typical); INL: ±0.9 LSB (typical)**
- **Crosstalk, worst adjacent channel, 10 MHz, −1 dBFS: −90 dB typical**
- **Serial LVDS (ANSI-644, default)**
  - **Low power, reduced signal option (similar to IEEE 1596.3)**
- **Data and frame clock outputs**
- **650 MHz full power analog bandwidth**
- **2 V p-p input voltage range**
- **1.8 V supply operation**
- **Serial port control**
  - **Flexible bit orientation**
  - **Built in and custom digital test pattern generation**
  - **Programmable clock and data alignment**
  - **Power-down and standby modes**

APPLICATIONS

- **Medical imaging**
- **Communications receivers**
- **Multichannel data acquisition**

GENERAL DESCRIPTION

The AD9249 is a 16-channel, 14-bit, 65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 65 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and an LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The AD9249 automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. Data clock outputs (DCO±1, DCO±2) for capturing data on the output and frame clock outputs (FCO±1, FCO±2) for signaling a new output byte are provided. Individual channel power-down is supported, and the device typically consumes less than 2 mW when all channels are disabled.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

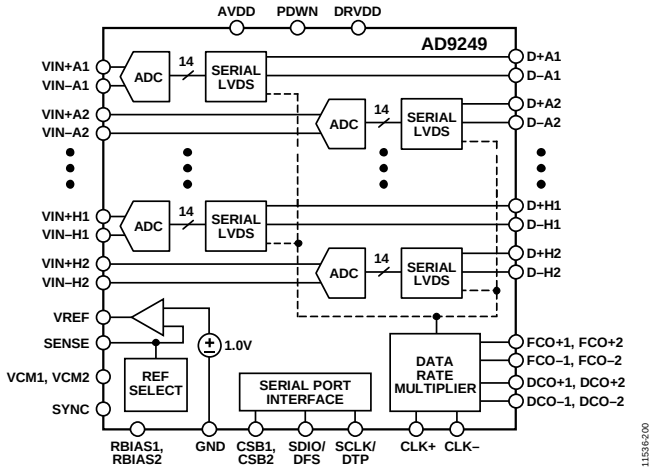

Figure 1.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation.

The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9249 is available in an RoHS-compliant, 144-ball CSP-BGA. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Sixteen ADCs are contained in a small, 10 mm × 10 mm package.
2. Low Power. 35 mW/channel at 20 MSPS with scalable power options.
3. Ease of Use. Data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 455 MHz and support double data rate (DDR) operation.
4. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. 0 **Document Feedback**

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SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	0	0.24	0.8	% FSR
Offset Matching	Full	0	0.24	0.7	% FSR
Gain Error	Full	−7.2	−3.5	+0.2	% FSR
Gain Matching	Full	0	1.8	6.0	% FSR
Differential Nonlinearity (DNL)	Full	−0.9	±0.6	+1.6	LSB
Integral Nonlinearity (INL)	Full	−3.0	±0.9	+3.0	LSB
TEMPERATURE DRIFT					
Offset Error	Full		−1.8		ppm/°C
Gain Error	Full		3.6		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.0	1.01	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		3		mV
Input Resistance	Full		7.5		kΩ
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		0.98		LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1 V)	Full		2		V p-p
Common-Mode Voltage	Full		0.9		V
Common-Mode Range	Full	0.5		1.3	V
Differential Input Resistance	Full		5.2		kΩ
Differential Input Capacitance	Full		3.5		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD}	Full		395	429	mA
I_{DRVDD} (ANSI-644 Mode)	Full		118	124	mA
I_{DRVDD} (Reduced Range Mode)	25°C		88		mA
TOTAL POWER CONSUMPTION					
Total Power Dissipation (16 Channels, ANSI-644 Mode)	Full		924	995	mW
Total Power Dissipation (16 Channels, Reduced Range Mode)	25°C		869		mW
Power-Down Dissipation	25°C		2		mW
Standby Dissipation[2]	25°C		199		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for information about how these tests were completed.
[2] Controlled via the SPI.

THEORY OF OPERATION

The AD9249 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 14-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9249 is a differential switched capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal dependent errors and achieve optimum performance.

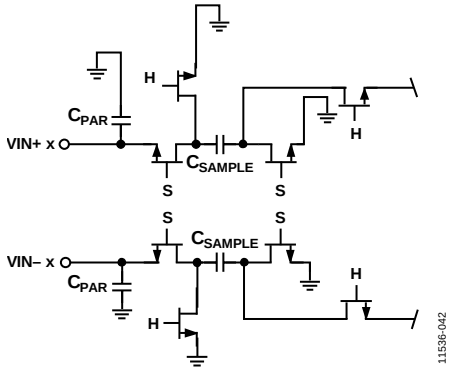


Figure 32. Switched Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 32). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values vary, depending on the application.

Input Common Mode

The analog inputs of the AD9249 are not internally dc biased. Therefore, in ac-coupled applications, the user must provide this bias externally. For optimum performance, set the device so that V_{CM} = AVDD/2. However, the device can function over a wider range with reasonable performance, as shown in Figure 33.

An on-chip, common-mode voltage reference is included in the design and is available at the VCMx pin. Decouple the VCMx pin to ground using a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9249, the largest available input span is 2 V p-p.

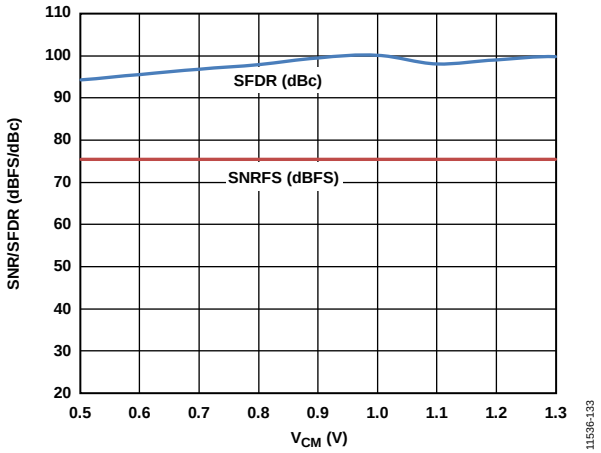


Figure 33. SNR/SFDR vs. Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

Differential Input Configurations

There are several ways to drive the AD9249, either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9249 provides excellent performance and a flexible interface to the ADC (see Figure 35) for baseband applications. Similarly, differential transformer coupling also provides excellent performance (see Figure 36).

Because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9249, use of these passive configurations is recommended wherever possible.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is recommended that the AD9249 inputs not be driven single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9249. Configure VREF using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section. Bypass the VREF pin to ground externally, using a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9249 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 34), setting VREF to 1.0 V.

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	GND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

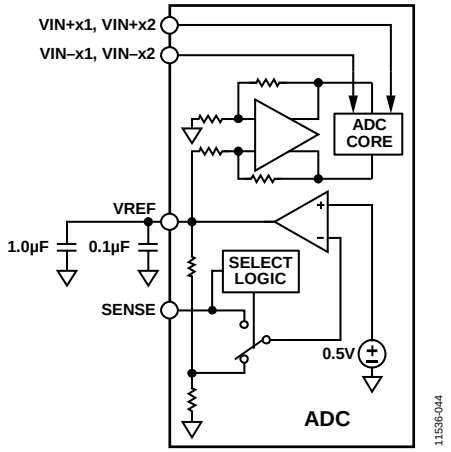


Figure 34. Internal Reference Configuration

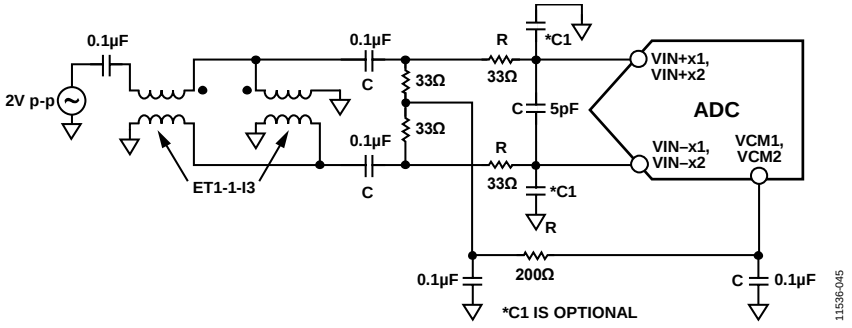


Figure 35. Differential Double Balun Input Configuration for Baseband Applications

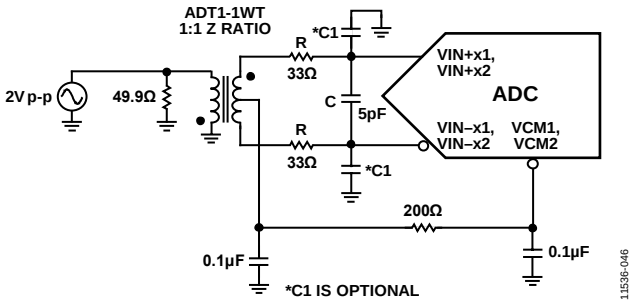


Figure 36. Differential Transformer Coupled Configuration for Baseband Applications

Figure 48 shows an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

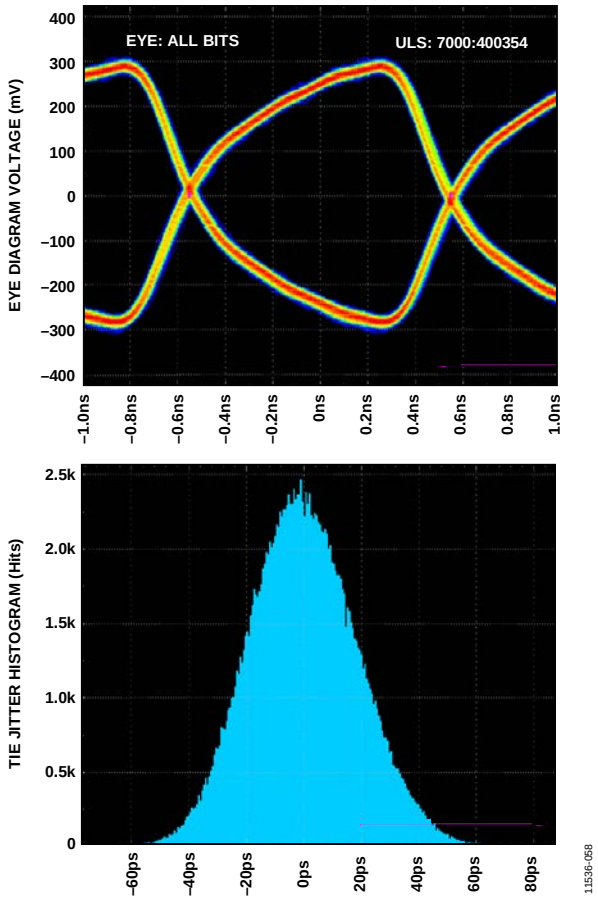


Figure 48. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

Figure 49 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position.

It is the responsibility of the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all 16 outputs to drive longer trace lengths, which can be achieved by programming Register 0x15. Although this option produces sharper rise and fall times on the data edges and is less prone to bit errors, it also increases the power dissipation of the DRVDD supply.

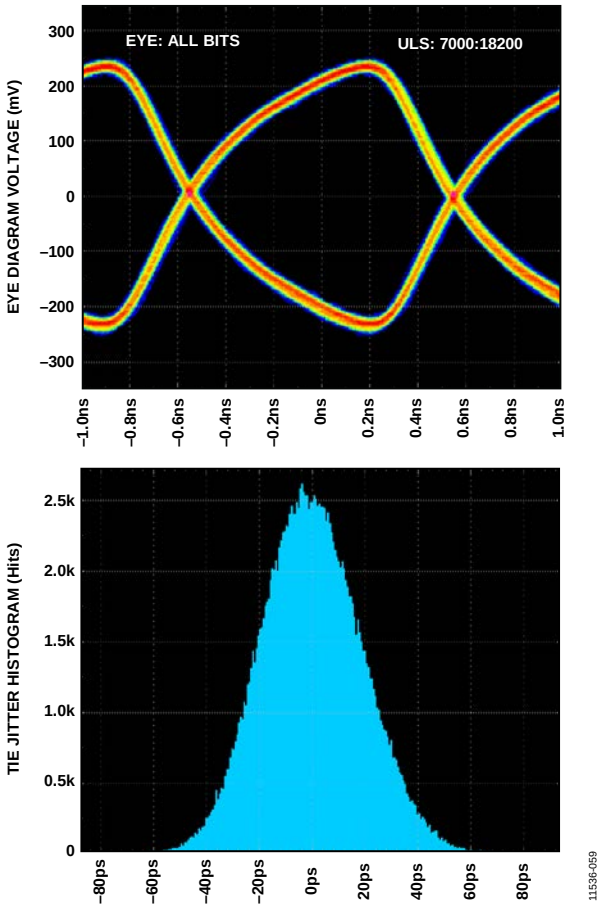


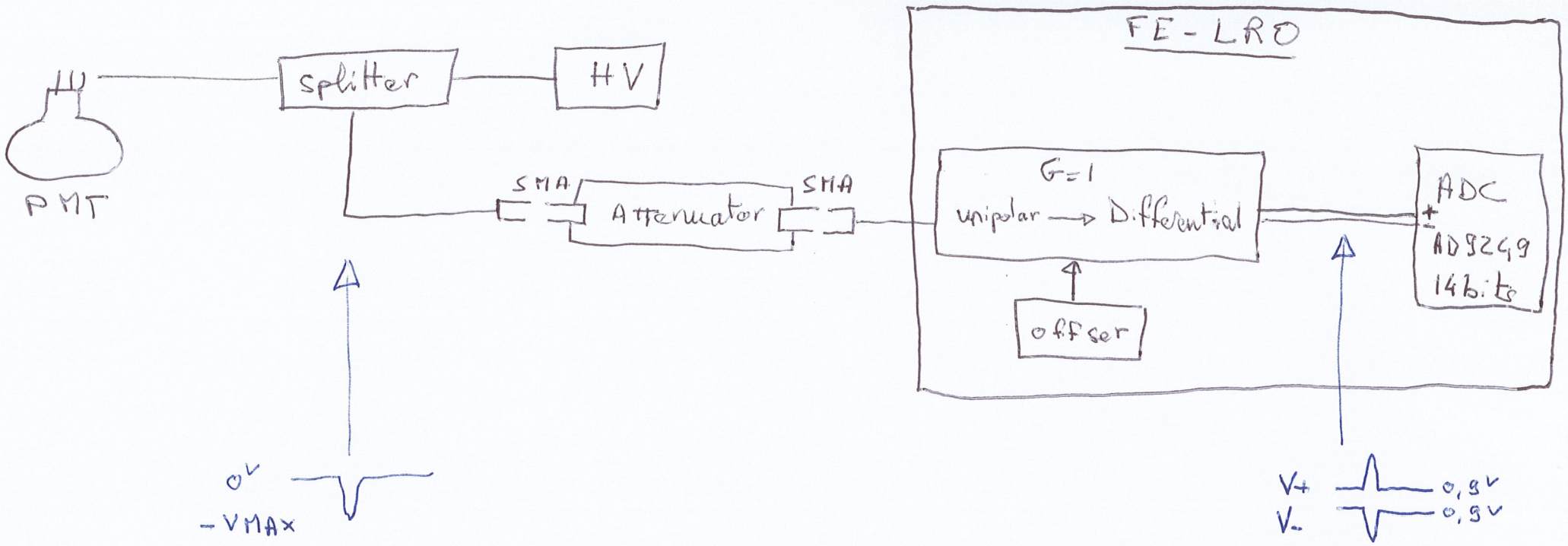
Figure 49. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater Than 24 Inches on Standard FR-4 Material, External 100 Ω Far End Termination Only

The default format of the output data is twos complement. Table 10 shows an example of the output coding format. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in DDR mode. The data rate for each serial stream is equal to 14 bits times the sample clock rate, quantity divided by 2, with a maximum of 455 Mbps (14 bits × 65 MSPS)/2 = 455 Mbps. The lowest typical conversion rate is 10 MSPS. See the Memory Map section for details on enabling this feature.

Table 10. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111



GOAL:

0V (⎺_⎺) → $V_+ - V_- = -V_{Ref}$

V+ 0,9V, 0,4V
V- 1,4V, 0,9V

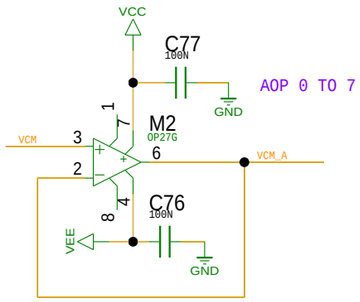
$\frac{-V_{MAX}}{2}$ (⎺V⎺) → $V_+ - V_- = 0$

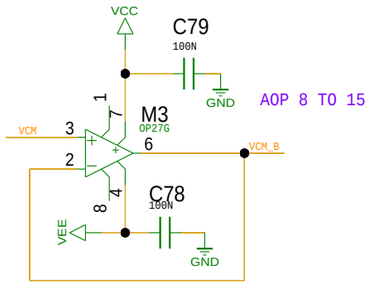
V+ 0,9V
V- 0,9V

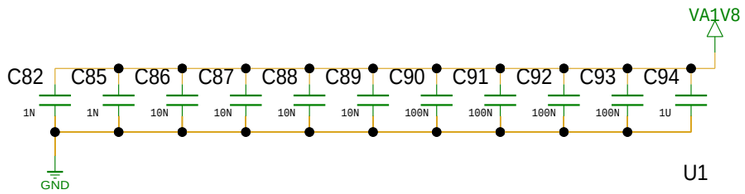
-VMAX (V) → $V_+ - V_- = V_{Ref}$

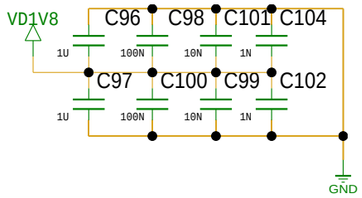
V+ 1,4V, 0,9V
V- 0,9V, 0,4V

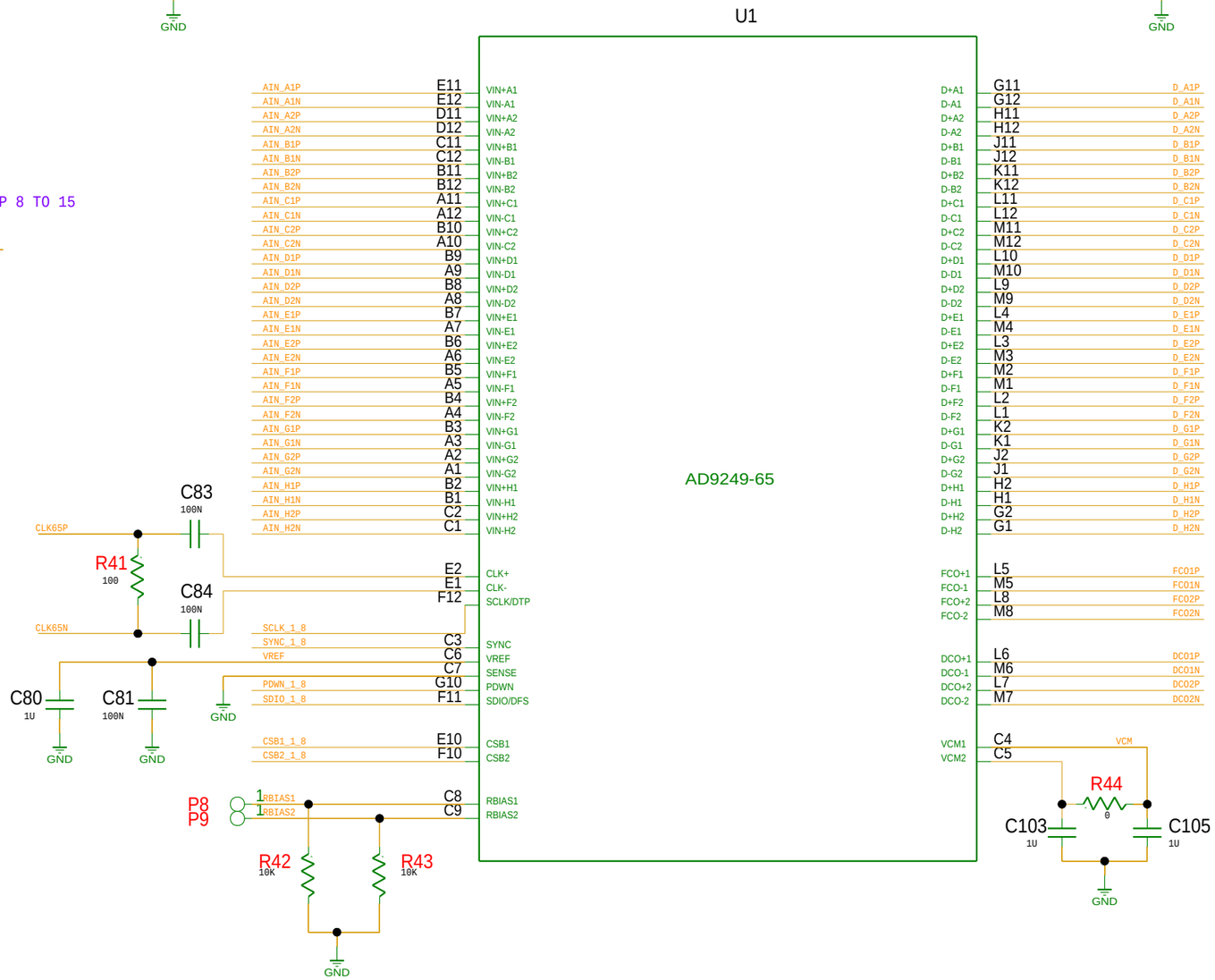
ADC











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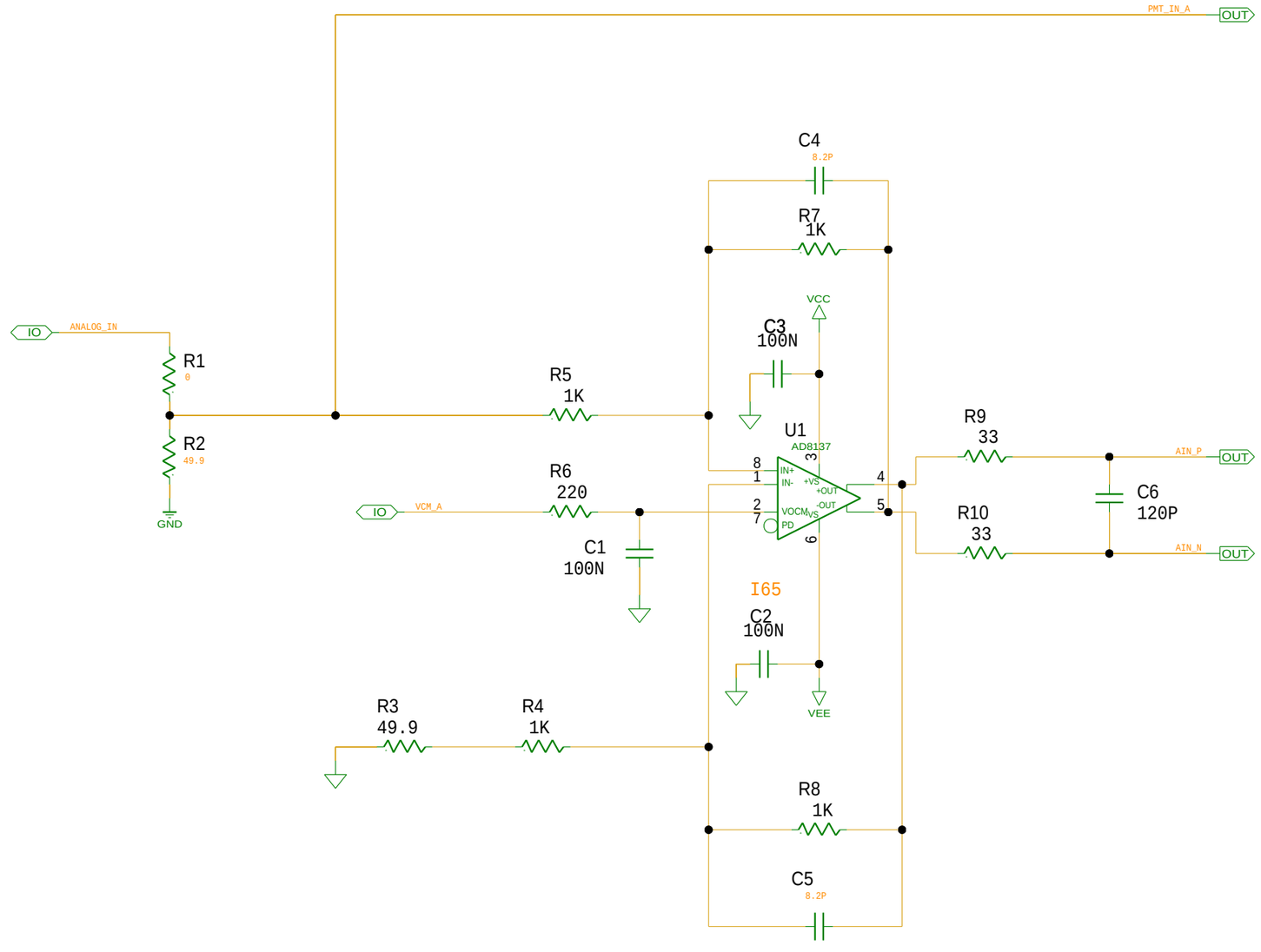
	DESSIN: REV 2	DATE: 15/12/2016

DIFFERENTIAL INPUT FROM PM



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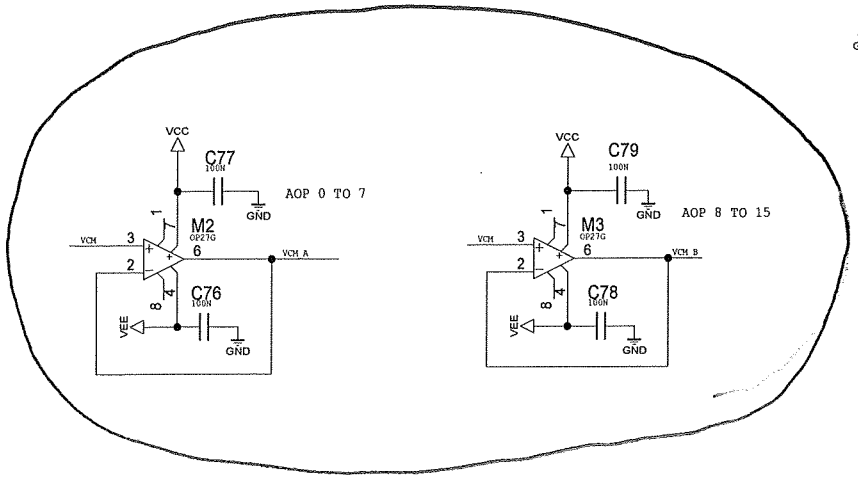
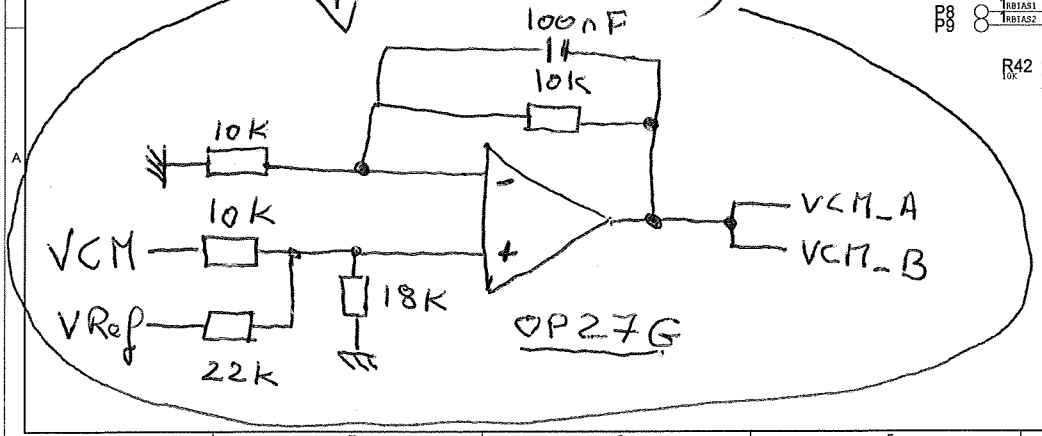
	DESSIN: REV 0.9	DATE: 23/07/2015

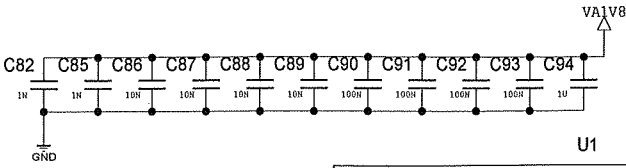
ADC

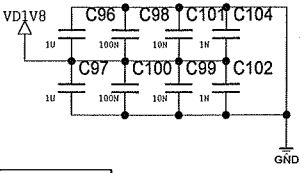


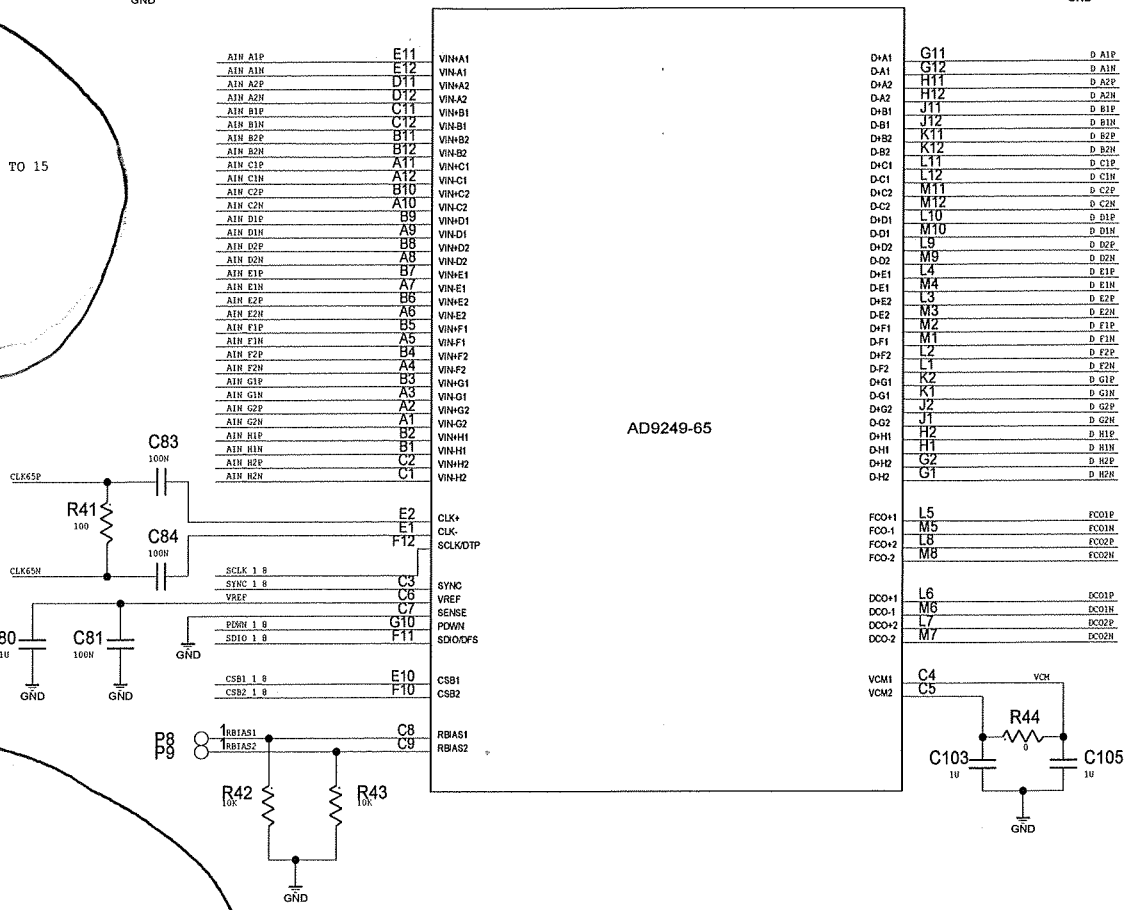
Replace by

(Pierre Prat, APC)









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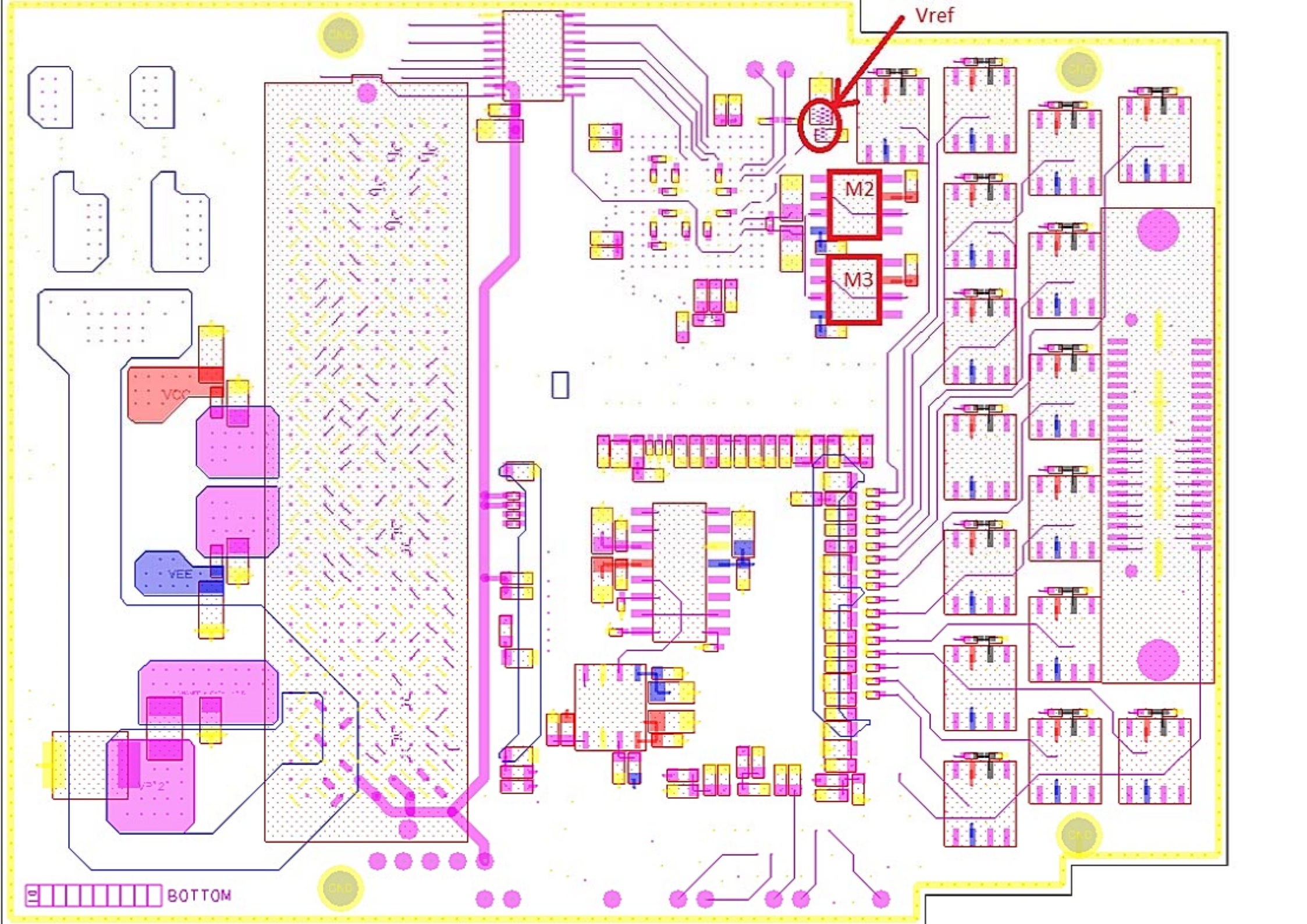
Vref
M2
M3
VCC
VEE
BOTTOM

VAT-10+
FXD SS ATTEN / SMA / RoHS
Connector Type: SMA

Connector types may vary. Please refer to datasheet for details.

RoHS

Data, Drawings & Downloads

DATASHEET

View Data

View Graphs

S11 S12
S21 S22 S-PARAMETERS

Case Style - FF704

Environmental Rating - ENV28T6

View All

Additional Information

Export Info

Coaxial, 3 dB, 6 dB, and 10 dB Attenuation, DC to 2000 MHz

Model Number	Case Style	Conn. 1	Conn. 2	F Low (MHz)	F High (MHz)	Nom. Attenuation (±0.3) (dB)	Flatness (dB) Typ.	VSWR (:1) Typ.	Power (W)
SF-BM-10+	DJ870	SMA-Female	BNC-Male	DC	2000.0	10.0	0.1	1.1	0.5
SM-BF-10+	DJ871	SMA-Male	BNC-Female	DC	2000.0	10.0	0.1	1.1	0.5

Coaxial (Type N), 0.5 to 1.0 Watt, 1 to 20 dB, DC to 6000 MHz

Model Number	Case Style	F Low (MHz)	F High (MHz)	Nom. Attenuation (dB)	Flatness (dB) DC - 3 GHz Max	Flatness (dB) 3 - 4.5 GHz Max	Flatness (dB) 4.5 - 6 GHz Max	Flatness (dB) DC - 6 GHz Max	VSWR (:1) DC - 3 GHz Typ.	VSWR (:1) DC - 3 GHz Max.	VSWR (:1) 3 - 4.5 GHz Typ.	VSWR (:1) 3 - 4,.5GHz Max.	VSWR (:1) 4.5 - 6 GHz Typ.	Power (W)
UNAT-1+	FF779	DC	6000.0	1.0	0.2	0.15	0.1	0.45	1.05	1.2	1.1	1.43	1.4	1.0
UNAT-2+	FF779	DC	6000.0	2.0	0.2	0.25	0.15	0.5	1.07	1.2	1.22	1.43	1.5	1.0
UNAT-3+	FF779	DC	6000.0	3.0	0.2	0.1	0.1	0.35	1.05	1.2	1.22	1.43	1.5	1.0
UNAT-4+	FF779	DC	6000.0	4.0	0.15	0.15	0.1	0.4	1.05	1.2	1.1	1.43	1.5	1.0
UNAT-5+	FF779	DC	6000.0	5.0	0.15	0.15	0.1	0.35	1.05	1.2	1.1	1.43	1.5	1.0
UNAT-6+	FF779	DC	6000.0	6.0	0.15	0.15	0.15	0.4	1.05	1.2	1.2	1.43	1.5	1.0
UNAT-7+	FF779	DC	6000.0	7.0	0.1	0.1	0.15	0.2	1.05	1.2	1.1	1.43	1.5	1.0
UNAT-8+	FF779	DC	6000.0	8.0	0.1	0.1	0.1	0.1	1.05	1.2	1.1	1.43	1.5	1.0
UNAT-9+	FF779	DC	6000.0	9.0	0.15	0.1	0.1	0.15	1.05	1.2	1.1	1.43	1.5	1.0
UNAT-10+	FF779	DC	6000.0	10.0	0.1	0.2	0.2	0.4	1.15	1.35	1.2	1.5	1.5	1.0
UNAT-12+	FF779	DC	6000.0	12.0	0.15	0.2	0.15	0.35	1.15	1.25	1.2	1.8	1.8	1.0
UNAT-15+	FF779	DC	6000.0	15.0	0.2	0.35	0.2	0.6	1.15	1.43	1.2	1.8	1.7	1.0
UNAT-20+	FF779	DC	6000.0	20.0	0.25	0.45	0.4	0.75	1.15	1.25	1.2	1.43	1.5	0.5
UNAT-30+	FF779	DC	6000.0	30.0	1.2	0.7	0.4	2.3	1.04	1.25	1.07	1.25	1.1	0.5

Attenuators, Coaxial (SMA), 0.5 to 1.0 watt, 1 to 30 dB, DC to 6000 MHz

Model Number	Case Style	F Low (MHz)	F High (MHz)	Nom. Attenuation (dB)	Flatness (dB) DC - 3 GHz Max	Flatness (dB) 3 - 5 GHz Max	Flatness (dB) 5 - 6 GHz Max	Flatness (dB) DC - 6 GHz Max	VSWR (:1) DC - 3 GHz Typ.	VSWR (:1) DC - 3 GHz Max.	VSWR (:1) 3 - 5 GHz Typ.	VSWR (:1) 3 - 5 GHz Max.	VSWR (:1) 5 - 6 GHz Typ.	Power (W)
VAT-1+	FF704	DC	6000.0	1.0	0.2	0.2	0.2	0.6	1.05	1.2	1.1	1.4	1.4	1.0
VAT-2+	FF704	DC	6000.0	2.0	0.2	0.2	0.25	0.65	1.05	1.2	1.2	1.5	1.5	1.0
VAT-3+	FF704	DC	6000.0	3.0	0.2	0.15	0.15	0.45	1.05	1.2	1.15	1.4	1.4	1.0
VAT-4+	FF704	DC	6000.0	4.0	0.2	0.15	0.2	0.55	1.05	1.2	1.15	1.45	1.45	1.0
VAT-5+	FF704	DC	6000.0	5.0	0.1	0.1	0.1	0.25	1.05	1.2	1.15	1.4	1.4	1.0
VAT-6+	FF704	DC	6000.0	6.0	0.15	0.1	0.2	0.45	1.05	1.2	1.15	1.4	1.5	1.0
VAT-7+	FF704	DC	6000.0	7.0	0.1	0.1	0.1	0.1	1.05	1.2	1.15	1.4	1.4	1.0