Front-end ASIC Digitizer

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UC Berkeley/LBNL
Mu2e-II Workshop
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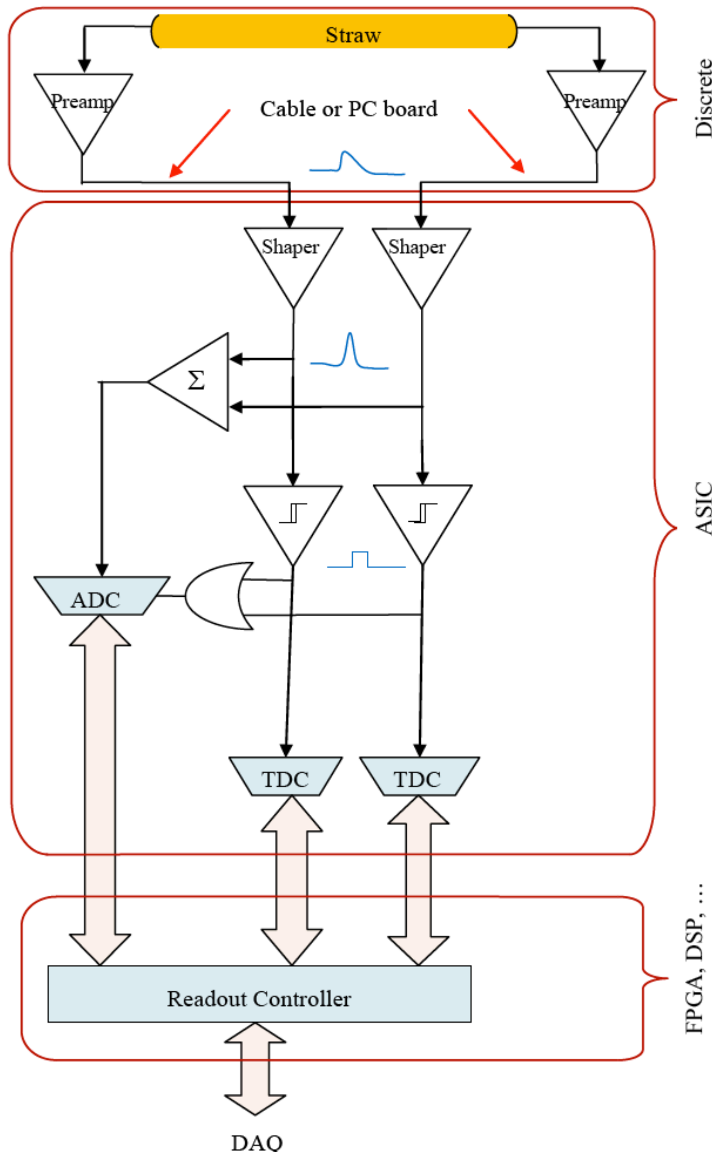
FEE Requirements For Mu2e-II ?



Experience from Mu2e

Read out straw signals on two sides, time division, ToT

Requirements for digitizer:

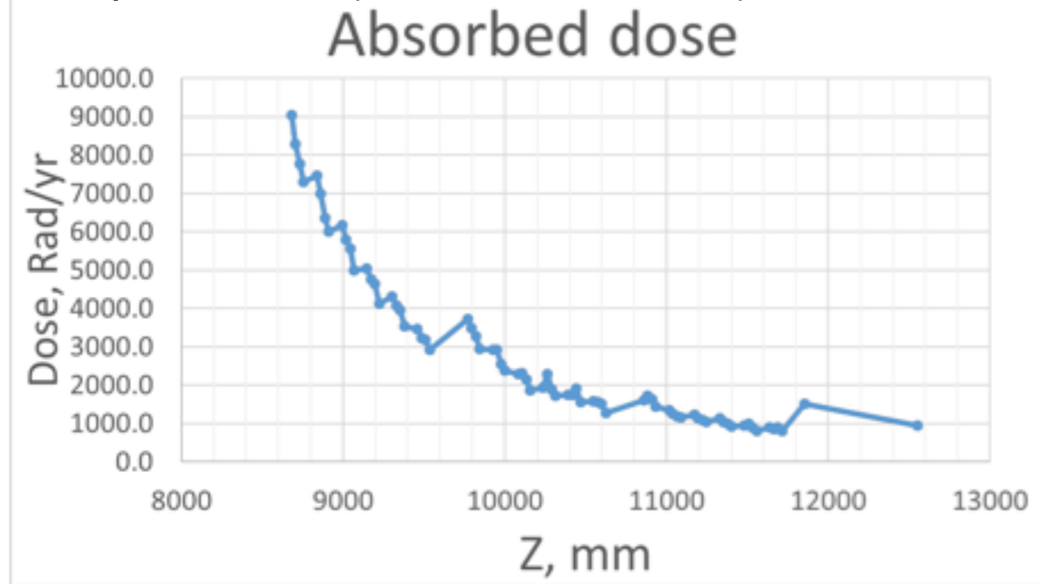
- Amplitude readout: waveform digitization @ ~50 MS/sec
- Resolution >7 ENOB
- Time division: σ(Δt) < 70 psec, σ(t) < 500 psec
- Deadtime ? Mu2e requirement: deadtime < 20-200 nsec
- Reliability and power
  - Digitizer power spec: <~150 mW/straw
  - Reliability: digitizer MTBF > 175 years. ~x10 TID compared to Mu2e

Challenges

- Excellent time resolution and stability
- High channel count
- High tolerance to neutron-induced SEUs, radiation hardness
- Cost (development)
- Mu2e has pivoted from ASIC baseline to COTS in 2014; DRAC has now successfully demonstrated performance (well, almost :)
- This experience has been very valuable
- Would COTS scale to Mu2e-II environment ?

Total Ionizing Dose

Mu2e requirements (from docDB-8938)



- Reduction with new geometry of ST

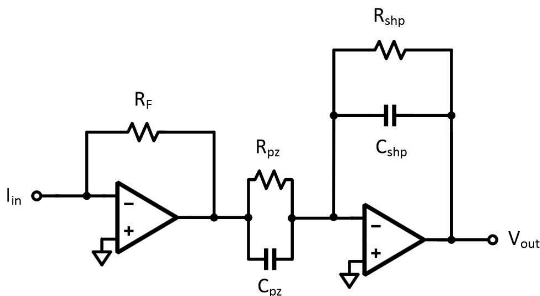
FEE mu2e Tracker/Vadim Rusu 2/8/2017

- Typical safety factors ~12, 5 years of running: ~200 kRad
- x10 for Mu2e-II: ~2 MRad.
- Could be more (e.g. new muon wedge design ?)
- Will need to leverage LHC experience and R&D
- COTS (FPGA) may not work: turn back to ASICs ?

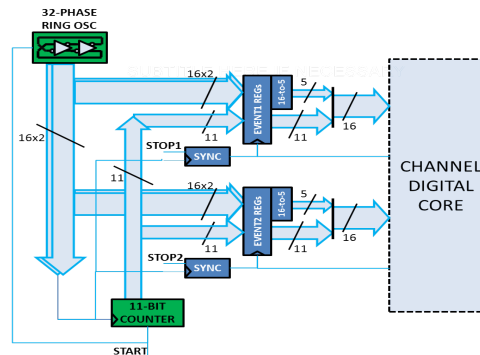
ASIC Development for Mu2e

- ASIC digitizer was the baseline until 2014
- Developed a prototype (POM 1.0)
  - Demonstrated ADC, TDC, shaper, discriminator specs, including SEE and (neutron-induced) dose
  - Had issue with clocking (understood)
  - Development terminated in 2014 (schedule requirements)
  - Performance documented in JINST **10**, P06007 (2015)

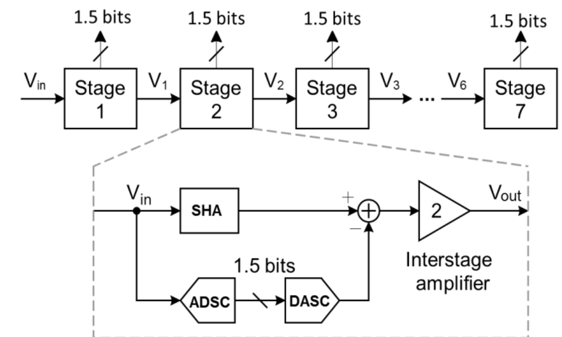
Low-noise preamp



32-phase ring oscillator TDC (16bit)



Low-power 8 bit pipeline ADC

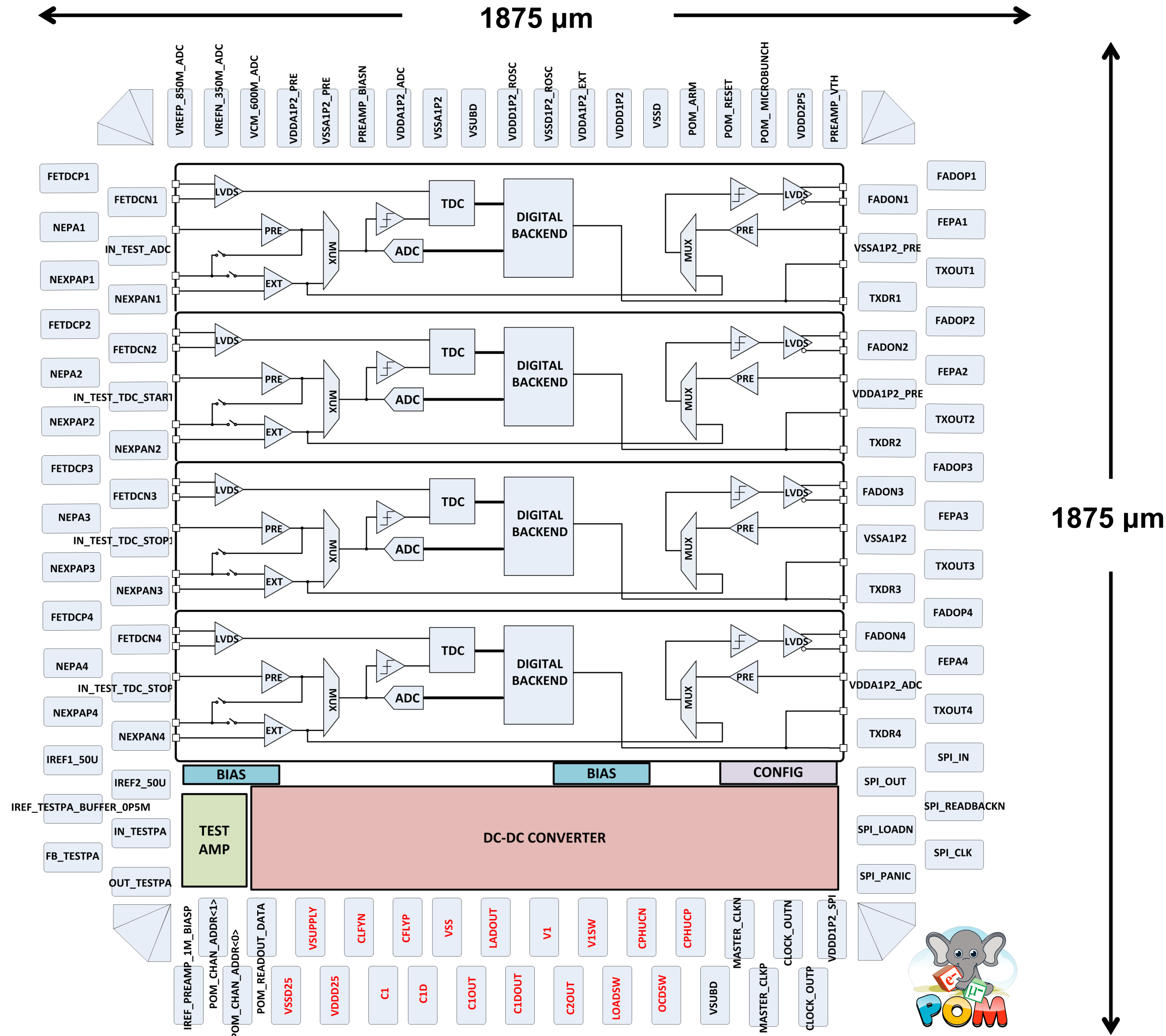


1.5 bits 1.5 bits 1.5 bits 1.5 bits

Mu2e ASIC Digitizer Prototype

POM1.0: a full 2-channel prototype
Analog buffer to receive preamp signals
2 discriminators/ TDCs per straw
One 8-bit ADC
Digital signals to ROC

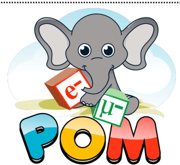
Functional prototype in TSMC TinyChip submission



1875 µm

1875 µm

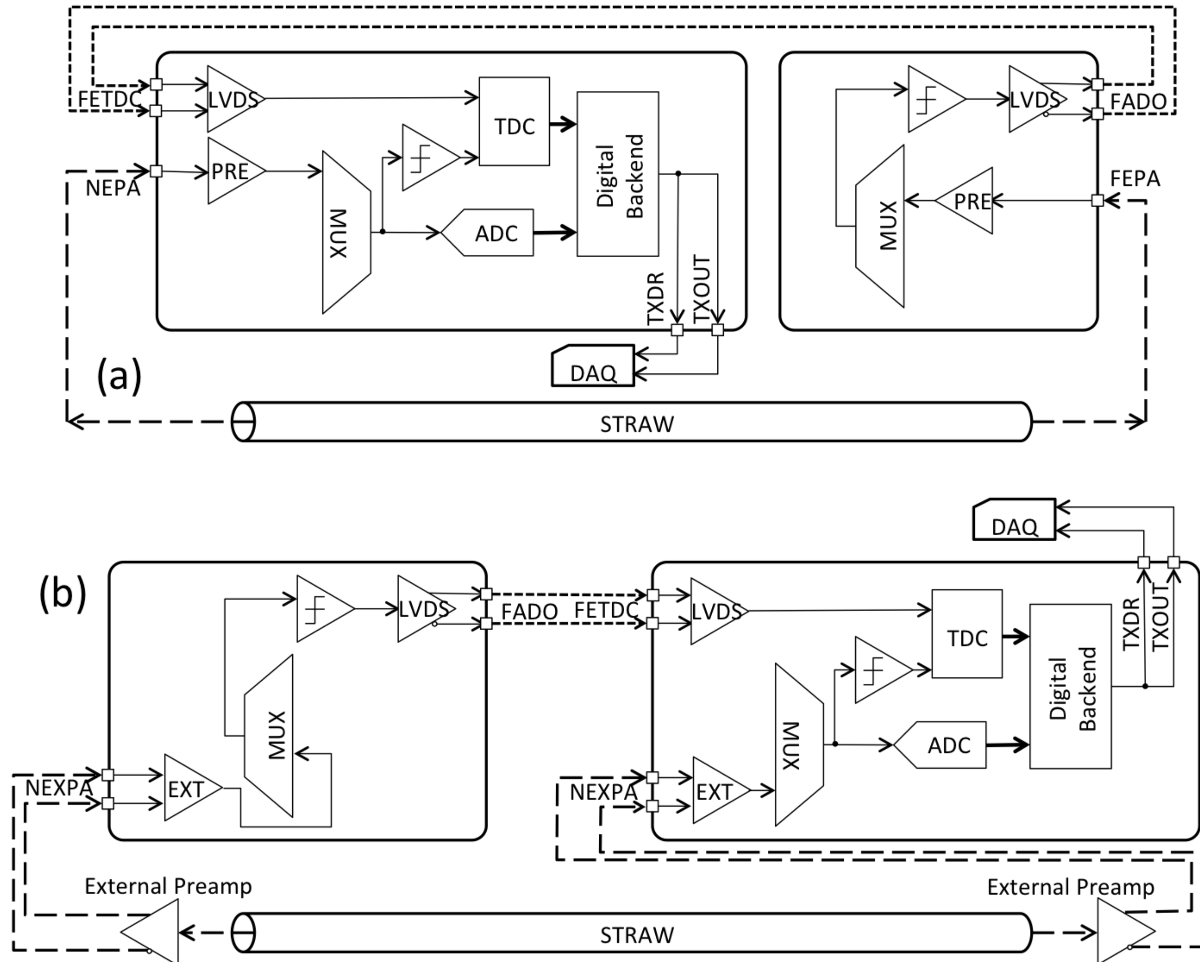
C. Grace



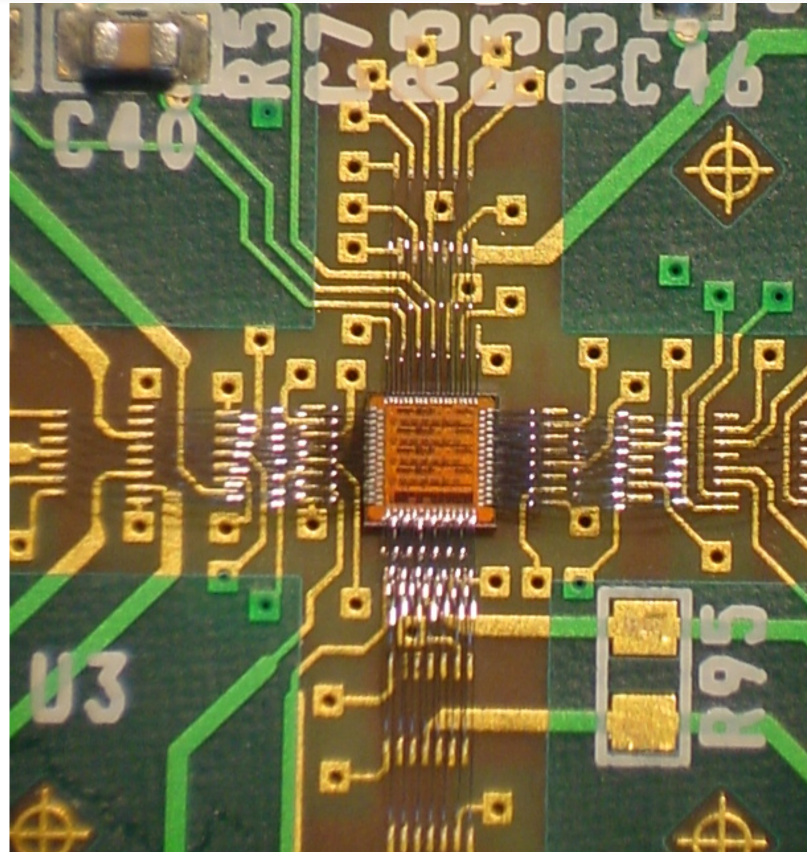
POM 1.0

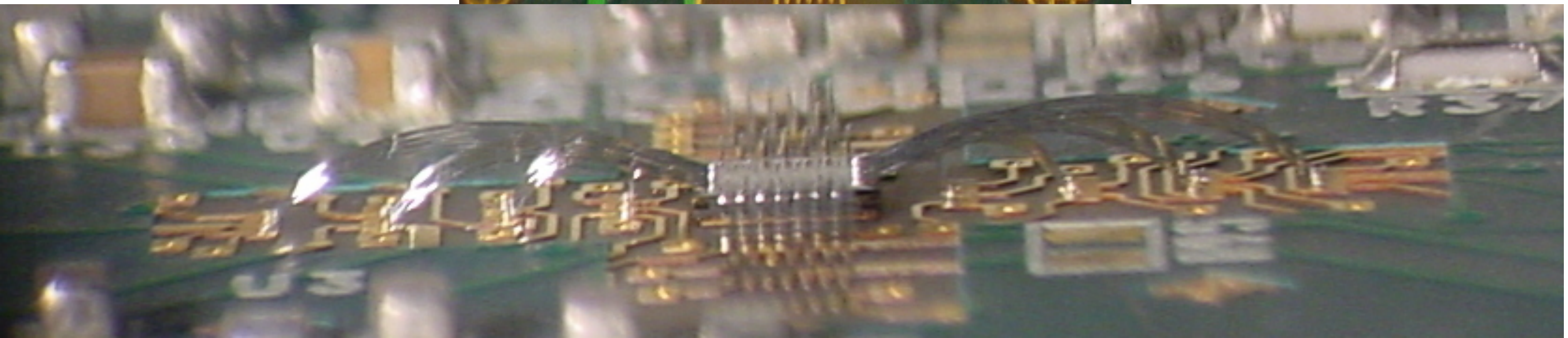
POM 1.0

2 modes of operation: internal vs external preamps

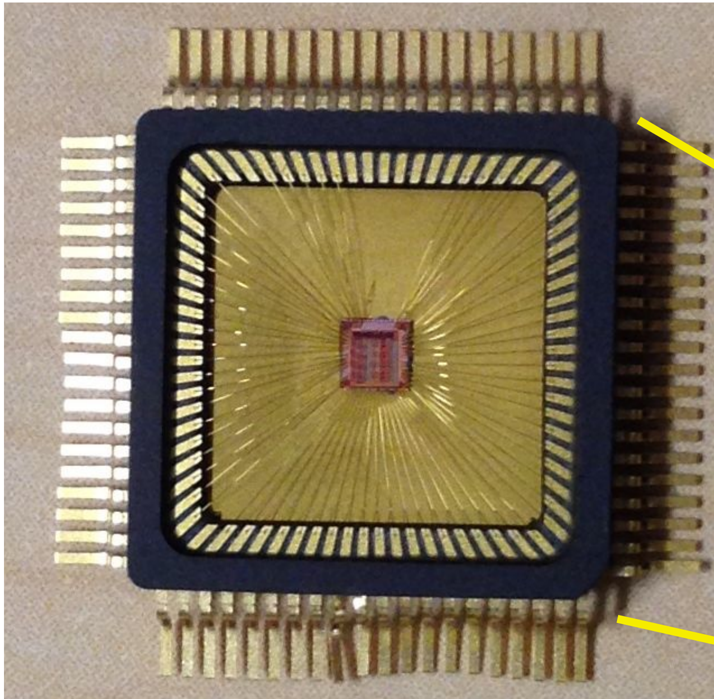


POM 1.0 on Test Board





Test Board V2



POM in package

ASIC ADC R&D: HIPPO

Pipelined 12-bit ADC based on 65nm process: compact, low power
LBNL design, Mu2e shared resources with BES (HIPPO) and ATLAS
Verified performance, radiation hardness

195 µm

160 µm

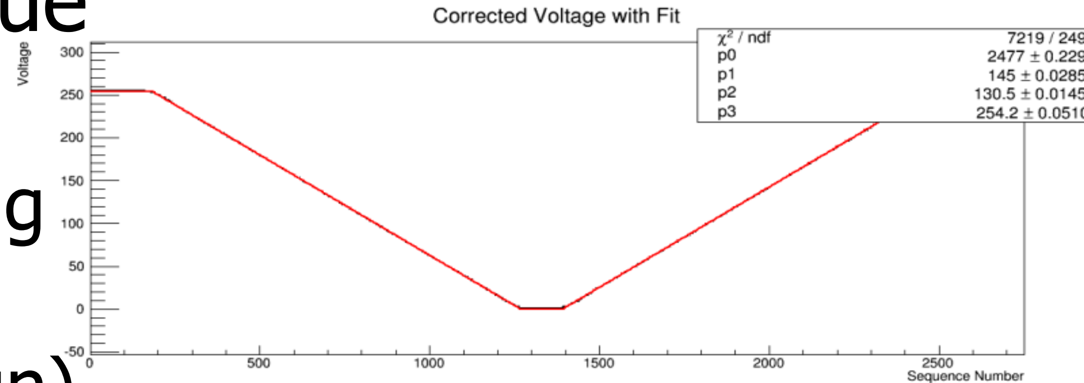
200 µm

1750 µm

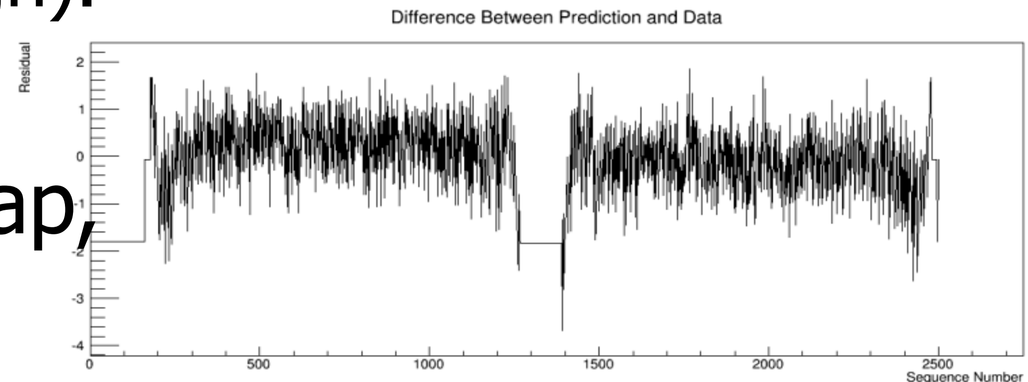
Pipelined ADC

ADC calibration

- ADC resolution limited by known design issue
  - Simulation study hits limitation when scaling down the ADC design (from precursor design).



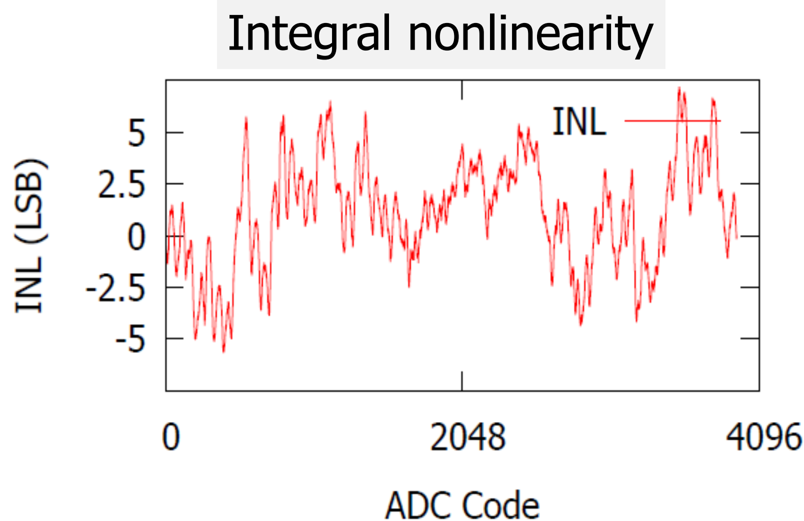
- Transfer function is extracted from hitmap, applied to waveform

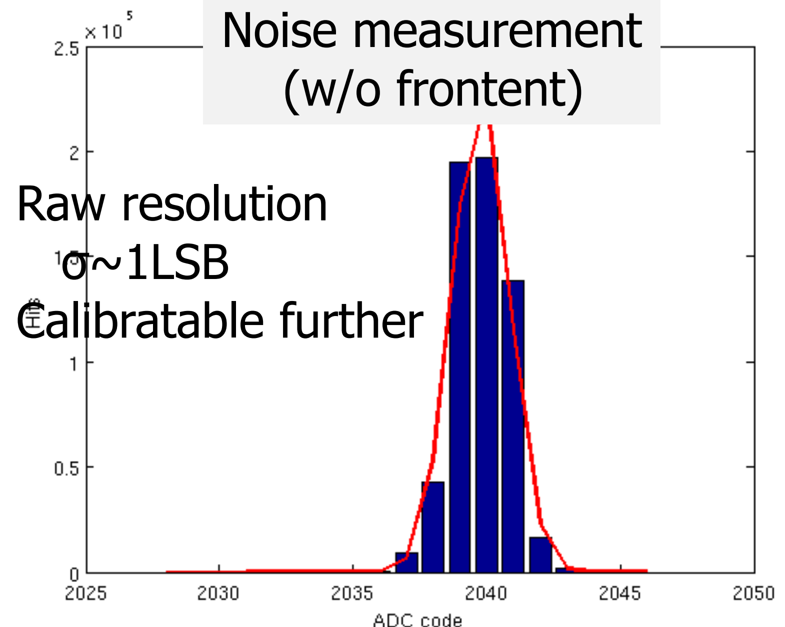


  - Effective number of bit = 6.8
  - Possible to improving ADC response by calibration

HIPPO ADC result

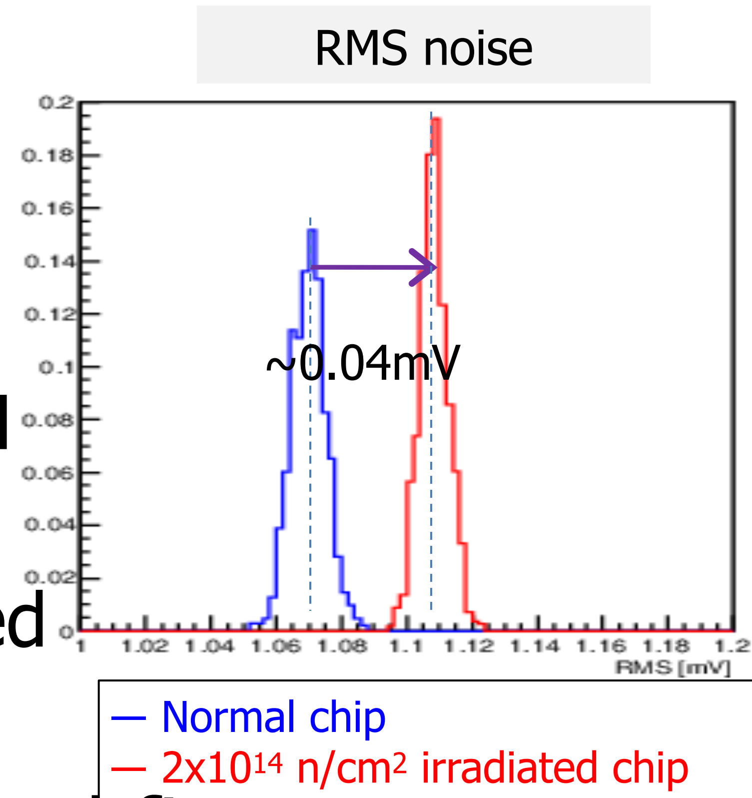
- The original 12bit ADC design is baseline of POM2.0
  - More power consumption (3.5 → 60mW/ch)
    - Total power (1.5kW) less than power requirement (10kW cooling capacity)
  - Better / proved performance : linearity, resolution





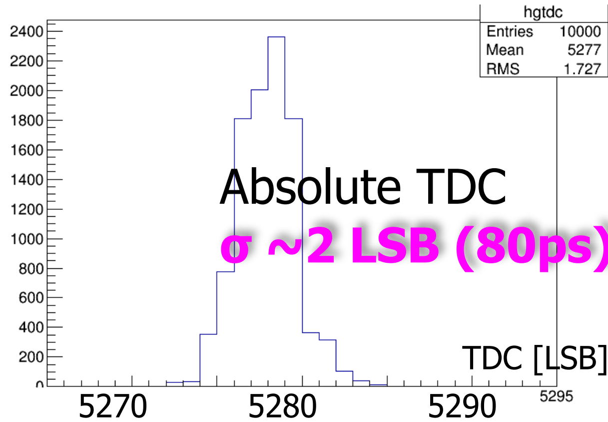
Neutron Radiation tolerance (ADC)

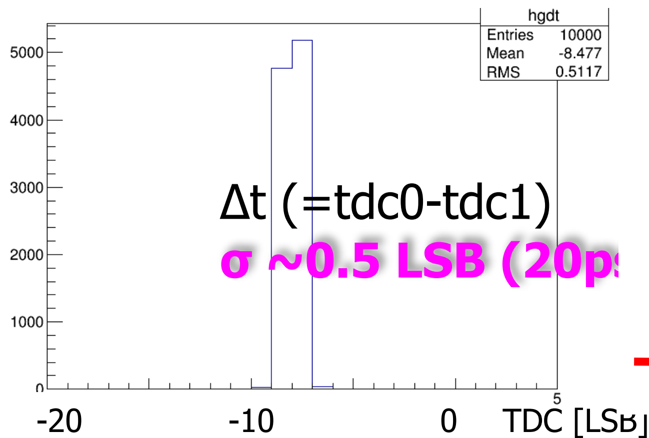
- HIPPO chip is irradiated with $2x10^{14}$ n/cm^2 neutrons.
  - UC Davis McClellan reactor
  - x100 Mu2e lifetime neutron dose at tracker electronics
  - ADC is the major part of POM
  - Data taken with seesaw signal input, fit/data compared to get noise level



- Irradiated HIPPO ADC worked fine
  - ~0.04mV (< 1LSB) noise increase observed.

TDC linearity, resolution in test mode



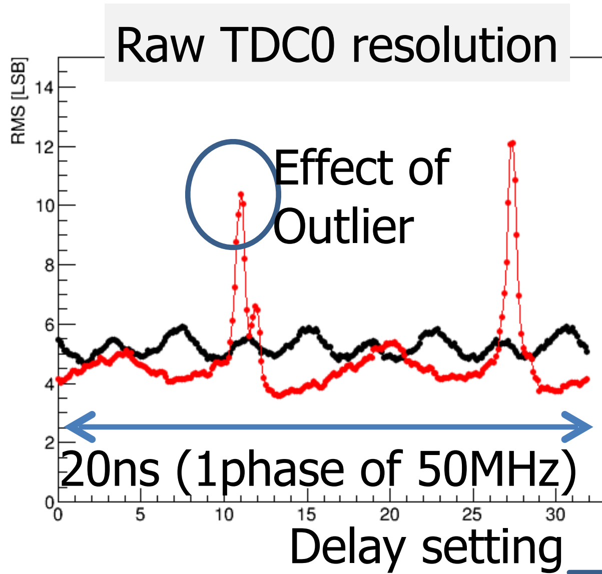


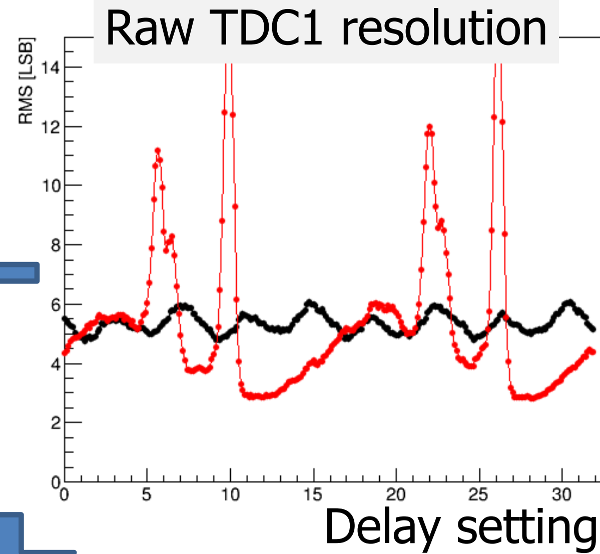
χ^2 / ndf 2.151e+07 / 4792
p0 5273 ± 0.07497
p1 25.59 ± 0.005195

Black : TDC data,
Red : linear fit
LSB ~39ps
25nsec
TDC
Residual
Residual = Data - Fit
50MHz
operation clock
Stop signal delay [ns]

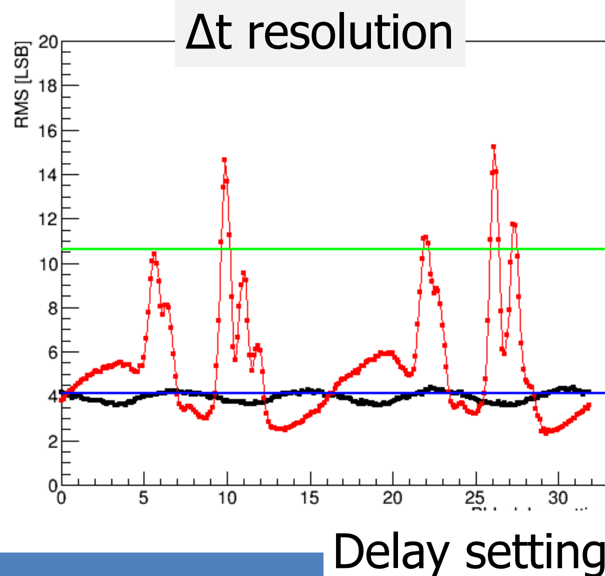
- Absolute time resolution ~80ps
- Intrinsic Δt resolution ~20ps
- LSB of TDC measurement = 39ps/TDC

Fine scan on TDC (analog mode)



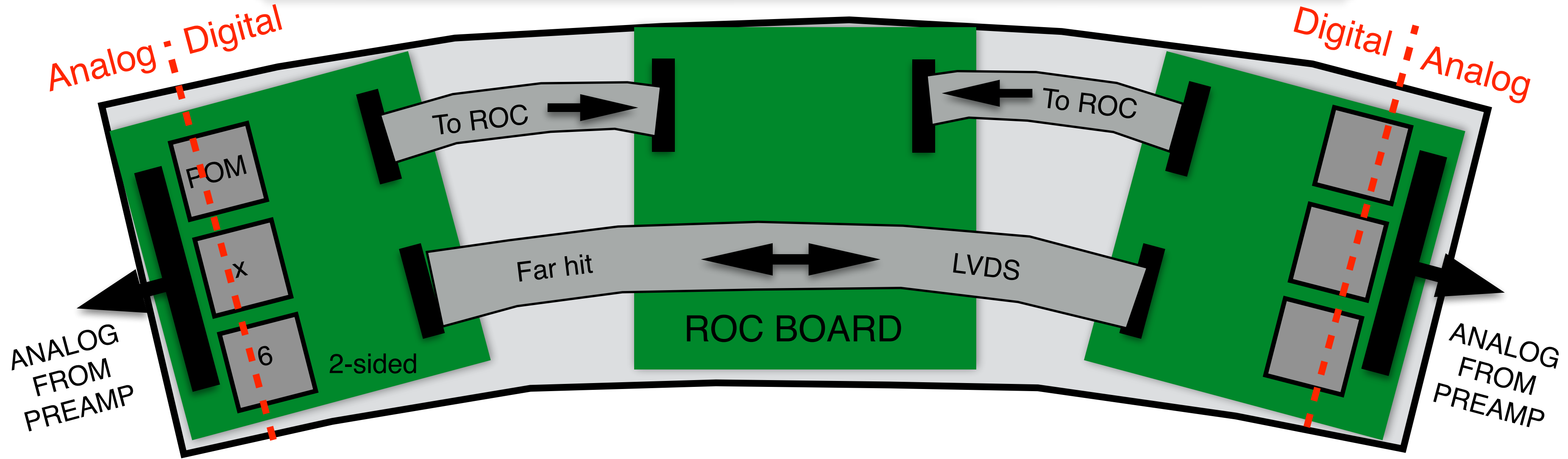


Red : with operation clock
Black : without clock
Green : Random trigger with clock
Blue : Random trigger without clock



- Clock feed-through to TDC (same as test mode)
  - Verified by turning off clock
  - Same effect on random triggering events

ASIC Motherboards Concept for Mu2e



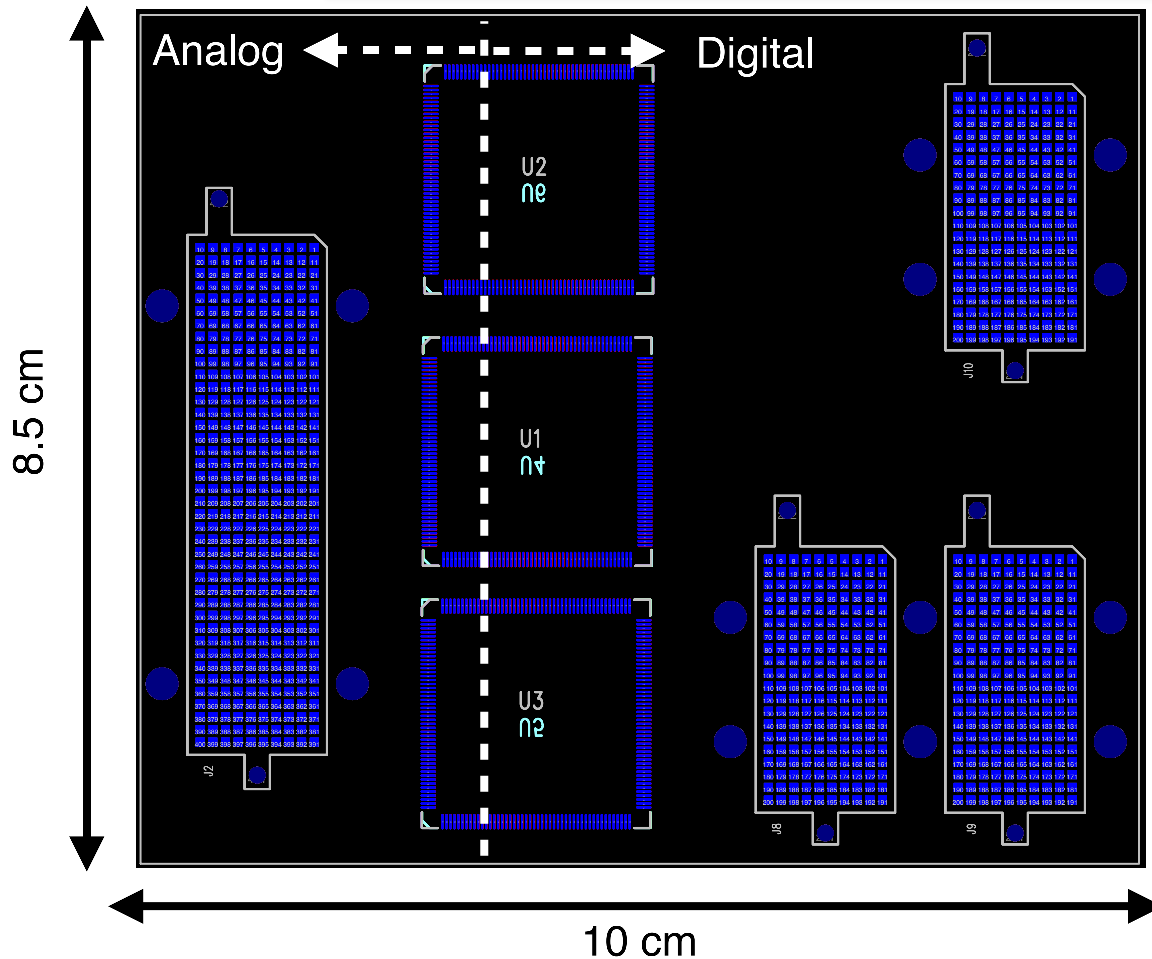
Compact packaging (12 ~1x1" packages or ~3x3mm flip chips)
Separate boards for digitizers and ROC: simplicity and reliability
Plenty of space for ROC, voltage regulators for preamps, diagnostic connectors, utilities. Good gas flow and cooling
Careful routing: separate digital from analog signals and grounds
Flex PCBs (3-4 layers) for connections to ROC and POMs
Interboard connector to preamp board: no need for bulkhead connector through the gas seal

Comments for Mu2e-II

- Raw FEE specs could be achieved by either COTS or ASICs
- SEU tolerance could be achieved by either
  - Mu2e: Altera → MicroSemi
- Experience with COTS says that achieving >MRad TID tolerance will be a challenge
  - Mu2e: SF2 → PolarFire, OK to ~600 kRad. What happens then ?
  - DACs, ADCs, BJTs tested to ~600 kRad. Found weak points and replaced. Possible with COTS, but slow process.
  - Could leverage HI-LHC R&D (often to GRad levels), but it is primarily focused on ASICs (65 nm now common)
- May need to be prepared for custom solutions
  - Digitizer would be fairly straightforward: POM, LHC experience
  - What do we do with ROC ? May need to be a custom solution, or look for rad-hard solutions (Xilinx ?)
  - Also consider auxiliary systems (DC-DC, optical links, …)

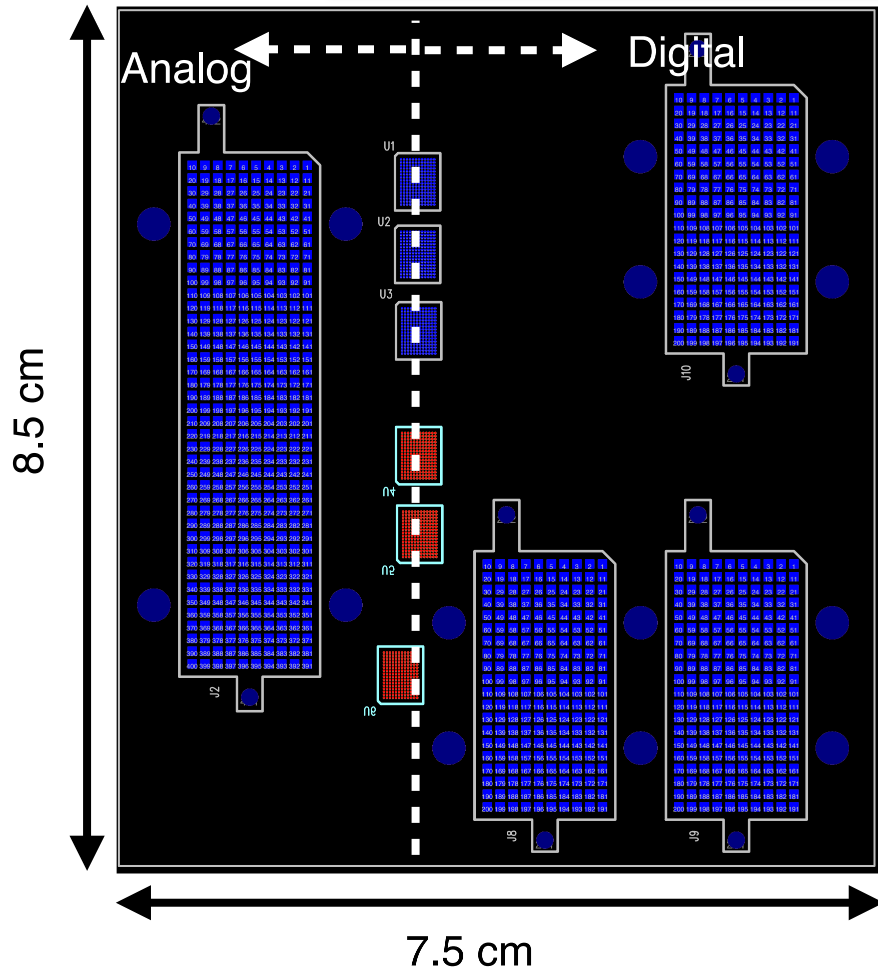
Backup

ASIC Motherboard: Packages



Two-sided board: 6 ASIC chips on each
144 or 192-pin package
Analog signals from the high-density "interposer" connector
Digital signals to ROC and the other POM board through high-density connectors and flex cables
8-10 layers, inexpensive

ASIC Motherboard: Flip Chips

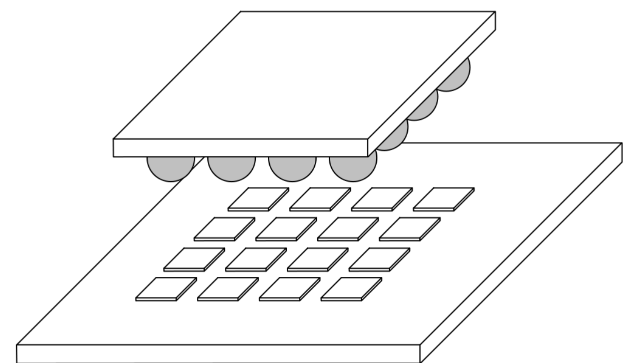


One- or two-sided board: 6 ASIC chips on each

Analog signals from the high-density interposer connector

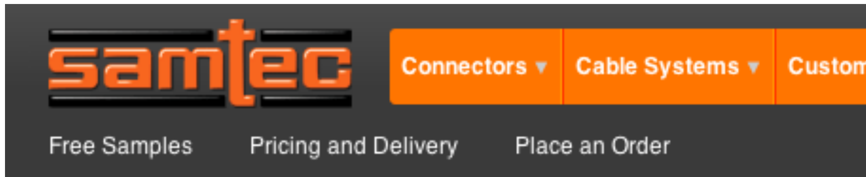
Digital signals to ROC and the other POM board through high-density connectors and flex cables

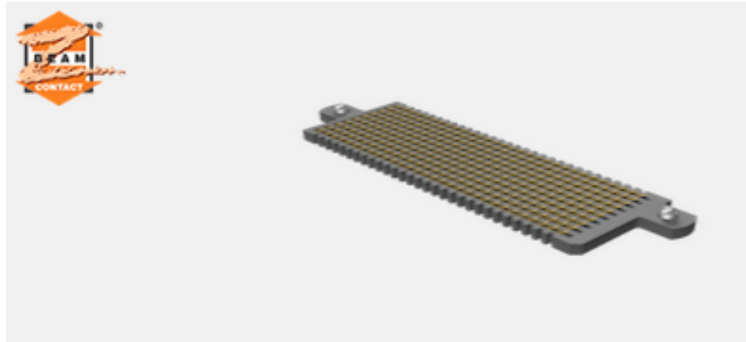
8-10 layers, inexpensive



Flip Chip

Connectors



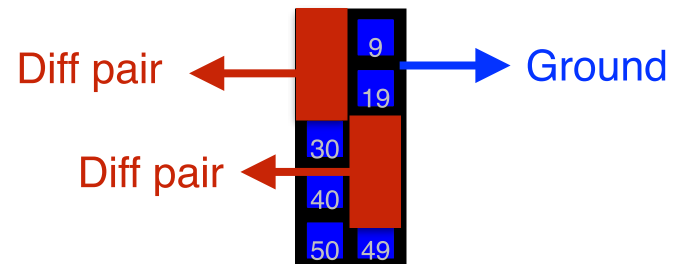


FEATURES

- Low Profile - 1,75 mm and 3,10 mm standard heights
- Ideal for board stacking, module-to-board and LGA interfaces
- Allows easy field upgrade, exchange
- Minimizes thermal expansion issues
- Up to 400 I/Os
- .050" (1,27 mm) pitch grid

RECOGNITIONS

Connector layout



High-density, low-profile connectors
No need for a bulkhead connector through the gas seal
Analog decoupling: separate diff pairs to reduce analog crosstalk

LBNL ASIC Experience

- Chip designers in Engineering Division (Henrik von der Lippe, et al)
  - Extensive expertise in ASIC design, first to adapt 65nm process in HEP
    - BaBar (ELEFANT, trigger), CDF (SVX), ATLAS (pixels, FE-I4), SNAP, etc.
    - One of the largest production and testing facilities among DOE labs